# SGM4591Q
# Automotive Low Voltage 16-Bit I²C and SMBus Low-Power I/O Expander

## GENERAL DESCRIPTION

The SGM4591Q is a general-purpose parallel input and output (I/O) expander device, which consists of two lanes and 8 bits parallel I/O expansion. The device communicates with processor through two-line bidirectional I²C bus (or SMBus), supporting I²C standard mode (100kHz) and I²C fast mode (400kHz) clock frequency. The SGM4591Q provides a simple solution for the devices that need additional I/Os, such as LEDs, buttons, sensors, etc.

The SGM4591Q is specified for automotive applications, which may select device address by the A0 and A1 pins. The SGM4591Q features an interrupt generated on the nINT whenever the state of input port changes. An output anomaly may also be indicated by the nINT pin when the corresponding nINT port register is set to 1. The SGM4591Q can cycle the power supply and cause a power-on reset to reset itself to the default state. In addition, the device can use a hardware nRESET pin to reset itself to the default state.

The device is AEC-Q100 qualified (Automotive Electronics Council (AEC) standard Q100 Grade 1) and it is suitable for automotive applications.

The SGM4591Q is available in a Green TSSOP-24 package and supports -40℃ to +125℃ temperature range.

## FEATURES

- **AEC-Q100 Qualified for Automotive Applications**
  **Device Temperature Grade 1**
  **$T_A$ = -40℃ to +125℃**
- **1.65V to 5.5V Input Voltage Range**
- **Parallel I²C I/O Expander**
- **5V Tolerant Input and Output Ports**
- **Active Low Reset Input**
- **Active Low Interrupt Output**
- **Support 400kHz I²C Fast Mode**
- **Internal Power-on Reset**
- **No Glitch on Power-up**
- **Polarity Inversion Register**
- **Compatible with Most Processors**
- **Select Device Address by Two Pins (up to Four Devices)**
- **Latched Outputs Drive LEDs Directly**
- **Latch-up Performance (>100mA) to Meet JESD 78 Class II Standard**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in a Green TSSOP-24 Package**

## APPLICATIONS

I²C GPIO Expansion
Automotive Infotainment and Body Electronics, ADAS, Hybrid Vehicles, Electric Vehicles and Powertrains
Automation in Industrial, Factory, Building, Test and Measurement

## TYPICAL APPLICATION

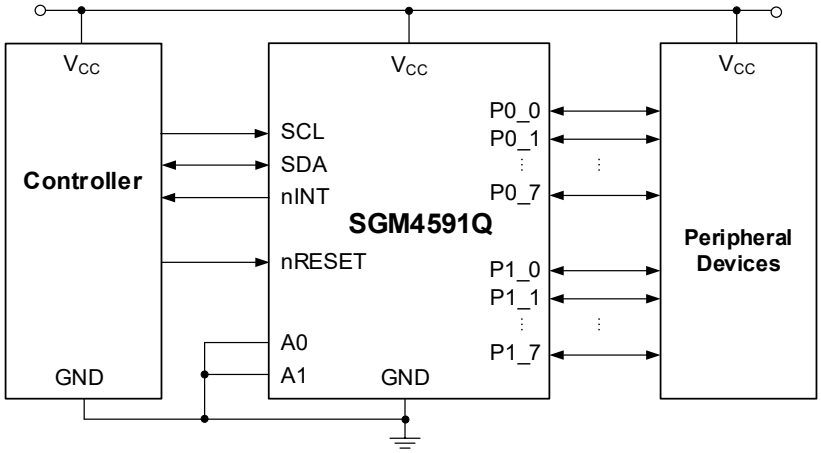


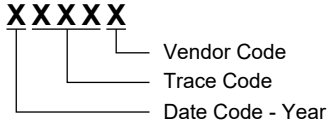

**Figure 1. Typical Application Circuit**

# PACKAGE/ORDERING INFORMATION

| MODEL | PACKAGE DESCRIPTION | SPECIFIED TEMPERATURE RANGE | ORDERING NUMBER | PACKAGE MARKING | PACKING OPTION |
|---|---|---|---|---|---|
| SGM4591Q | TSSOP-24 | -40℃ to +125℃ | SGM4591QTS24G/TR | 0RQTS24G<br>XXXXX | Tape and Reel, 4000 |

## MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.




Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

## ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range, $V_{CC}$ ..... -0.5V to 6V
Input Voltage Range (1), $V_I$ ..... -0.5V to 6V
Output Voltage Range (1), $V_O$ ..... -0.5V to 6V
Input Clamp Current, $I_{IK}$ ($V_I$ < 0V) .....-20mA
Output Clamp Current, $I_{OK}$ ($V_O$ < 0V) .....-20mA
Input-Output Clamp Current, $I_{IOK}$ ($V_O$ < 0V or $V_O$ > $V_{CC}$)
.....±20mA
Continuous Output Low Current, $I_{OL}$ ($V_O$ = 0V to $V_{CC}$) ..50mA
Continuous Output High Current, $I_{OH}$ ($V_O$ = 0V to $V_{CC}$) -50mA
Continuous Current through GND.....-250mA
Continuous Current through $V_{CC}$.....160mA
Package Thermal Resistance
TSSOP-24, $\theta_{JA}$..... 105.8℃/W
TSSOP-24, $\theta_{JB}$..... 73.0℃/W
TSSOP-24, $\theta_{JC}$..... 45.8℃/W
Junction Temperature.....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility (2) (3)
HBM.....±4000V
CDM .....±1000V

NOTES:

1. When the input and output current ratings are observed, the input and I/O negative voltage ratings may be exceeded.

2. For human body model (HBM), all pins comply with AEC-Q100-002 specification.

3. For charged device model (CDM), all pins comply with AEC-Q100-011 specification.

## RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range, $V_{CC}$..... 1.65V to 5.5V
I/O Ports Voltage Range, $V_{I/O}$
SCL, SDA, A0, A1, nRESET, nINT (1) .....-0.5V to 5.5V
For P0_7-0, P1_7-0 Configured as Outputs
.....-0.5V to 5.5V
For P0_7-0, P1_7-0 Configured as Inputs (1)
.....-0.5V to 5.5V
High-Level Input Voltage, $V_{IH}$
SCL, SDA, A0, A1, nRESET, P0_7-0, P1_7-0
..... 0.7 × $V_{CC}$ (MIN)
Low-Level Input Voltage, $V_{IL}$
SCL, SDA, A0, A1, nRESET, P0_7-0, P1_7-0
..... 0.3 × $V_{CC}$ (MAX)
High-Level Output Current, $I_{OH}$ (P0_7-0, P1_7-0)
..... -10mA
Low-Level Output Current, $I_{OL}$ (P0_7-0, P1_7-0)
$T_J$ ≤ +65℃ ..... 25mA
$T_J$ = +85℃ ..... 18mA
$T_J$ = +105℃ ..... 9mA
$T_J$ = +125℃ ..... 4.5mA
$T_J$ = +135℃ ..... 3.5mA
Low-Level Output Current, $I_{OL}$ (nINT, SDA)
$T_J$ ≤ +85℃ ..... 6mA
$T_J$ = +105℃ ..... 3mA
$T_J$ = +125℃ ..... 1.8mA
$T_J$ = +135℃ ..... 1.5mA
Operating Temperature Range..... -40℃ to +125℃

NOTE:
1. Voltages applied above $V_{CC}$ will cause an increase in $I_{CC}$.

## ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

## OVERSTRESS CAUTION

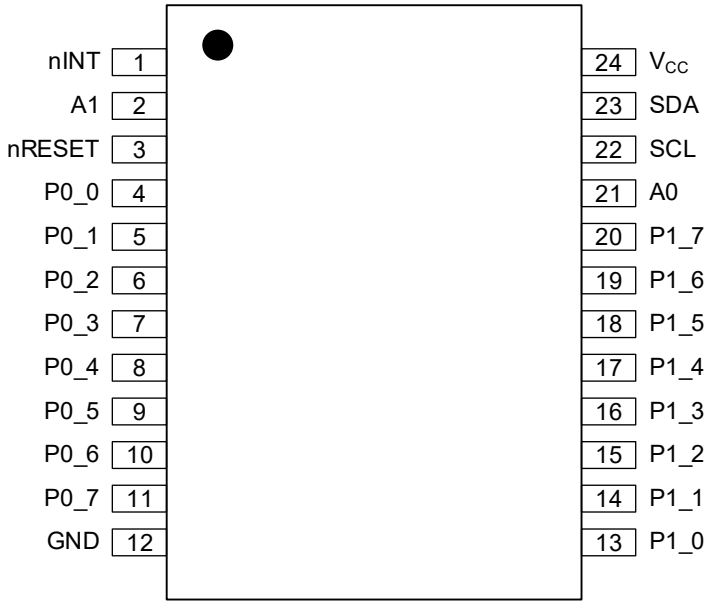
Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

## DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

## PIN CONFIGURATION

(TOP VIEW)




TSSOP-24

## PIN DESCRIPTION

| PIN | NAME | TYPE (1) | DESCRIPTION |
|---|---|---|---|
| 1 | nINT | O | Open-Drain Output. A pull-up resistor is used to connect to $V_{CC}$. |
| 2 | A1 | I | Analog Input A1. Connected to $V_{CC}$ or GND. |
| 3 | nRESET | I | Active Low Reset Input. If there is no active connection, this pin is connected to the $V_{CC}$ pin via a pull-up resistor. |
| 4-11 | P0_0-7 | I/O | P0 to P7 of Port 0 Input/Output. Default as an input at power-on. |
| 12 | GND | — | Ground. |
| 13-20 | P1_0-7 | I/O | P0 to P7 of Port 1 Input/Output. Default as an input at power-on. |
| 21 | A0 | I | Analog Input A0. Connected to $V_{CC}$ or GND. |
| 22 | SCL | I | Clock Signal. |
| 23 | SDA | I/O | Data Signal. |
| 24 | $V_{CC}$ | — | Supply Voltage. |

NOTE: 1. I = Input, O = Output, I/O = Input and Output.

# ELECTRICAL CHARACTERISTICS

(Full = -40℃ to +125℃, all typical values are measured at $T_A$ = +25℃ and $V_{CC}$ = 1.8V, 2.5V, 3.3V or 5V, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| Input Diode Clamp Voltage | $V_{IK}$ | $I_I$ = -18mA, $V_{CC}$ = 1.65V to 5.5V | | | -1.2 | | | V |
| Power-on Reset Voltage on $V_{CC}$ Rising | $V_{PORR}$ | $V_I$ = $V_{CC}$ or GND, $V_{CC}$ = 1.65V to 5.5V | | | | 1.2 | 1.5 | V |
| Power-on Reset Voltage on $V_{CC}$ Falling | $V_{PORF}$ | $V_I$ = $V_{CC}$ or GND, $V_{CC}$ = 1.65V to 5.5V | | | 0.55 | 1.0 | | V |
| P-Port High-Level Output Voltage (1) | $V_{OH}$ | $I_{OH}$ = -8mA | $V_{CC}$ = 1.65V | | 1.20 | | | V |
| | | | $V_{CC}$ = 2.3V | | 1.90 | | | |
| | | | $V_{CC}$ = 3.0V | | 2.65 | | | |
| | | | $V_{CC}$ = 3.6V | | 3.30 | | | |
| | | | $V_{CC}$ = 4.75V | | 4.45 | | | |
| | | $I_{OH}$ = -10mA | $V_{CC}$ = 1.65V | | 1.10 | | | |
| | | | $V_{CC}$ = 2.3V | | 1.80 | | | |
| | | | $V_{CC}$ = 3.0V | | 2.60 | | | |
| | | | $V_{CC}$ = 3.6V | | 3.20 | | | |
| | | | $V_{CC}$ = 4.75V | | 4.35 | | | |
| Low-Level Output Current | $I_{OL}$ | SDA | $V_{CC}$ = 1.65V to 5.5V, $V_{OL}$ = 0.4V | | 3 | | | mA |
| | | P-Port (2) | $V_{CC}$ = 1.65V to 5.5V, $V_{OL}$ = 0.5V | | 8 | | | |
| | | | $V_{CC}$ = 1.65V to 5.5V, $V_{OL}$ = 0.7V | | 10 | | | |
| | | nINT | $V_{CC}$ = 1.65V to 5.5V, $V_{OL}$ = 0.4V | | 10 | | | |
| Input Leakage Current | $I_I$ | SCL, SDA | $V_I$ = $V_{CC}$ or GND, $V_{CC}$ = 1.65V to 5.5V | | | | ±1 | μA |
| | | A0, A1, nRESET | | | | | ±1 | |
| High-Level Input Current | $I_{IH}$ | P-Port | $V_I$ = $V_{CC}$, $V_{CC}$ = 1.65V to 5.5V | | | | 1 | μA |
| Low-Level Input Current | $I_{IL}$ | P-Port | $V_I$ = GND, $V_{CC}$ = 1.65V to 5.5V | | | | -1 | |
| Quiescent Supply Current | $I_{CC}$ | Operating Mode | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0A, I/O = inputs, $f_{SCL}$ = 400kHz, no load | $V_{CC}$ = 5.5V | | 25.8 | 40 | μA |
| | | | | $V_{CC}$ = 3.6V | | 14.0 | 30 | |
| | | | | $V_{CC}$ = 2.7V | | 9.5 | 18 | |
| | | | | $V_{CC}$ = 1.95V | | 6.5 | 11 | |
| | | Standby Mode | $V_I$ = $V_{CC}$, $I_O$ = 0A, I/O = inputs, $f_{SCL}$ = 0kHz, no load | $V_{CC}$ = 5.5V | | 5.0 | 15 | |
| | | | | $V_{CC}$ = 3.6V | | 2.5 | 8 | |
| | | | | $V_{CC}$ = 2.7V | | 1.5 | 5 | |
| | | | | $V_{CC}$ = 1.95V | | 0.9 | 3.5 | |
| | | | $V_I$ = GND, $I_O$ = 0A, I/O = inputs, $f_{SCL}$ = 0kHz, no load | $V_{CC}$ = 5.5V | | 5.0 | 15 | |
| | | | | $V_{CC}$ = 3.6V | | 2.5 | 8 | |
| | | | | $V_{CC}$ = 2.7V | | 1.5 | 5 | |
| | | | | $V_{CC}$ = 1.95V | | 0.9 | 3.5 | |
| Input Capacitance | $C_I$ | SCL | $V_I$ = $V_{CC}$ or GND | $V_{CC}$ = 1.65V to 5.5V | | 6 | | pF |
| Input/Output Capacitance | $C_{I/O}$ | SDA | $V_{I/O}$ = $V_{CC}$ or GND | $V_{CC}$ = 1.65V to 5.5V | | 7.5 | | pF |
| | | P-Port | | | | 9.5 | | |

NOTES:

1. Each octal (P0_7-0 and P1_7-0) has a limitation to the maximum allowed $I_{OL}$(100mA) externally and a total of 200mA for a device at $T_J$ ≤ +85℃.

2. The maximum total sourced current by all I/Os must be less than 160mA.

## I²C INTERFACE TIMING REQUIREMENTS

($T_A$ = -40℃ to +125℃, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN (1) | TYP | MAX (1) | UNITS |
|---|---|---|---|---|---|---|
| **I²C Bus—Standard Mode** | | | | | | |
| Clock Frequency | $f_{SCL}$ | | 0 | | 100 | kHz |
| Clock High Time | $t_{SCH}$ | | 4 | | | μs |
| Clock Low Time | $t_{SCL}$ | | 4.7 | | | μs |
| Spike Time | $t_{SP}$ | | | | 50 | ns |
| Serial-Data Setup Time | $t_{SU\_DAT}$ | | 250 | | | ns |
| Serial-Data Hold Time | $t_{HD\_DAT}$ | | 0 | | | ns |
| Input Rise Time | $t_{IR}$ | | | | 1000 | ns |
| Input Fall Time | $t_{IF}$ | | | | 300 | ns |
| Output Fall Time | $t_{OF}$ | 10pF to 400pF bus | | | 300 | ns |
| Bus Free Time between Stop and Start | $t_{BUF}$ | | 4.7 | | | μs |
| Setup Time for Start or Repeated Start Condition | $t_{STS}$ | | 4.7 | | | μs |
| Hold Time for Start or Repeated Start Condition | $t_{STH}$ | | 4 | | | μs |
| Setup Time for Stop Condition | $t_{SPS}$ | | 4 | | | μs |
| Valid Data Time | $t_{VD\_DAT}$ | SCL low to SDA output valid | | | 3.45 | μs |
| Valid Data Time of ACK Condition | $t_{VD\_ACK}$ | ACK signal from SCL low to SDA (out) low | | | 3.45 | μs |
| Bus Capacitive Load | $C_B$ | | | | 400 | pF |
| **I²C Bus—Fast Mode** | | | | | | |
| Clock Frequency | $f_{SCL}$ | | 0 | | 400 | kHz |
| Clock High Time | $t_{SCH}$ | | 0.6 | | | μs |
| Clock Low Time | $t_{SCL}$ | | 1.3 | | | μs |
| Spike Time | $t_{SP}$ | | | | 50 | ns |
| Serial-Data Setup Time | $t_{SU\_DAT}$ | | 100 | | | ns |
| Serial-Data Hold Time | $t_{HD\_DAT}$ | | 0 | | | ns |
| Input Rise Time | $t_{IR}$ | | 20 | | 300 | ns |
| Input Fall Time | $t_{IF}$ | | 20 × ($V_{CC}$/5.5V) | | 300 | ns |
| Output Fall Time | $t_{OF}$ | 10pF to 400pF bus | 20 × ($V_{CC}$/5.5V) | | 300 | ns |
| Bus Free Time between Stop and Start | $t_{BUF}$ | | 1.3 | | | μs |
| Setup Time for Start or Repeated Start Condition | $t_{STS}$ | | 0.6 | | | μs |
| Hold Time for Start or Repeated Start Condition | $t_{STH}$ | | 0.6 | | | μs |
| Setup Time for Stop Condition | $t_{SPS}$ | | 0.6 | | | μs |
| Valid Data Time | $t_{VD\_DAT}$ | SCL low to SDA output valid | | | 0.9 | μs |
| Valid Data Time of ACK Condition | $t_{VD\_ACK}$ | ACK signal from SCL low to SDA (out) low | | | 0.9 | μs |
| Bus Capacitive Load | $C_B$ | | | | 400 | pF |

NOTE: 1. Specified by design and characterization, not production tested.

## nRESET TIMING REQUIREMENTS

($T_A$ = -40℃ to +125℃, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Reset Pulse Duration (1) | $t_W$ | | 6 | | | ns |
| Reset Recovery Time (1) | $t_{REC}$ | | 0 | | | ns |
| Time to Reset | $t_{RESET}$ | $V_{CC}$ = 2.3V to 5.5V | 450 | | | ns |
| | | $V_{CC}$ = 1.65V to 2.3V | 550 | | | |

## SWITCHING CHARACTERISTICS

($T_A$ = -40℃ to +125℃, $C_L$ ≤ 100pF, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Interrupt Valid Time | $t_{IV}$ | From P-Port to nINT | | | | 4 | μs |
| Interrupt Reset Delay Time | $t_{IR}$ | From SCL to nINT | | | | 4 | μs |
| Data Output Valid Time | $t_{DV}$ | From SCL to P-Port | $V_{CC}$ = 2.3V to 5.5V | | | 200 | ns |
| | | | $V_{CC}$ = 1.65V to 2.3V | | | 300 | ns |
| Data Input Setup Time (1) | $t_{DSU}$ | From P-Port to SCL | | 2 | | | CLK |
| Data Input Hold Time (1) | $t_{DH}$ | From P-Port to SCL | | 1 | | | μs |

NOTE: 1. Specified by design and characterization, not production tested.

## TEST CIRCUIT

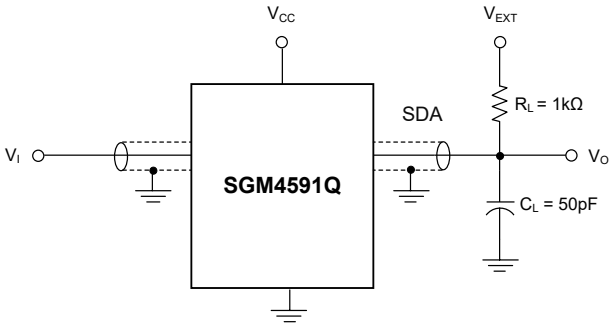
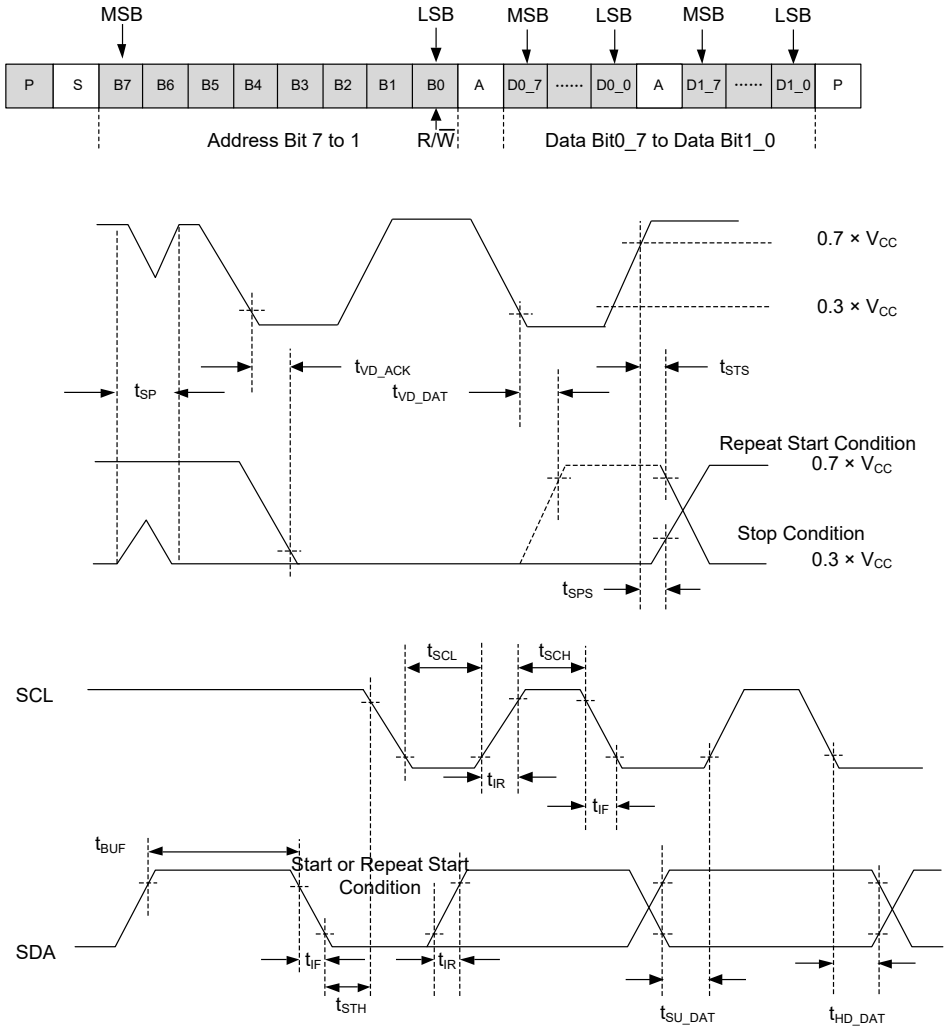



**Figure 2. I²C Interface Load Circuit**

NOTES:

1. $R_L$ refers to load resistance. $C_L$ refers to load capacitance (includes jig and probe).
2. All inputs are supplied by generators featured by: PRR ≤ 10MHz, $Z_O$ = 50Ω, $t_R/t_F$ ≤ 30ns.

## WAVEFORMS




| Byte | Description |
|---|---|
| 1 | I²C address |
| 2, 3 | P-port data |

**Figure 3. I²C Interface Voltage Waveforms**

## TEST CIRCUIT (continued)

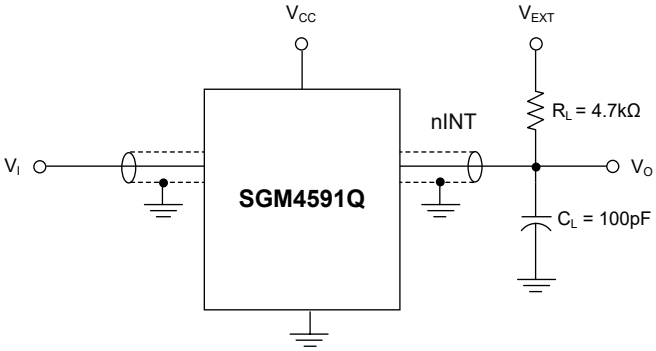



**Figure 4. Interrupt Load Circuit**

NOTES:

1. $R_L$ refers to load resistance. $C_L$ refers to load capacitance (includes jig and probe).
2. All inputs are supplied by generators featured by: PRR ≤ 10MHz, $Z_O$ = 50Ω, $t_R/t_F$ ≤ 30ns.

## WAVEFORMS

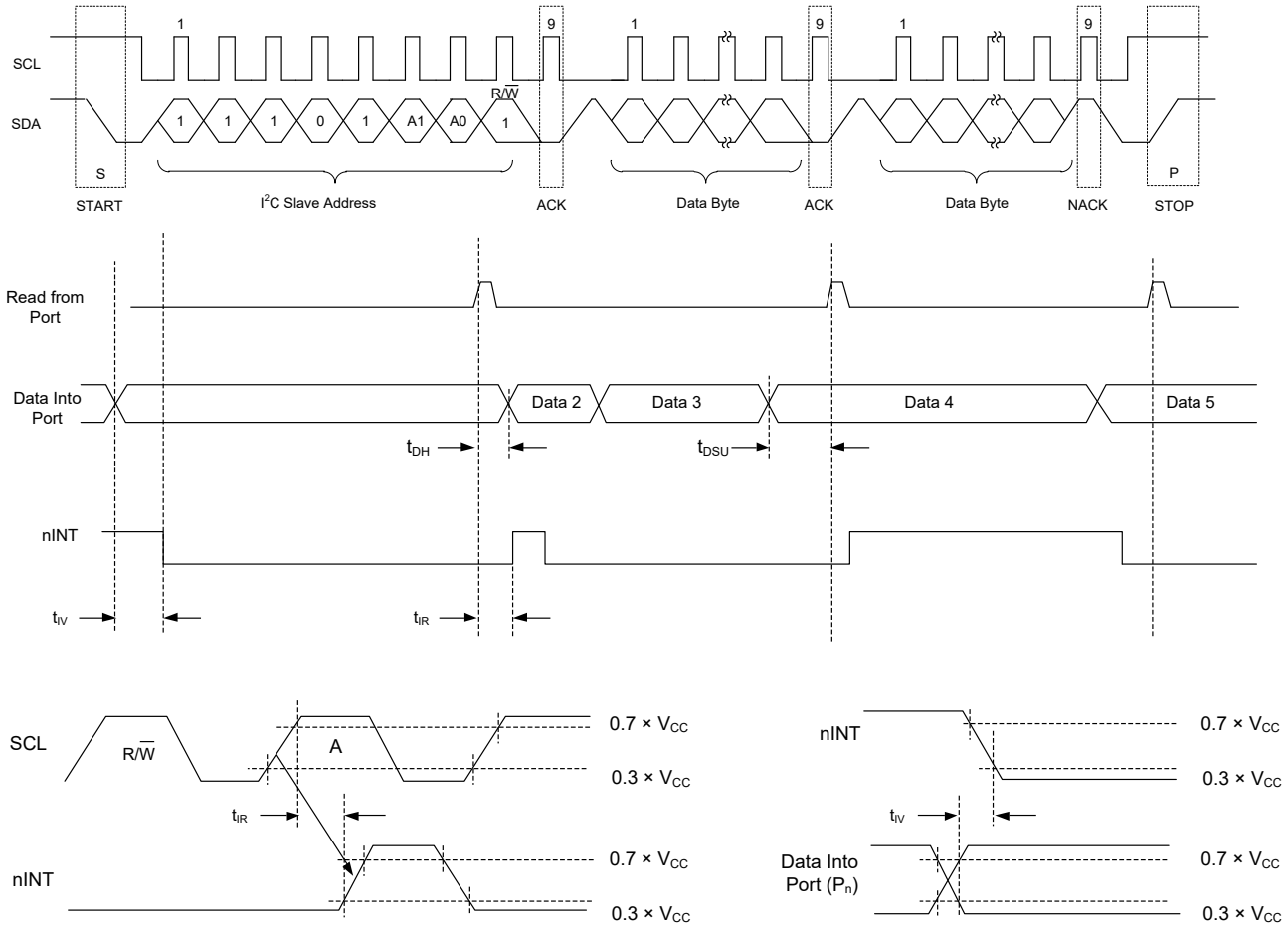






**Figure 5. Interrupt Voltage Waveforms**

## TEST CIRCUIT (continued)

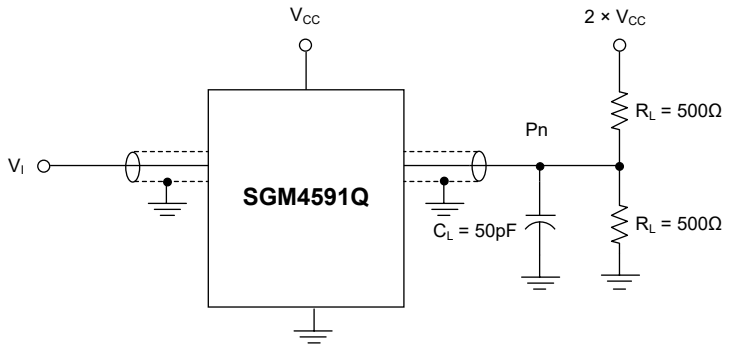



**Figure 6. P-Port Load Circuit**

NOTES:
1. $R_L$ refers to load resistance. $C_L$ refers to load capacitance (includes jig and probe).
2. All inputs are supplied by generators featured by: PRR ≤ 10MHz, $Z_O$ = 50Ω, $t_R/t_F$ ≤ 30ns.
3. $t_{DV}$ is measured from 0.7 × $V_{CC}$ on SCL to 50% I/O ($P_n$) output.
4. The outputs are measured one by one with a transition every measurement.

## WAVEFORMS

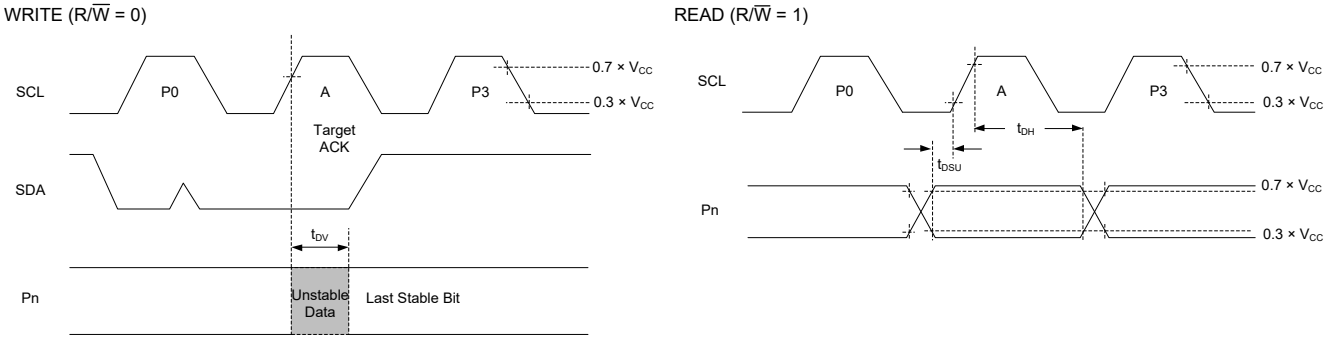



**Figure 7. P-Port Voltage Waveforms**

## TEST CIRCUIT (continued)

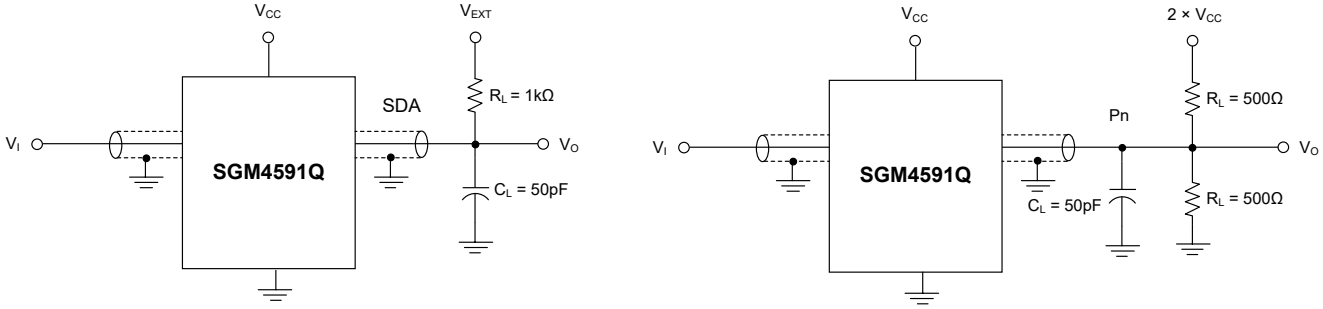



**Figure 8. Reset Load Circuits**

NOTES:

1. $R_L$ refers to load resistance. $C_L$ refers to load capacitance (includes jig and probe).
2. All inputs are supplied by generators featured by: PRR ≤ 10MHz, $Z_O$ = 50Ω, $t_r/t_f$ ≤ 30ns.
3. I/Os are designed as inputs.
4. The outputs are measured one by one with a transition every measurement.

## WAVEFORMS

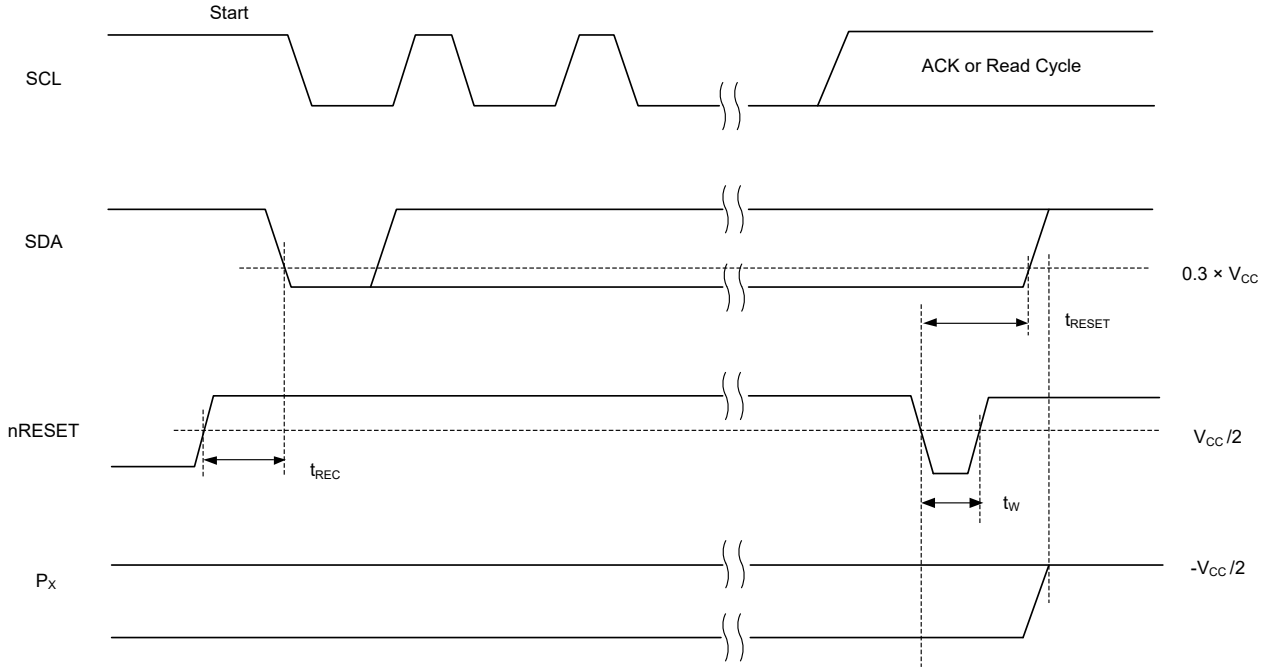
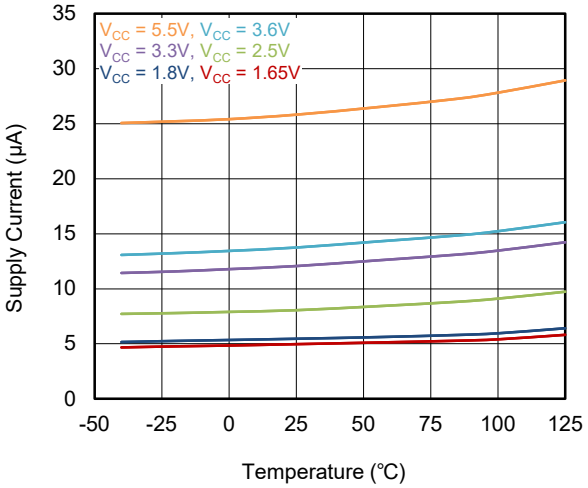



**Figure 9. Reset Load Circuits and Voltage Waveforms**

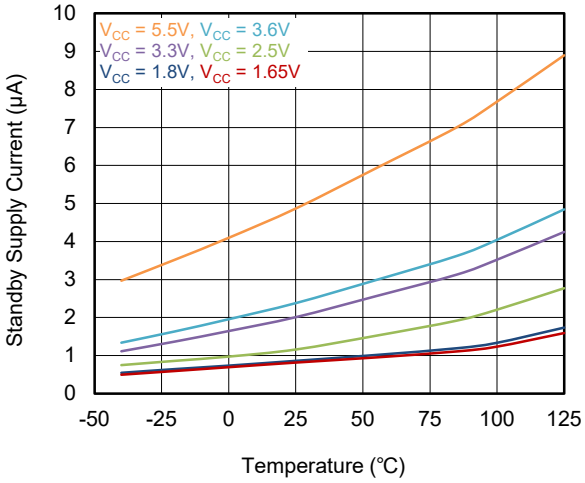
## TYPICAL PERFORMANCE CHARACTERISTICS

$T_A$ = +25℃, unless otherwise noted.

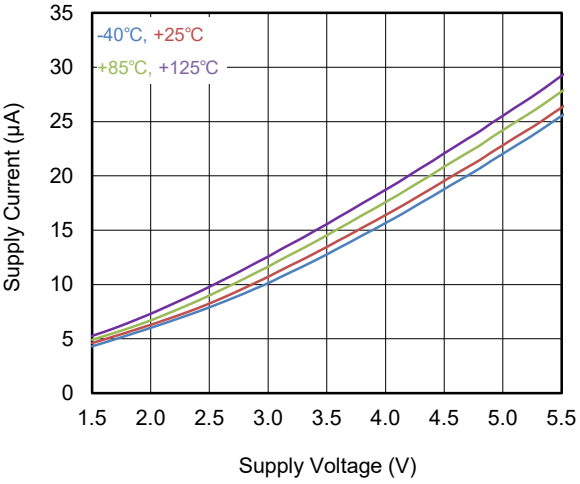
Supply Current vs. Temperature



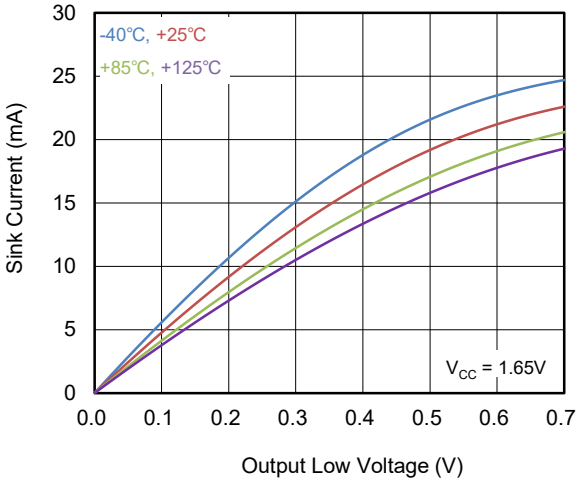

Standby Supply Current vs. Temperature



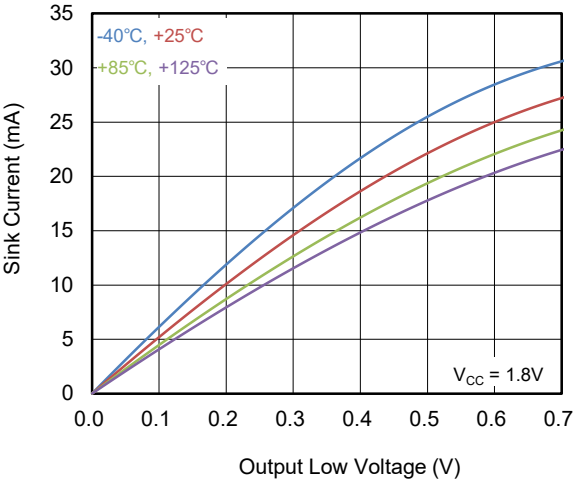

Supply Current vs. Supply Voltage



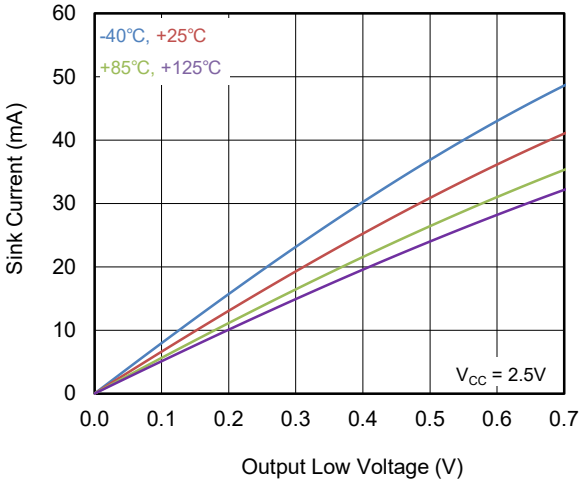

Sink Current vs. Output Low Voltage




Sink Current vs. Output Low Voltage



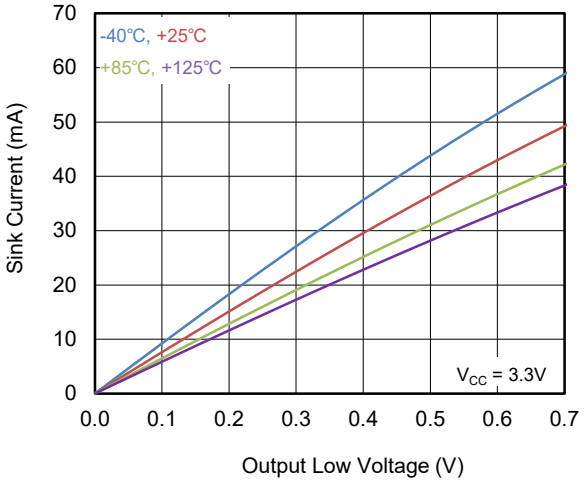

Sink Current vs. Output Low Voltage



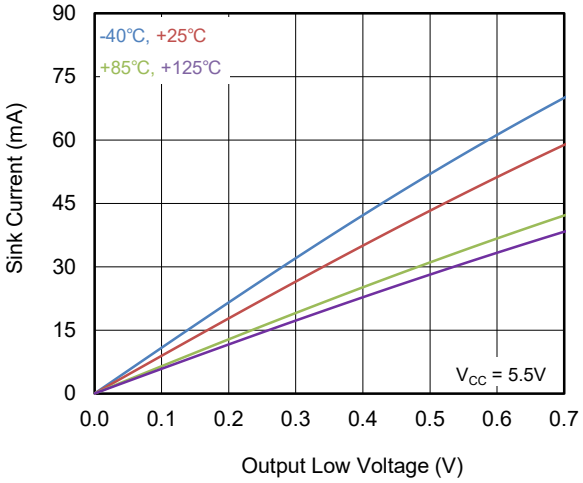
## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$T_A$ = +25℃, unless otherwise noted.

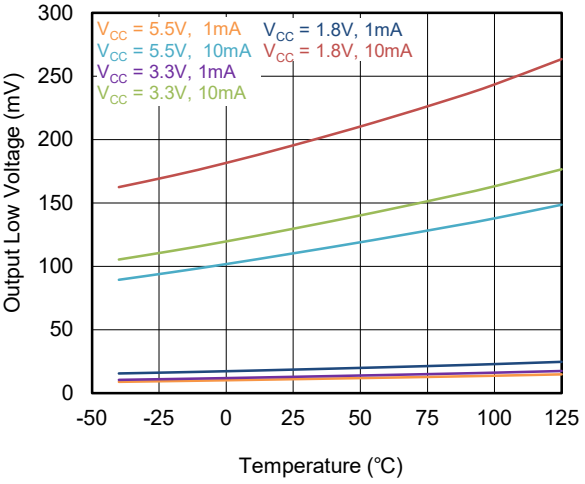
Sink Current vs. Output Low Voltage



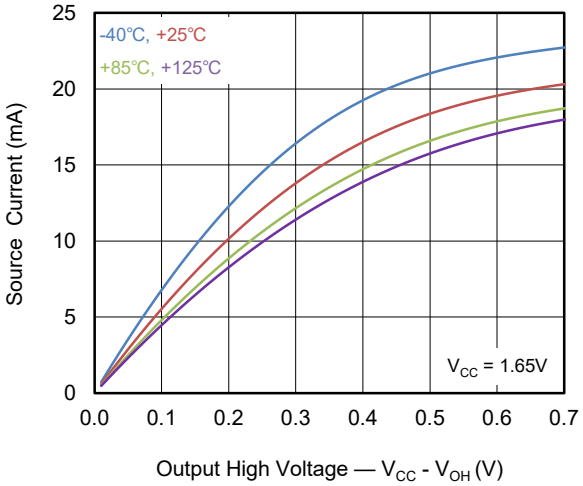

Sink Current vs. Output Low Voltage



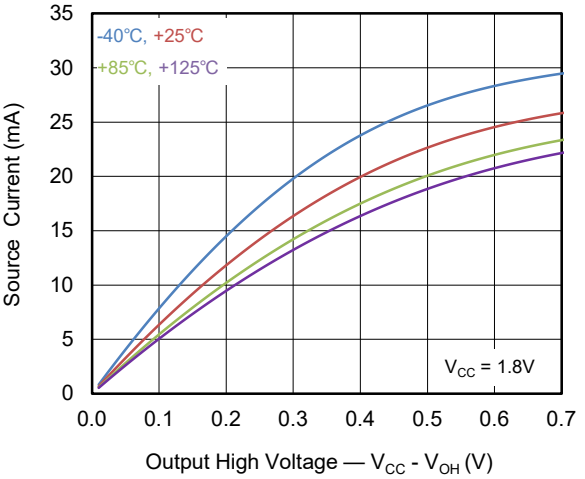

Output Low Voltage vs. Temperature



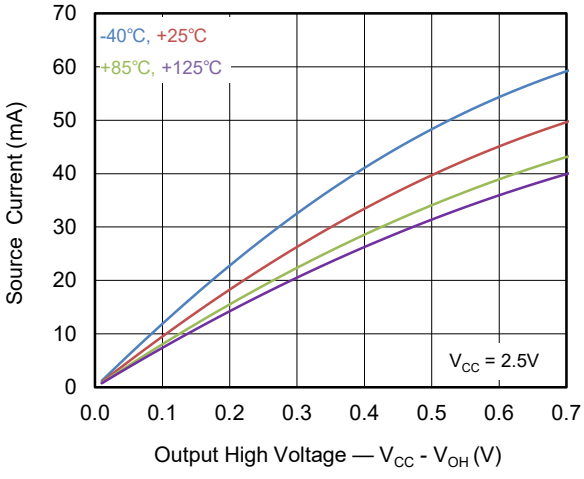

Source Current vs. Output High Voltage — $V_{CC}$ - $V_{OH}$




Source Current vs. Output High Voltage — $V_{CC}$ - $V_{OH}$



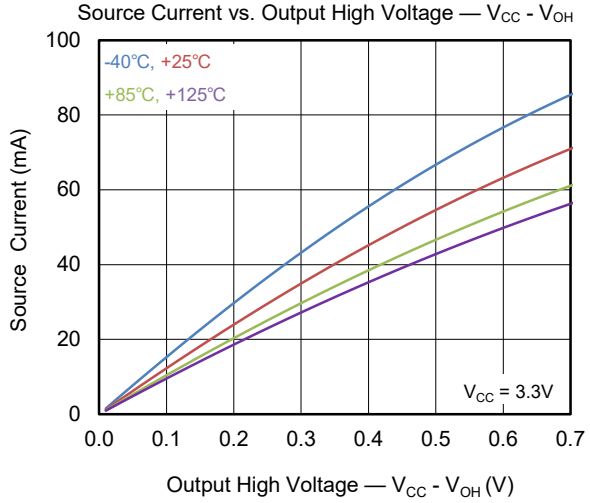

Source Current vs. Output High Voltage — $V_{CC}$ - $V_{OH}$



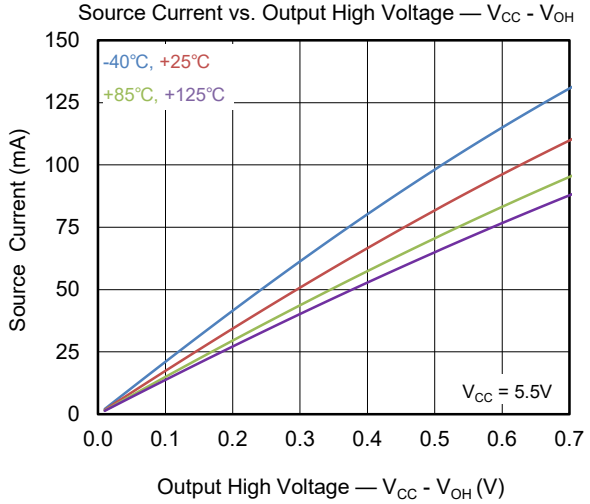
## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$T_A$ = +25℃, unless otherwise noted.

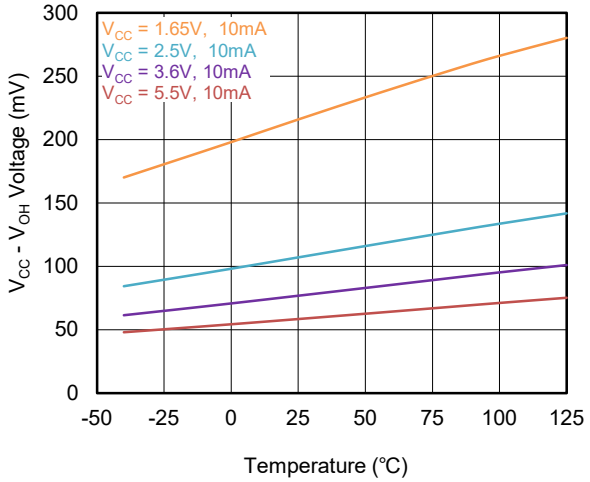
Source Current vs. Output High Voltage — $V_{CC}$ - $V_{OH}$



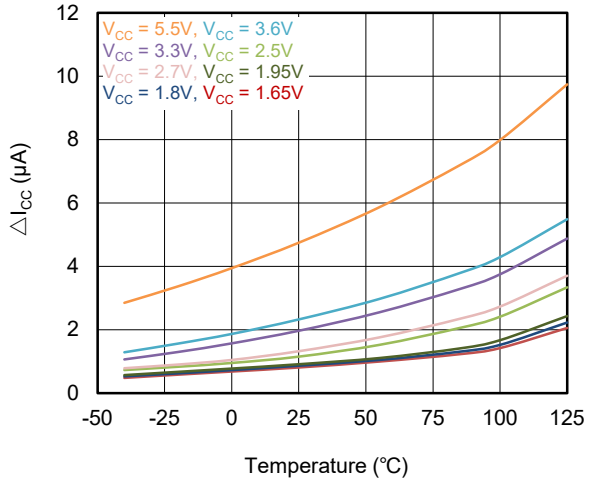

Source Current vs. Output High Voltage — $V_{CC}$ - $V_{OH}$



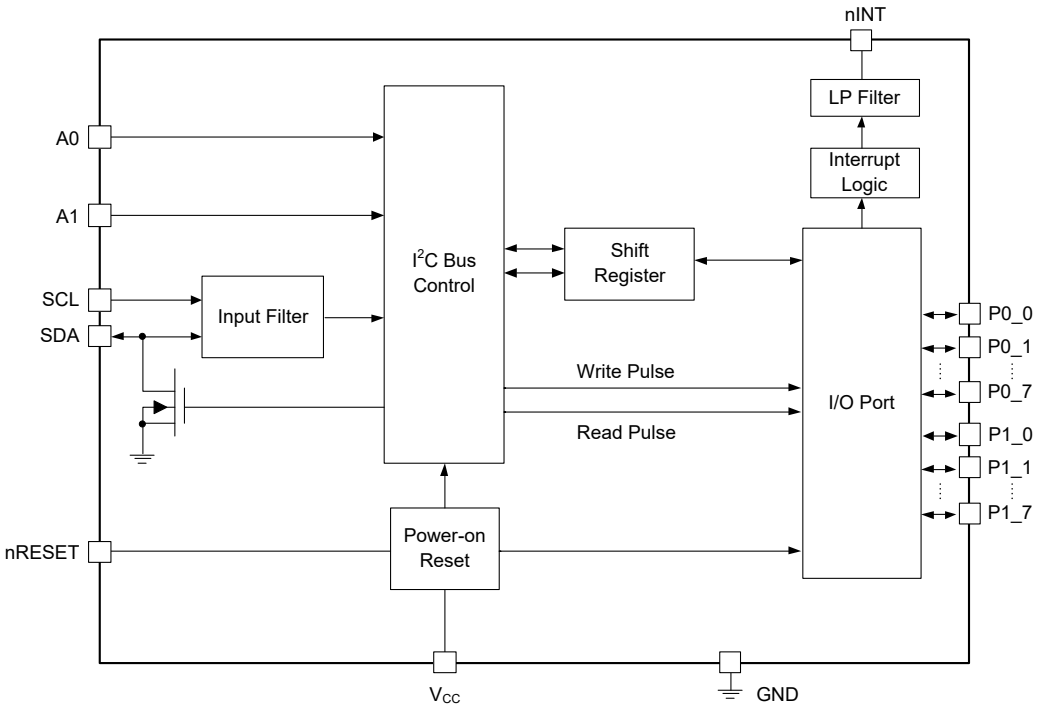

$V_{CC}$ - $V_{OH}$ Voltage vs. Temperature




$\triangle I_{CC}$ vs. Temperature

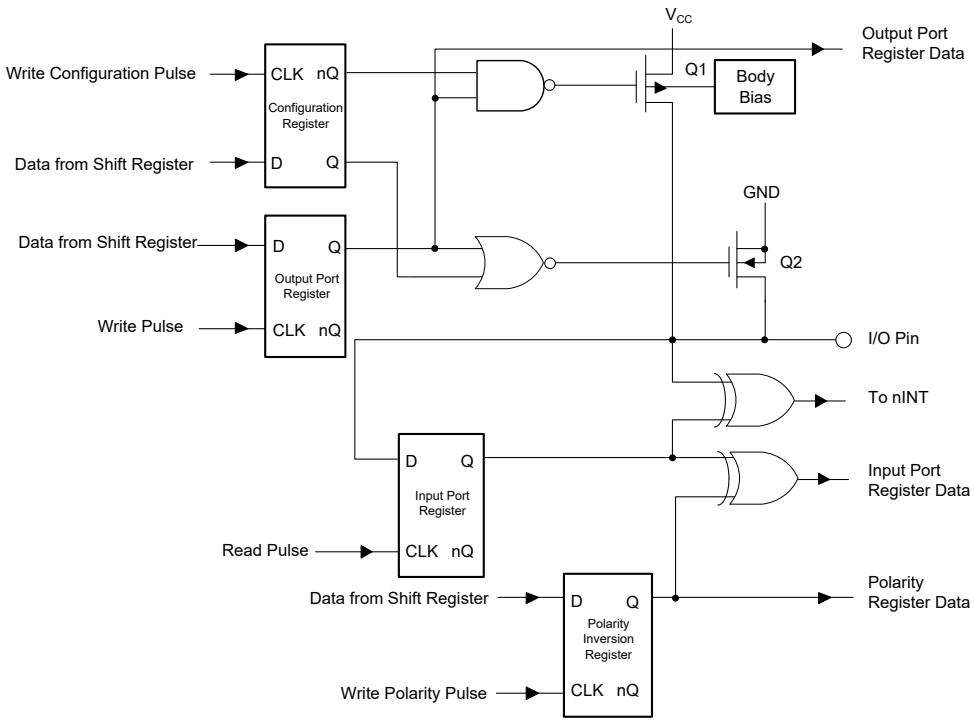


## FUNCTIONAL BLOCK DIAGRAM




NOTE: All I/Os are set as inputs when reset.

**Figure 10. Functional Block Diagram (Positive Logic)**




NOTE: At power-on reset, all registers return to default values.

**Figure 11. Simplified Schematic of P-Port Inputs or Outputs**

# DETAILED DESCRIPTION

## Overview

The SGM4591Q is a multi-use parallel I/O expander device, which consists of two lanes, 8 bits parallel I/O expansion. It communicates with processor through two-line bidirectional $I^2C$ bus (or SMBus).

The SGM4591Q has two groups of 8-bit registers, including Input Port x (x = 0, 1), Output Port x, Polarity Inversion x, Configuration Port x, Output Mode Configuration x, and Output Anomaly Port x. When the device is powered on, all ports are designed as inputs. Writing to the register Configuration Port x could set the corresponding ports as input or output. Writing '1' to the Polarity Inversion x register can invert the polarity of the input register. The register Output Mode Configuration x can configure ports as push-pull or open-drain when the corresponding ports are set as output mode. And the Output Anomaly Port x can be enabled to indicate the situation of output short-circuit. All registers can be read by the processor.

By setting the nRESET input low, the processor can reset the SGM4591Q when a timeout or other improper operation occurs. The power-on reset can initialize the $I^2C$ state machine, and reset all registers. Putting nRESET low could also perform the same reset operation without repowering the device.

Any input state differing from its corresponding Input Port x register can cause the open-drain interrupt (nINT) activation. If the Output Anomaly Port x is enabled, in the situation that the output state differs from its corresponding Output Port register, the nINT output is also activated. It is used to indicate an output anomaly to the processor.

The SGM4591Q can remain a simple target device. The nINT can be connected to the input of a processor, the remote I/O can inform the processor whether there is incoming data changing or an output anomaly without $I^2C$ bus.

The SGM4591Q may select device address by the A0 and A1 pins and allow up to four devices to share the same $I^2C$ or SMBus.

## Feature Description

### I/O Ports

The I/Os would be in high-impedance state when configured as an input because FETs Q1 and Q2 are off. The input voltage may be raised above $V_{CC}$ to a maximum of 5.5V.

When the I/Os are designed as an output, the state of Output Port x decides whether Q1 or Q2 to be enabled. In this case, the low-impedance paths exist between the ports pin and either $V_{CC}$ or GND. For proper operation, the external voltage applied to this port pin must not exceed the recommended voltage. The output mode can be set as push-pull or open-drain via the Output Mode Configuration x register.

### nRESET Input

Holding the nRESET pin low for a minimum of $t_W$ can cause a reset. $I^2C$ state machine is reset and all registers are held in their default values until nRESET is high once again. The input needs to be high via a pull-up resistor when there is no active connection.

### Interrupt (nINT) Output

Any change of the state of port pins can generate an interrupt in the input mode. It also can be generated when output anomaly occurs and the nINT indicator function is enabled in the output mode. The actual pin value can be read from the Input Port registers. Therefore, the abnormal output bits can be identified.

The nINT signal becomes valid after the interrupt valid time ($t_{IV}$). The nINT would be reset when the state of port pins changes to the original setting or the corresponding Input Port x register is read. In the read mode, the resetting occurs at the acknowledge (ACK) bit after the rising edge of SCL signal. Pay attention to that the nINT is reset at the ACK before sending the changed data bytes. Interrupt that occurs during the ACK clock pulse may be lost (or be very short) due to resetting of interrupt during this pulse. After resetting, each change of the port pin in the input mode would be detected and transmitted as nINT.

There is no effect on the interrupt circuit when operating a read or a write to another device. If the state of a port pin is not consistent with the content of the corresponding Input Port x register, a false interrupt may occur when changing an I/O port from an output state to an input state. Due to that each 8-bit port is read independently, when port 0 causes an interrupt, it will not be cleared by reading port 1, or vice versa.

nINT needs a pull-up resistor to $V_{CC}$ due to the open-drain structure.

# DETAILED DESCRIPTION (continued)

## Function Mode

### Power-on Reset (POR)

During power-on, the POR function keeps the SGM4591Q in a reset state until $V_{CC}$ reaches $V_{PORR}$. Then, the SGM4591Q would release the reset condition and initialize its register to the default state. After that, $V_{CC}$ must be lowered to $V_{PORF}$ and then backs to the operating voltage for a power-reset cycle.

## Programming

### I²C Interface

The SGM4591Q has a standard bidirectional I²C interface that may be controlled by a processor that can configure or read the state of this device. The SGM4591Q has a specific device address to distinguish it from other targets on the same I²C bus.

I²C is a well-known 2-wire serial communication interface that can connect one (or more) master device(s) to some slave devices for two-way communication. The bus lines are named serial data (SDA) and serial clock (SCL). The device that initiates a data transfer is a master. A master generates the SCL signal. Slave devices have unique addresses to identify. A master is typically a micro controller or a digital signal processor. Bus lines are pulled high by weak current source or pull-up resistors and in logic high state with no clocking when the bus is idle. The SDA and SCL pins are open-drain. Data transfer can only begin when the bus is idle. When both the SDA and SCL lines are high after the stop condition, the bus is considered idle.

Figure 12 and Figure 13 show the general processor for a processor accessing a target device:

1. Send data to target:
- Controller-transmitter sends a START signal and device address to the target receiver.
- Controller-transmitter sends data to target receiver.
- Controller-transmitter sends a STOP signal to terminate this transfer.

2. Receive data from target:
- Controller-receiver sends a START signal and device address to the target transmitter.
- Controller-receiver sends the relevant register address to the target transmitter.
- Controller-receiver receives data from the target transmitter.
- Controller-receiver sends a STOP signal to terminate this transfer.

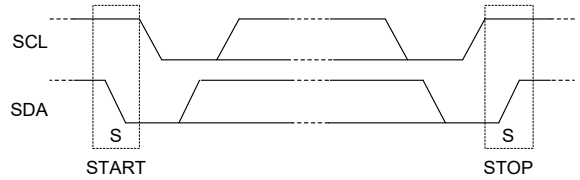



**Figure 12. I²C Bus in START and STOP Conditions**

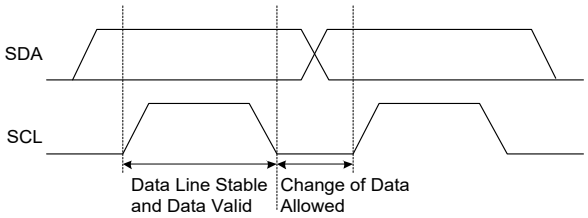



**Figure 13. Bit Transfer**

The interface definition is illustrated in Table 1.

**Table 1. Interface Definition**

| Byte | Bits | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 (MSB) | D6 | D5 | D4 | D3 | D2 | D1 | D0 (LSB) |
| I²C Target Address | 1 | 1 | 1 | 0 | 1 | A1 | A0 | R/$\overline{W}$ |
| P0_x I/O Data Bus | P0_7 | P0_6 | P0_5 | P0_4 | P0_3 | P0_2 | P0_1 | P0_0 |
| P1_x I/O Data Bus | P1_7 | P1_6 | P1_5 | P1_4 | P1_3 | P1_2 | P1_1 | P1_0 |

# DETAILED DESCRIPTION (continued)

## Bus Transactions

The controller and the SGM4591Q can finish data transactions through R/$\overline{W}$ commands.

Registers are located in the memory of target containing information, no matter what it is the configuration information or some sampled data sent to the controller. The controller instructs the SGM4591Q to perform some tasks through writing information to these registers.

**WRITE:** The controller sends a START condition accompanied by the address of target, and the last bit is written as '0', which indicates a 'write' command. After receiving the ACK signal, the controller sends the register address. The SGM4591Q sends the ACK signal again, indicating it is ready. Then, the controller starts transmitting the register data to the target until the controller has sent all the necessary data. The controller could send a STOP condition to terminate the transmission.

See the **Control Register and Command Byte** section for more details. Figure 14 indicates the write of a single byte to a target register.

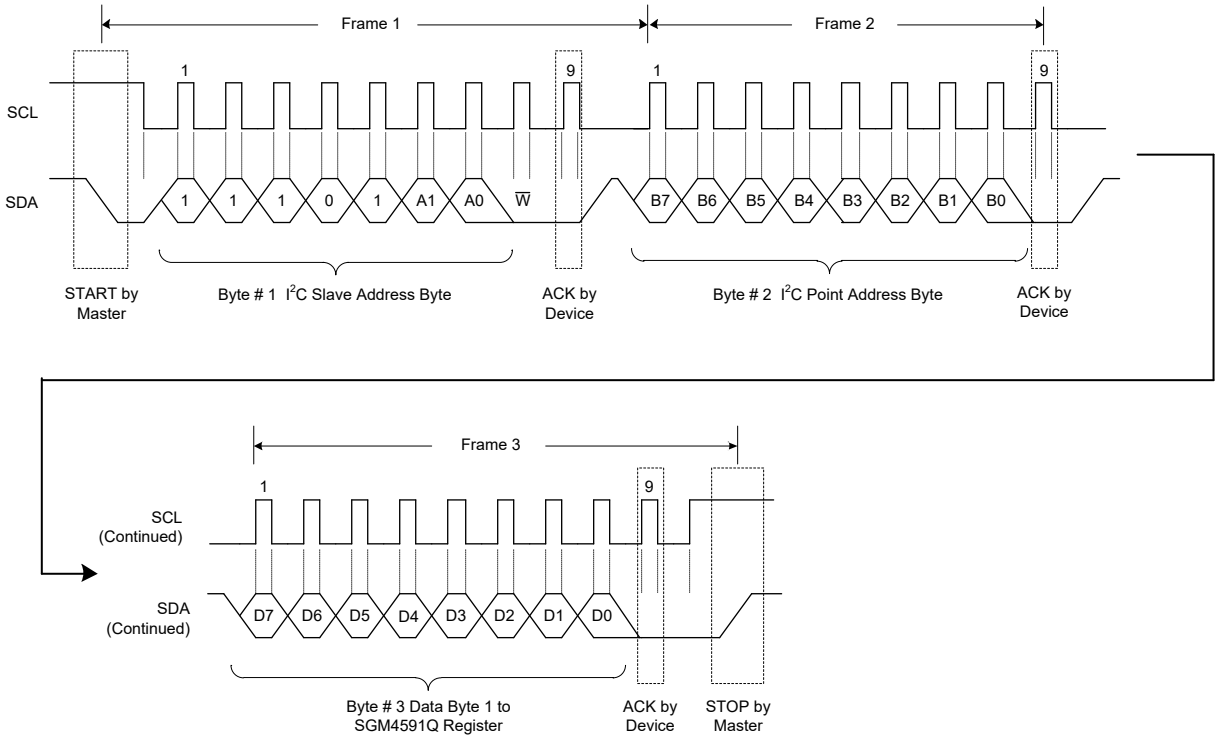



**Figure 14. Write to Register**

## DETAILED DESCRIPTION (continued)

Figure 15 indicates the write to the Polarity Inversion register.

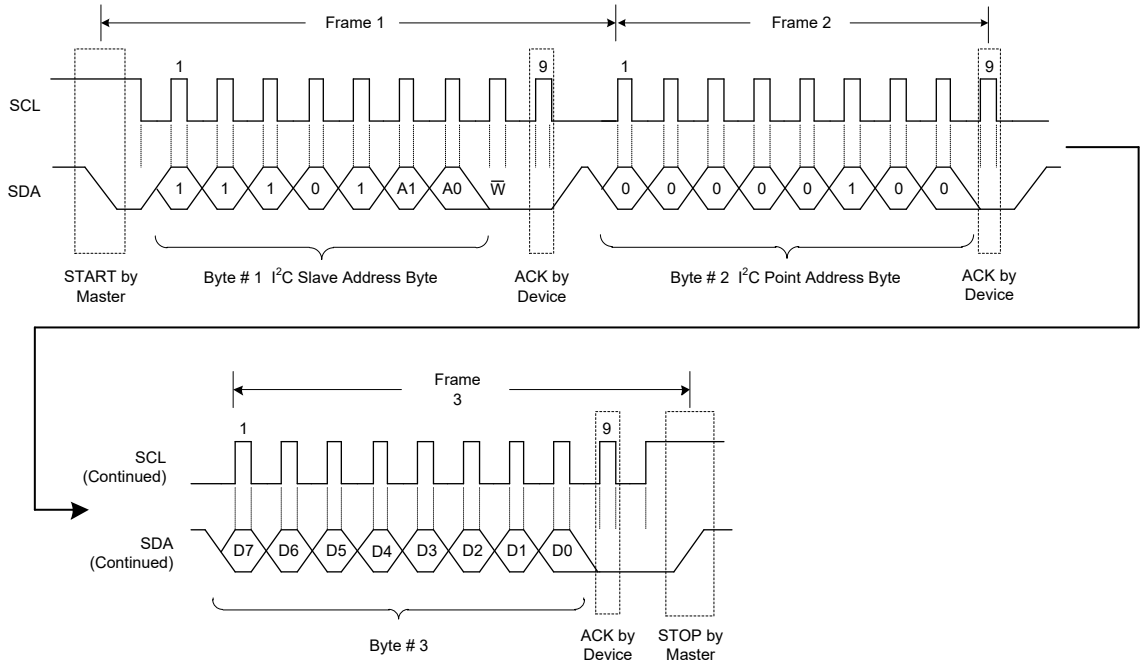



**Figure 15. Write to the Polarity Inversion Port 0 Register**

Figure 16 indicates the write to Output Port register.

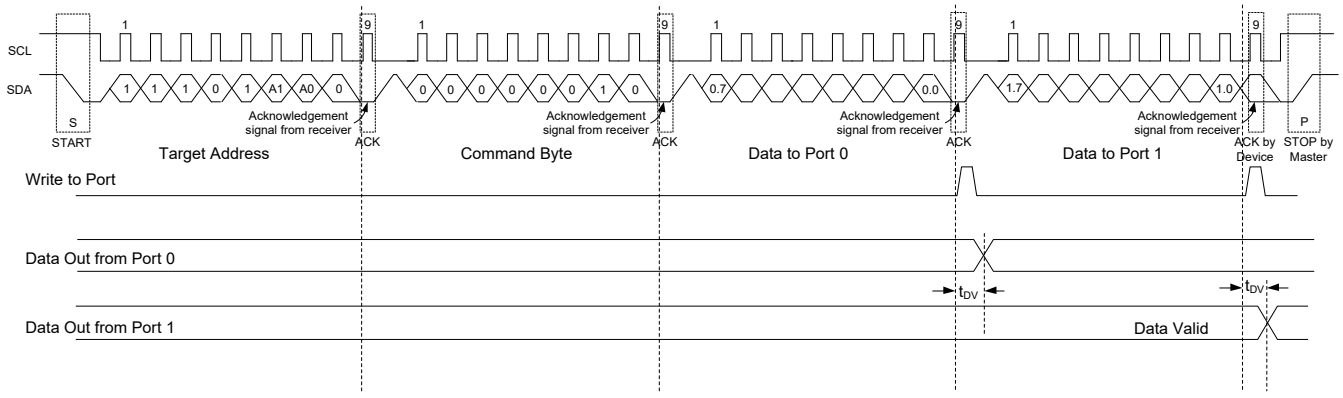



**Figure 16. Write to Output Port 0 Register**

## DETAILED DESCRIPTION (continued)

**READ:** 'Read' command is similar to 'write' command, but needs a few extra steps. Reading from a target requests that the controller must firstly give the target an instruction about which register it wants to read from. This step is consistent with 'write', and the last bit is written '0' (indicating a 'write'), followed by the register it wants to read from. After receiving the ACK signal, the controller sends a START again with the last bit written '1' (indicating a 'read'). Then, the SGM4591Q sends the ACK signal again, indicating it is ready. And the controller releases the SDA but still supplies the clock signal to the target. In this transaction, the controller becomes the receiver of data, and the SGM4591Q becomes the transmitter.

The controller continues to supply the clock signal but releases the SDA so that the target can transmit data. The controller must send an ACK to the target at the end of every byte of data so that the target could send more data. The controller receives the number of bytes as expected, then it sends an NACK to the target to stop data transaction and release the SDA bus. After this, the controller sends a STOP condition.

If the command byte is not set through a write first, and a read is needed by the controller, the device NACKs until a command byte register address is set as described above.

See the **Control Register and Command Byte** section for more details. Figure 17 indicates the reading of a single byte from a target register.

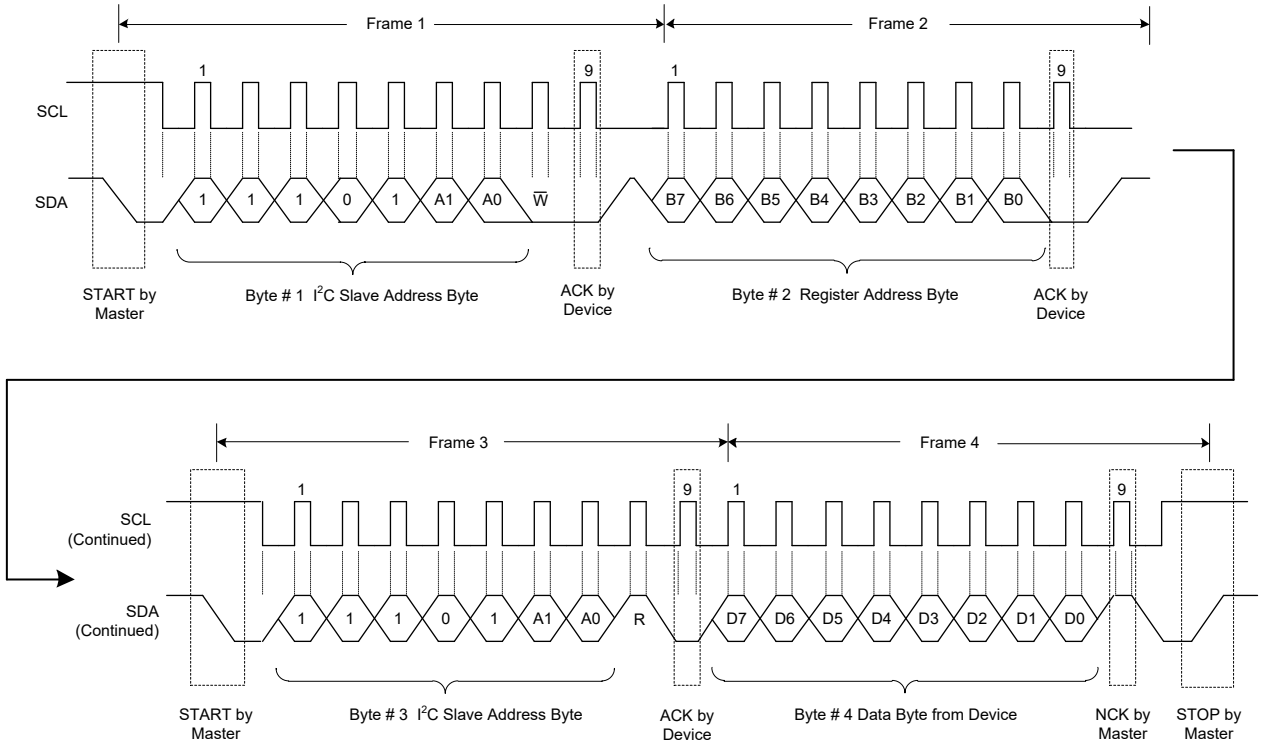
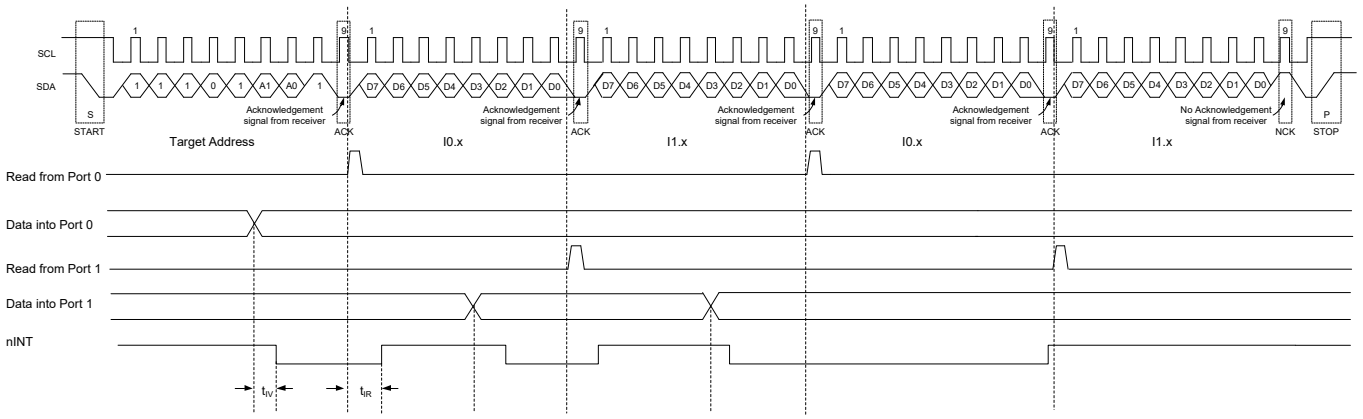



**Figure 17. Read from Register**

After a single write request to a register, a repeated start signal occurs, then the requested register is used for the read request. Note that when reading multiple bytes, the data is clocked into the register on the rising edge of the ACK signal pulse before data is transferred. After reading the first byte, other bytes may also be read. However, the current data just reflects the information in the other register of the pair. For instance, if Input Port 0 is read, Input Port1 is read next. During read operation, if a RESTART occurs, the data may be lost due to that the internal register has already been changed to the other register of the pair.

## DETAILED DESCRIPTION (continued)

The number of received data bytes in one read transmission has no limitation, but the controller must not acknowledge the data when the final byte is received. Figure 18 and Figure 19 show two different scenarios.

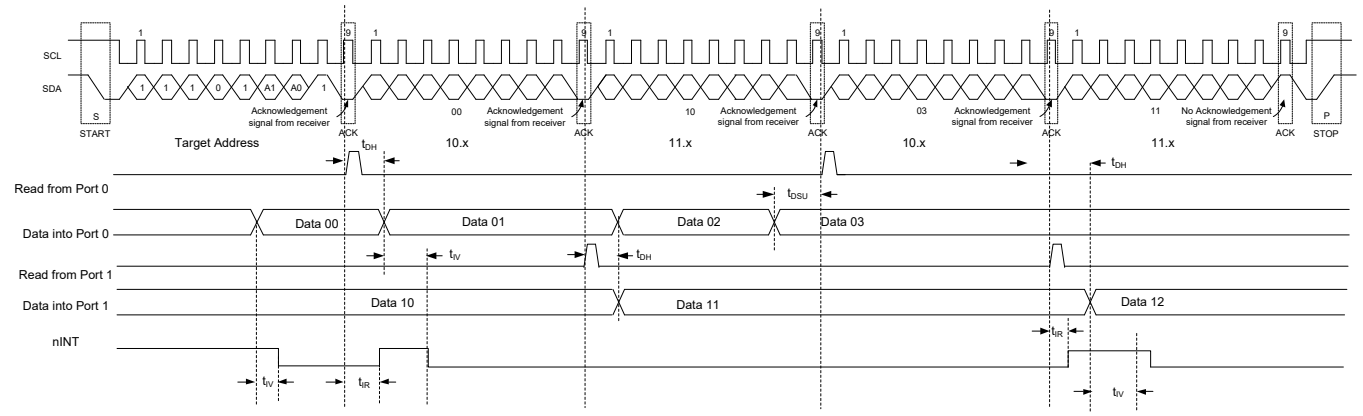



NOTES:

1. A STOP condition could stop data transaction at any time. Despite this, the data presented during the recent validation phase is valid (output mode), assuming that the command byte was previously set to 00.

2. This figure eliminates the command byte transfer, restart and target address call between the initial target address call and actual data transfer from P port (more details refers to Reads).

**Figure 18. Scenario 1 of Read Input Port Register**




NOTES:

1. A STOP condition could stop data transaction at any time. Despite this, the data presented during the recent validation phase is valid (output mode), assuming that the command byte was previously set to 00.

2. This figure eliminates the command byte transfer, restart, and target address call between the initial target address call and actual data transfer from the P port (more details refers to Reads).

**Figure 19. Scenario 2 of Read Input Port Register**

# REGISTER MAPS

All registers are 8-bit and individual bits are named from D[7] (MSB) to D[0] (LSB).

## I²C Register Address Map

Figure 20 shows the address byte of the SGM4591Q.

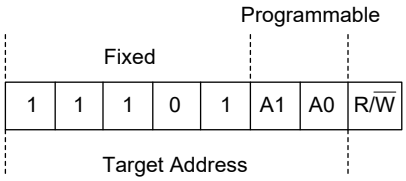



**Figure 20. SGM4591Q Address**

Table 2 shows the address reference of the SGM4591Q.

**Table 2. Address Reference**

| Parameter | | I²C Bus Target Address | |
|---|---|---|---|
| A1 | A0 | Decimal | Hexadecimal |
| L | L | 116 | 74 |
| L | H | 117 | 75 |
| H | L | 118 | 76 |
| H | H | 119 | 77 |

The last bit of the target address defines the read or write operation. 1 (high) performs the read operation, while 0 (low) performs the write operation.

**Control Register and Command Byte**

After acknowledging the address byte of target device successfully, the controller-transmitter would send a command byte stored in the control register. Four bits of the command byte state the operation (read or write) and the internal register (input, output, polarity inversion, configuration, output mode and output anomaly indication) that is affected. These registers support read or write operation via the I²C bus. Command bytes are sent only during write transmission.

After sending a command byte, the addressed register pair continues to be accessed by reads until a new command byte is sent. Figure 21 shows the control register bits.

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0 | 0 | 0 | 0 | B3 | B2 | B1 | B0 |

**Figure 21. Control Register Bits**

## REGISTER MAPS (continued)

### I²C Slave Register Addresses of SGM4591Q: 0x0X

| ADDRESS | REGISTER NAME | TYPE | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x00 | Input Port 0 Register | R | I0[7:0] | | | | | | | |
| 0x01 | Input Port 1 Register | R | I1[7:0] | | | | | | | |
| 0x02 | Output Port 0 Register | R/W | O0[7:0] | | | | | | | |
| 0x03 | Output Port 1 Register | R/W | O1[7:0] | | | | | | | |
| 0x04 | Polarity Inversion Port 0 Register | R/W | N0[7:0] | | | | | | | |
| 0x05 | Polarity Inversion Port 1 Register | R/W | N1[7:0] | | | | | | | |
| 0x06 | Configuration Port 0 Register | R/W | C0[7:0] | | | | | | | |
| 0x07 | Configuration Port 1 Register | R/W | C1[7:0] | | | | | | | |
| 0x08 | Output Mode Setting Port 0 Register | R/W | OC0[7:0] | | | | | | | |
| 0x09 | Output Mode Setting Port 1 Register | R/W | OC1[7:0] | | | | | | | |
| 0x0A | Output Anomaly Indication Port 0 Register | R/W | OA0[7:0] | | | | | | | |
| 0x0B | Output Anomaly Indication Port 1 Register | R/W | OA1[7:0] | | | | | | | |

Bit Types:
R/W: Read/Write bit(s)
R: Read only bit(s)
RC: Bit(s) cleared to 0 by being read
PORV: Power-on Reset Value
n: Parameter code formed by the bits as an unsigned binary number.

# REGISTER MAPS (continued)

## REG0x00: Input Port 0 Register [Reset = 0xXX]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION |
|---|---|---|---|---|
| D[7:0] | I0[7:0] | xxxx xxxx | R | This input port 0 register reflects the incoming logic levels of the corresponding pins. The register just only acts on the read operation, no matter whether the port pins are defined as I/O by the configuration port registers (REG0x06 and REG0x07). Writing to the two registers has no effect. The default value is set by the external port pins' logic level. Before a read operation, send a write transmission with a command byte to show the I²C device that this register is accessed next. |

## REG0x01: Input Port 1 Register [Reset = 0xXX]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION |
|---|---|---|---|---|
| D[7:0] | I1[7:0] | xxxx xxxx | R | This input port 1 register reflects the incoming logic levels of the corresponding pins. The register just only acts on the read operation, no matter whether the port pins are defined as I/O by the configuration port registers (REG0x06 and REG0x07). Writing to the two registers has no effect. The default value is set by the external port pins' logic level. Before a read operation, send a write transmission with a command byte to show the I²C device that this register is accessed next. |

## REG0x02: Output Port 0 Register [Reset = 0xFF]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION |
|---|---|---|---|---|
| D[7:0] | O0[7:0] | 1111 1111 | R/W | The output port 0 register reflects the outgoing logic levels of the corresponding pins defined as outputs by the configuration port registers (REG0x06 and REG0x07). The bit values in this register have no effect on the pins configured as input. Reading from the register reflects the value that is in the flip-flop controlling the output selection, not the actual pin value. |

## REG0x03: Output Port 1 Register [Reset = 0xFF]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION |
|---|---|---|---|---|
| D[7:0] | O1[7:0] | 1111 1111 | R/W | The output port 1 register reflects the outgoing logic levels of the corresponding pins defined as outputs by the configuration port registers (REG0x06 and REG0x07). The bit values in this register have no effect on the pins configured as input. Reading from the register reflects the value that is in the flip-flop controlling the output selection, not the actual pin value. |

## REG0x04: Polarity Inversion Port 0 Register [Reset = 0x00]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION |
|---|---|---|---|---|
| D[7:0] | N0[7:0] | 0000 0000 | R/W | The polarity inversion port 0 register allows polarity inversion of the corresponding port pins defined as input by the configuration port registers (REG0x06 and REG0x07). A bit in the register is written as '1', then the polarity of corresponding port pin is inverted. A bit in the register is written as '0', then the original polarity of corresponding port pin is retained. |

## REG0x05: Polarity Inversion Port 1 Register [Reset = 0x00]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION |
|---|---|---|---|---|
| D[7:0] | N1[7:0] | 0000 0000 | R/W | The polarity inversion port 1 register allows polarity inversion of the corresponding port pins defined as input by the configuration port registers (REG0x06 and REG0x07). A bit in the register is written as '1', then the polarity of corresponding port pin is inverted. A bit in the register is written as '0', then the original polarity of corresponding port pin is retained. |

# REGISTER MAPS (continued)

## REG0x06: Configuration Port 0 Register [Reset = 0xFF]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION |
|---|---|---|---|---|
| D[7:0] | C0[7:0] | 1111 1111 | R/W | The configuration port 0 register is used to configure the directions of the port pins. A bit in the register is written as '1', then the corresponding port pin is enabled as a high-impedance input. A bit in the register is written as '0', then the corresponding port pin is enabled as an output. The output mode can be set as push-pull or open-drain by the output mode setting registers (REG0x08 and REG0x09). |

## REG0x07: Configuration Port 1 Register [Reset = 0xFF]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION |
|---|---|---|---|---|
| D[7:0] | C1[7:0] | 1111 1111 | R/W | The configuration port 1 register is used to configure the directions of the port pins. A bit in the register is written as '1', then the corresponding port pin is enabled as a high-impedance input. A bit in the register is written as '0', then the corresponding port pin is enabled as an output. The output mode can be set as push-pull or open-drain by the output mode setting registers REG0x08 and REG0x09). |

## REG0x08: Output Mode Setting Port 0 Register [Reset = 0xFF]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION |
|---|---|---|---|---|
| D[7:0] | OC0[7:0] | 1111 1111 | R/W | The output mode setting port 0 register can configure the output mode of port pins defined as outputs. A bit in the register is written as '1', then the corresponding port pin is configured as Push-Pull mode. A bit in the register is written as '0', then the corresponding port pin is configured as open-drain mode. |

## REG0x09: Output Mode Setting Port 1 Register [Reset = 0xFF]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION |
|---|---|---|---|---|
| D[7:0] | OC1[7:0] | 1111 1111 | R/W | The output mode setting port 1 register can configure the output mode of port pins defined as outputs. A bit in the register is written as '1', then the corresponding port pin is configured as Push-Pull mode. A bit in the register is written as '0', then the corresponding port pin is configured as open-drain mode. |

## REG0x0A: Output Anomaly Indication Port 0 Register [Reset = 0x00]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION |
|---|---|---|---|---|
| D[7:0] | OA0[7:0] | 0000 0000 | R/W | The output anomaly indication port 0 register sets the indication of nINT pin that occurring output short-circuit. The default value of each bit is '0', a bit in the register is written '1', then the corresponding output port pin would trigger an interrupt when its actual output level state differs from its corresponding output port register (REG0x02). When the actual output level state changes to match its corresponding output port register, the interrupt is reset. The reset that occurs when the processor reads the corresponding input port register would only occur once, and then the interrupt would not be triggered when the output anomaly occurs again. When a bit in the register is written '0', the corresponding port pin output anomaly indicator function is disabled. The nINT pin generates an interrupt whenever an input port changes state, regardless of what state the register is set to. |

## REGISTER MAPS (continued)

### REG0x0B: Output Anomaly Indication Port 1 Register [Reset = 0x00]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION |
|---|---|---|---|---|
| D[7:0] | OA1 | 0000 0000 | R/W | The output anomaly indication port 1 register sets the indication of nINT pin that occurring output short-circuit. The default value of each bit is '0', a bit in the register is written '1', then the corresponding output port pin would trigger an interrupt when its actual output level state differs from its corresponding output port register (REG0x03). When the actual output level state changes to match its corresponding output port registers, the interrupt is reset. The reset that occurs when the processor reads the corresponding input port register would only occur once, and then the interrupt would not be triggered when the output anomaly occurs again. When a bit in the register is written '0', the corresponding port pin output anomaly indicator function is disabled. The nINT pin generates an interrupt whenever an input port changes state, regardless of what state the register is set to. |

# APPLICATION INFORMATION

I/O expanders, such as SGM4591Q, are mainly used for LEDs control (for feedback or status lights), digital signals' enable/disable, and even output reading of other devices.

SGM4591Q connects to an $I^2C$ bus as a target, and the bus may contain any other target devices. SGM4591Q is usually placed remotely from the controller and close to the GPIO that the controller needs to monitor or control.

## Design Requirements

### Junction Temperature and Power Dissipation

In order to verify the safe operation of the device, the junction temperature of SGM4591Q must be calculated due to many of the parameters are rated over junction temperature. Equation 1 shows the calculation of junction temperature.

$$T_J = T_A + (\theta_{JA} \times P_D) \quad (1)$$

$\theta_{JA}$ is the standard junction to ambient thermal resistance measurement of the package. $P_D$ is the total power dissipation of the device. Equation 2 shows the approximate calculation.

$$P_D \approx (I_{CC\_STATIC} \times V_{CC}) + \sum P_{D\_PORT\_L} + \sum P_{D\_PORT\_H} \quad (2)$$

The sum of static power and the power dissipated by each port are shown in Equation 2, which is an approximate value of power dissipation in the device. It should be noted that the power consumption of the nINT and SDA pins are ignored in this equation. If these transients are small, they are pulled down, then Equation 3 can easily include them in the power dissipation calculation, which gives the maximum power dissipation.

$$P_{D\_PORT\_L} = (I_{OL} \times V_{OL}) \quad (3)$$

The power consumption of a single port pin set to low output is shown in Equation 3. A port's power consumption is the $V_{OL}$ of the port multiplied by its absorbed current.

$$P_{D\_PORT\_H} = \left[I_{OH} \times (V_{CC} - V_{OH})\right] \quad (4)$$

Equation 4 shows the power dissipation of a single port pin set to high output. The power consumed by a port is the current provided by the port multiplied by the voltage drop across the device (the difference between $V_{CC}$ and output voltage).

### Minimize $I_{CC}$ when I/Os Control LEDs

Normally, an I/O used to control an LED is connected to $V_{CC}$ through a resistor due to that the LED acts as a diode. The input voltage of an I/O is about 1.2V less than $V_{CC}$ when the LED is off. In the applications powered by battery, for minimizing the current consumption when the LED is off, the I/O pin voltage should be greater than or equal to the supply voltage.

Figure 22 shows that a 100kΩ resistor is in parallel with the LED. As shown in Figure 23, $V_{CC}$ is at least 1.2V lower than LED power supply voltage. Both the two ways can keep the supply voltage of an I/O equals to or above $V_{CC}$ and prevent additional power current consumption when the LED is off.

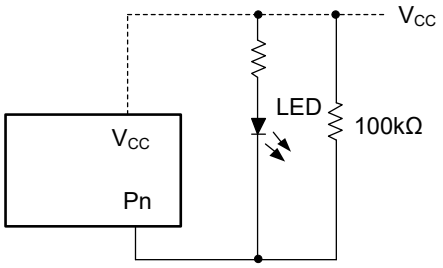



**Figure 22. High-Value Resistor in Parallel with LED**

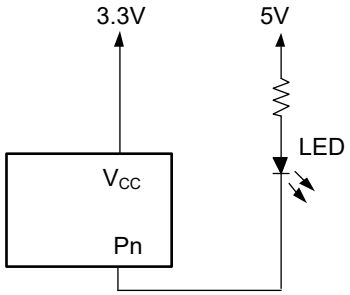



**Figure 23. Device Supplied by Lower Voltage**

# APPLICATION INFORMATION (continued)

## Power-on Reset (POR) Requirements

When a glitch or data corruption occurs, the power-on reset feature of the SGM4591Q can be reset to the default conditions. The voltage waveform of POR is shown in Figure 24.

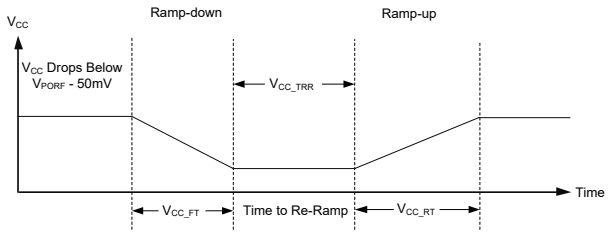



**Figure 24. $V_{CC}$ Lowered below the POR Threshold, then Ramped Back**

The power glitch can also have an effect on the POR operation of SGM4591Q. The width and height of glitch are interdependent. The POR performance can also be affected by the bypass capacitance, source and device impedance, etc.

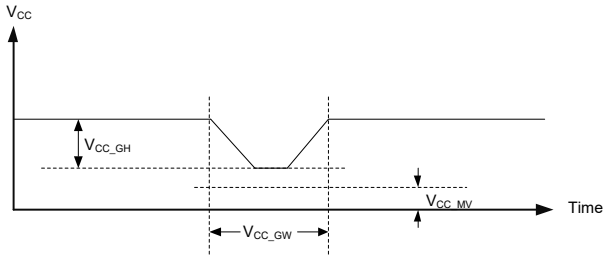



**Figure 25. Width, Height and Minimum Voltage of Glitch**

$V_{POR}$ is the voltage which reset condition, registers, $I^2C$ and SMBus are rated, which is essential to POR. $V_{POR}$ varies based on the supply voltage being reduced to or from 0. Figure 26 and Table 3 show more details.

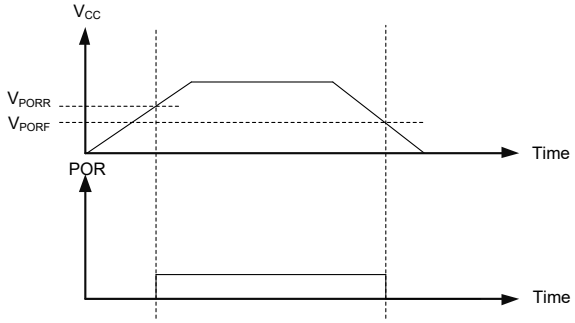



**Figure 26. $V_{POR}$**

Table 3 shows the performance of POR feature.

**Table 3. Recommended Supply Sequence and Ramp Rates (1)**

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Fall Rate (2) | $V_{CC\_FT}$ | See Figure 24 | 0.1 | | | ms |
| Rise Rate (2) | $V_{CC\_RT}$ | See Figure 24 | 0.1 | | | ms |
| Time to Re-Ramp (when $V_{CC}$ drops to $V_{POR\_MIN}$ - 50mV or when $V_{CC}$ drops to GND) (2) | $V_{CC\_TRR}$ | See Figure 24 | 2 | | | μs |
| The level (referenced to $V_{CC}$) that $V_{CC}$ can glitch down to, but not cause a functional disruption when $V_{CC\_GW}$. (2) | $V_{CC\_GH}$ | See Figure 25 | | | 1.2 | V |
| The minimum voltage that $V_{CC}$ can glitch down to without causing a reset ($V_{CC\_GH}$ must not be violated) (2) | $V_{CC\_MV}$ | See Figure 25 | 1.55 | | | V |
| Glitch Width that does not cause a functional disruption (2) | $V_{CC\_GW}$ | See Figure 25 | | | 10 | μs |
| Power-on Reset Voltage on Rising $V_{CC}$ | $V_{PORR}$ | | | 1.2 | 1.5 | V |
| Power-on Reset Voltage on Falling $V_{CC}$ | $V_{PORF}$ | | 0.55 | 1.0 | | V |

NOTES:

1. $T_A$ = -40℃ to +125℃, unless otherwise noted.

2. Specified by design and characterization, not production tested.

# APPLICATION INFORMATION (continued)

## Layout Guidelines

The PCB layout of SGM4591Q should follow the common layout guidelines, but other concerns about high-speed data transfer cannot affect the $I^2C$ signal speed, such as the differential pairs and the matched impedances.

Right angles should be avoided in signal traces in all PCB layouts. Fan out signal traces away from each other upon leaving the vicinity of the IC, and use trace with thicker width to carry the larger current that normally passes through the power supply and ground traces. Bypass and decoupling capacitors are commonly used to control the voltage on $V_{CC}$ pins. Larger capacitors are used to provide additional power in the case of a short-circuit power failure, and smaller capacitors are used to filter out high-frequency ripple. These capacitors must be put as close as possible to SGM4591Q.

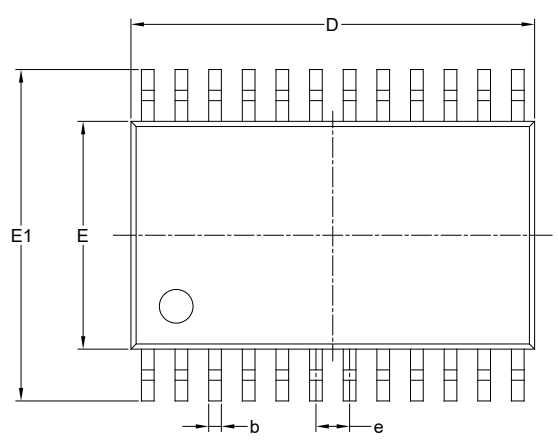
# REVISION HISTORY

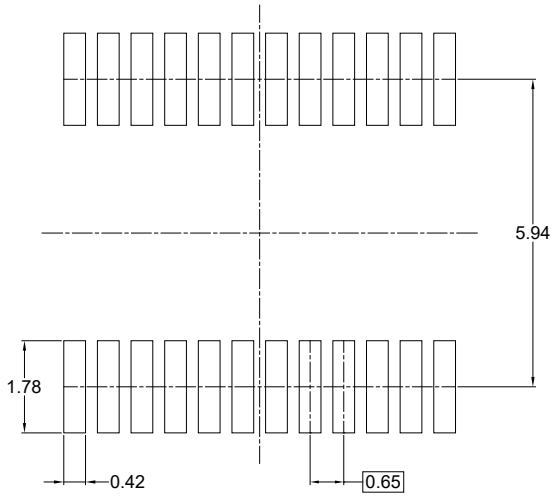
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Original (OCTOBER 2024) to REV.A | Page |
|---|---|
| Changed from product preview to production data | All |

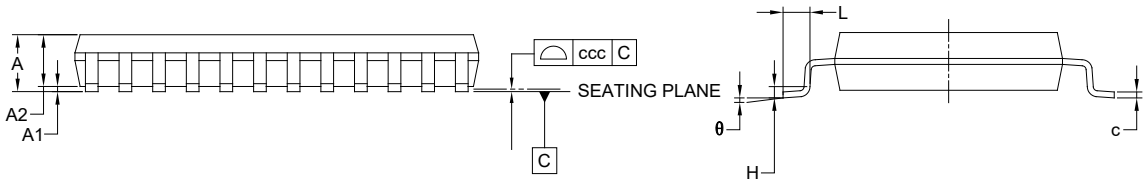
# PACKAGE OUTLINE DIMENSIONS

## TSSOP-24




**RECOMMENDED LAND PATTERN** (Unit: mm)

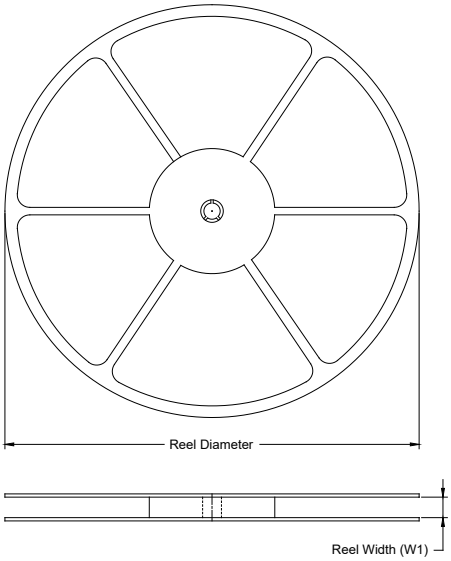



| Symbol | Dimensions In Millimeters | | |
|---|---|---|---|
| | MIN | MOD | MAX |
| A | - | - | 1.200 |
| A1 | 0.050 | - | 0.150 |
| A2 | 0.800 | - | 1.050 |
| b | 0.190 | - | 0.300 |
| c | 0.090 | - | 0.200 |
| D | 7.700 | - | 7.900 |
| E | 4.300 | - | 4.500 |
| E1 | 6.200 | - | 6.600 |
| e | 0.650 BSC | | |
| L | 0.450 | - | 0.750 |
| H | 0.250 TYP | | |
| θ | 0° | - | 8° |
| ccc | 0.100 | | |

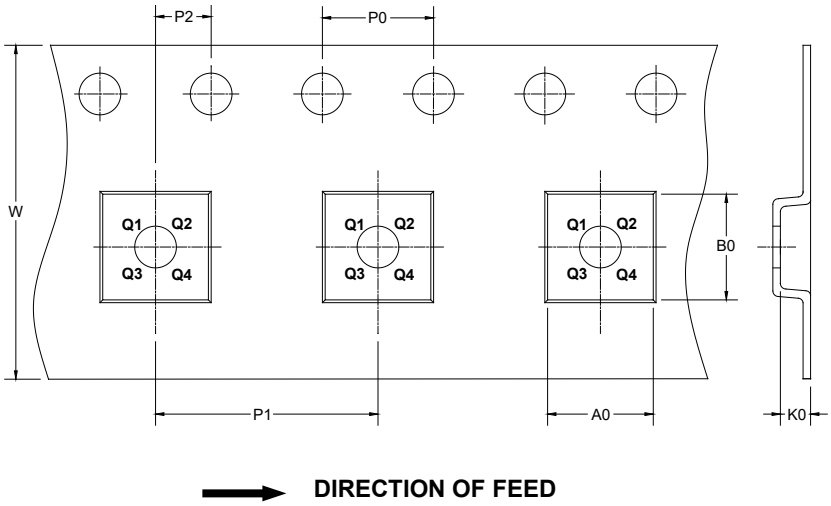
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-153.

# TAPE AND REEL INFORMATION

### REEL DIMENSIONS




### TAPE DIMENSIONS



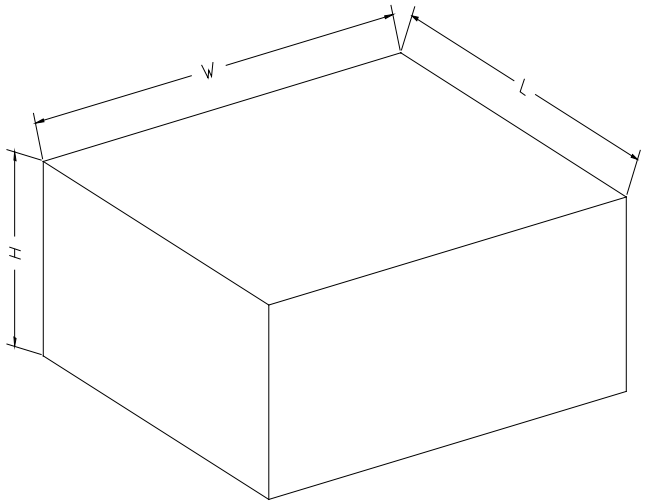

NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF TAPE AND REEL

| Package Type | Reel Diameter | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | P1 (mm) | P2 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|
| TSSOP-24 | 13" | 16.4 | 6.80 | 8.30 | 1.60 | 4.0 | 8.0 | 2.0 | 16.0 | Q1 |

DD0001

## CARTON BOX DIMENSIONS




NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF CARTON BOX

| Reel Type | Length (mm) | Width (mm) | Height (mm) | Pizza/Carton |
|---|---|---|---|---|
| 13″ | 386 | 280 | 370 | 5 |

DD0002