

8ch Low-side switch

BD8LA700EFV-C

Features

- Monolithic power IC that has a built-in control part (CMOS) and a power MOS FET on 1chip
- 8ch Low-side switch for driving resistive, inductive load
- 16bit Serial peripheral interface(SPI) for diagnostics and control
- Built-in Open Load Detection circuit in output-off state
- Built-in Over Current Protection circuit (OCP)
- Built-in Active Clamp circuit
- Built-in Thermal shutdown circuit (TSD)
- Low On resistance of $R_{ON}=700m\Omega$ ($V_{IN}=5V$, $T_j=25^\circ C$, $I_o=0.2A$, Typ)
- Surface mount HTSSOP-B24 Package
- AEC-Q100 Qualified (Note 1) Grade1

Overview

BD8LA700EFV is 8ch Low-Side switch for automotive and industrial equipment. It has a built-in, Open Load Detection circuit, Over Current Protection circuit, Active clamp circuit and Thermal Shutdown circuit.

Application

For driving resistive, inductive load

Basic Application Circuit (Recommendation)

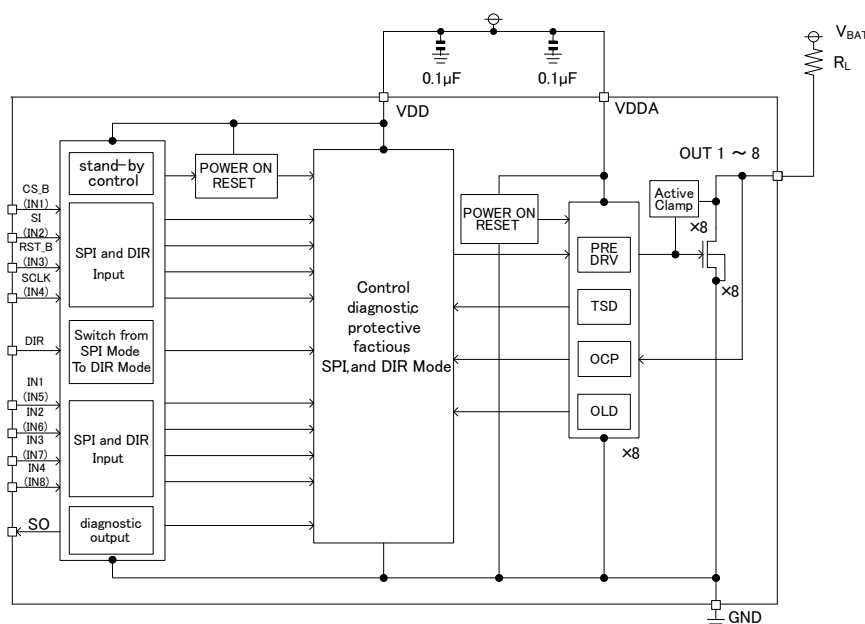
Product Summary

Digital part Operating voltage	3.0V to 5.5V
Analog part Operating voltage	4.0V to 5.5V
On-state resistance (25°C, Typ)	700mΩ
Over current limit (Typ)	1.2A
Active clamp energy(25°C)	75mJ

Package

HTSSOP-B24

W(Typ) x D(Typ) x H(Max)
7.80mm x 7.60mm x 1.00mm



Pin Descriptions

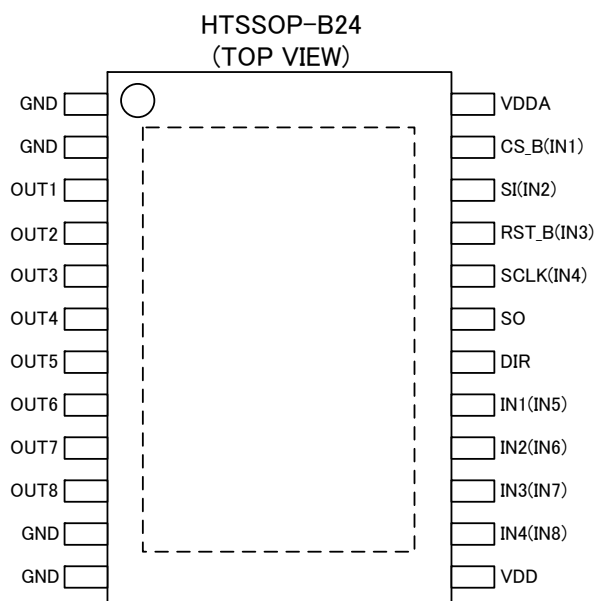
Pin	Symbol	I/O ^(Note 1)		Function
1	GND	-		GND
2	GND	-		GND
3	OUT1	O		Channel 1 output
4	OUT2	O		Channel 2 output
5	OUT3	O		Channel 3 output
6	OUT4	O		Channel 4 output
7	OUT5	O		Channel 5 output
8	OUT6	O		Channel 6 output
9	OUT7	O		Channel 7 output
10	OUT8	O		Channel 8 output
11	GND	-		GND
12	GND	-		GND
13	VDD	-		Digital power supply
14	IN4(IN8)	I	PD	Control input for Channel 4 and 8 (DIR=L) / Control input for Channel 8 (DIR=H)
15	IN3(IN7)	I	PD	Control input for Channel 3 and 7 (DIR=L) / Control input for Channel 7 (DIR=H)
16	IN2(IN6)	I	PD	Control input for Channel 2 and 6 (DIR=L) / Control input for Channel 6 (DIR=H)
17	IN1(IN5)	I	PD	Control input for Channel 1 and 5 (DIR=L) / Control input for Channel 5 (DIR=H)
18	DIR	I	PD	SPI mode, DIR mode change input terminal
19	SO	O		Serial data output terminal
20	SCLK(IN4)	I	PD	Serial clock (DIR=L) / Control input for Channel 4 (DIR=H)
21	RST_B(IN3)	I	PD	Reset terminal (DIR=L) / Control input for Channel 3 (DIR=H)
22	SI(IN2)	I	PD	Serial data input (DIR=L) / Control input for Channel 2 (DIR=H)
23	CS_B(IN1)	I	PU/PD ^(Note 2)	SPI enable input (DIR=L) / Control input for Channel 1 (DIR=H)
24	VDDA	-		Analog power supply
FIN	FIN	-		Since it has connected with sub of IC, please connect the heat dissipation metal to external GND potential.

(Note 1) O : Output terminal, I : Input terminal

PD : Pull Down terminal, PU : Pull Up terminal

(Note 2) Pull Up at DIR=Low setting, Pull Down at DIR=High

Pin Configurations



Absolute Maximum Ratings

Item	Symbol	Limit values	Unit
Power supply voltage (Pin No:13,24)	V_{CC}	-0.3 to +7	V
Output voltage (Pin No:3 to 10)	$V_{DS1\sim 8}$	-0.3 to 45(Internally limited)	V
Output current (Pin No:3 to 10)	I_{Dn}	0.5(Internally limited) ^(Note 1)	A
Diagnostic output voltage (Pin No:19)	V_{SO}	-0.3 to +7	V
Input voltage(Pin No:14 to 18,20 to 23)	V_{IN}	-0.3 to +7	V
Junction temperature range	T_j	-40 to +150	°C
Storage temperature range	T_{stg}	-55 to +150	°C
Maximum junction temperature	T_{jmax}	150	°C
Active clamp energy (single pulse) ($T_{j(0)}=25^{\circ}\text{C}$)	E_{S1}	75 ^(Note 2)	mJ
Active clamp energy (single pulse) ($T_{j(0)}=150^{\circ}\text{C}$)	E_{S2}	25 ^(Note 3)	mJ
Active clamp energy (repetitive) ($T_{j(0)}=105^{\circ}\text{C}$)	E_{AR}	20 ^(Note 4)	mJ

(Note 1) However, never exceed T_{jmax} .(Note 2) Max Active clamp energy at $T_{j(0)} = 25^{\circ}\text{C}$, using single non-repetitive pulse of 0.5A(Note 3) Max Active clamp energy at $T_{j(0)} = 150^{\circ}\text{C}$, using single non-repetitive pulse of 0.5A. Not 100% tested.(Note 4) Max Active clamp energy at $T_{j(0)} = 105^{\circ}\text{C}$, using repetitive pulse of 0.4A and cycles of 1M times. Not 100% tested.**Operating Voltage Ratings (-40°C ≤Tj ≤+150°C)**

Item	Code	Limit values	Unit
Digital part Operating voltage	V_{DD}	3.0 to 5.5	V
Analog part Operating voltage	V_{DDA}	4.0 to 5.5	V

Electrical Characteristics (unless otherwise specified, $V_{DDA}=V_{DD}=5V$, $-40^{\circ}C \leq T_j \leq +150^{\circ}C$)

Item	Symbol	Limit values			Unit	Condition
		Min	Typ	Max		
[Power Supply Block]						
VDDA Standby current (All output on standby mode)	I _{DDAS}	-	0	20	μA	V _{DDA} =V _{DD} =V _{CS_B} =5V V _{RST_B} =0V
VDD Standby current (All output on standby mode)	I _{DDS}	-	0	20	μA	V _{DDA} =V _{DD} =V _{CS_B} =5V V _{RST_B} =0V
VDDA Operating current)	I _{DDA}	-	3.0	5.0	mA	V _{DDA} =V _{DD} =5V
VDD Operating current)	I _{DD}	-	0.5	1.0	mA	V _{DDA} =V _{VDD} =5V
VDDA power on reset Threshold Voltage	V _{PORA}	-	-	4.0	V	
VDD power on reset Threshold Voltage	V _{POR}	-	-	2.7	V	
[Input PIN]						
L level input voltage	V _{INL}	0	-	VDD×0.2	V	
H level input voltage	V _{INH}	VDD×0.7	-	VDD	V	
Input Hysteresis	V _{HYS}	0.1	0.3	0.5	V	
L level input current 1 (RST_B,DIR,IN1 to IN4,SCLK,SI)	I _{INL1}	-10	0	10	μA	V _{RST_B} , V _{DIR} , V _{IN1} to V _{IN4} , V _{SCLK} , V _{SI} =0V
L level input current 2(CS_B)	I _{INL2}	-100	-50	-25	μA	V _{CS_B} =0V, V _{DIR} =0V
L level input current 3(CS_B)	I _{INL3}	-10	0	10	μA	V _{CS_B} =0V, V _{DIR} =5V
H level input current 1 (RST_B,DIR,IN1 to IN4,SCLK,SI)	I _{INH1}	25	50	100	μA	V _{RST_B} , V _{DIR} , V _{IN1} to V _{IN4} , V _{SCLK} , V _{SI} =5V
H level input current 2(CS_B)	I _{INH2}	-10	0	10	μA	V _{CS_B} =5V, V _{DIR} =0V
H level input current 3(CS_B)	I _{INH3}	25	50	100	μA	V _{CS_B} =5V, V _{DIR} =5V
[Power MOS Output]						
Output ON resistance	R _{DS(ON)}	-	0.70	0.87	Ω	V _{DD} =V _{DDA} =5V, I _{Dn} ^(Note 1) =0.2A, T _j =25°C
		-	1.30	1.56	Ω	V _{DD} =V _{DDA} =5V, I _{Dn} ^(note 1) =0.2A, T _j =150°C
Output leak current	I _{L(OFF)}	-	0	1	μA	V _{DS} =30V, T _j =25°C, V _{DIR} =0V
		-	5	20	μA	V _{DS} =30V, T _j =150°C, V _{DIR} =0V
Output leak current (Open load detected)	I _{OL}	15	40	90	μA	V _{DS} =40V, V _{DIR} =5V
Switching time	t _{ON}	-	30	50	μs	V _{DD} =5V, V _{INn} ^(Note 1) =0V/5V, R _L =60Ω, V _{BAT} =12V, V _{DIR} =5V
	t _{OFF}	-	30	50	μs	V _{DD} =5V, V _{INn} ^(Note 1) =0V/5V, R _L =60Ω, V _{BAT} =12V, V _{DIR} =5V
Slew rate on	dV/dt _{ON}	0.3	1.0	3.0	V/μs	V _{DD} =5V, V _{INn} ^(Note 1) =0V/5V, R _L =60Ω, V _{BAT} =12V, V _{DIR} =5V, 80% to 20% of V _{BAT}
Slew rate off	-dV/dt _{OFF}	0.3	1.0	3.0	V/μs	V _{DD} =5V, V _{INn} ^(Note 1) =0V/5V, R _L =60Ω, V _{BAT} =12V, V _{DIR} =5V, 20% to 80% of V _{BAT}
PWM Output range	f _{PWM}	-	-	5	kHz	V _{DD} =5V, V _{INn} ^(Note 1) =0V/5V, R _L =60Ω, V _{DIR} =5V, V _{BAT} =12V
Output clamp voltage	V _{CL}	45	50	55	V	I _{Dn} ^(Note 1) =1mA(output off state)

(Note 1) "n" shows the channel number.

Electrical Characteristics (unless otherwise specified, V _{DDA} =V _{DD} =5V, -40°C≤T _j ≤+150°C)						
Item	Symbol	Limit values			Unit	Condition
		Min	Typ	Max		
[Serial Output]						
L level output voltage	V _{SOL}	-	0.3	0.6	V	I _{SO} =1mA
H level output voltage	V _{SOH}	VDD-0.6	VDD-0.3	-	V	I _{SO} =-1mA
Serial out output leak current	I _{SO(OFF)}	-5	0	5	μA	
[Protect circuit]						
Over current detection current	I _{OCP(ON)}	0.5	1.2	2.0	A	
Over current detection time	t _{OCP}	400	1000	2200	μs	
Open load relase voltage	V _{OLD(OFF)}	1.2	2.5	3.5	V	
Open load detection voltage	V _{OLD(ON)}	1.0	2.0	3.0	V	V _{INn} ^(Note 1) =0V, V _{DIR} =5V
Open load detection time	t _{OLD}	50	150	600	μs	
TSD detection temperature ^(Note 2)	T _{jd}	-	175	-	°C	

(Note 1) " n" shows the channel number.
(Note 2) Not 100% tested..

Definition

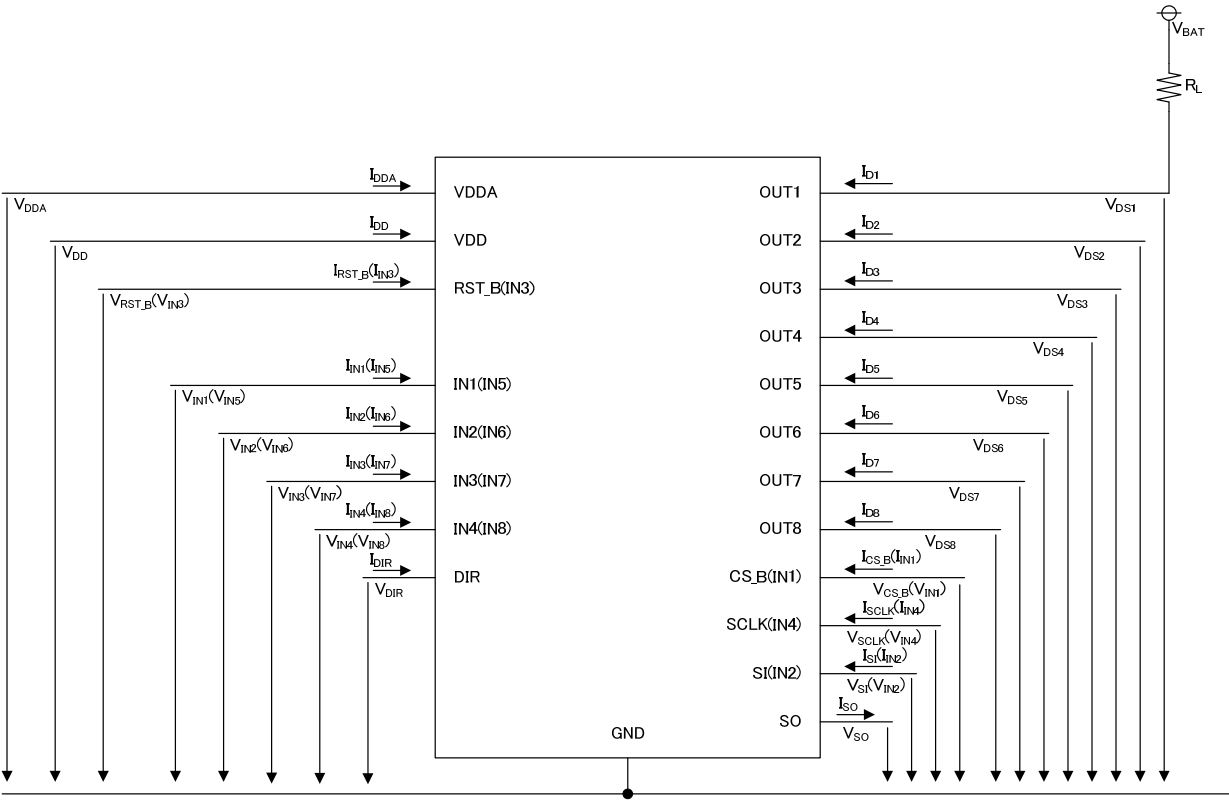


Figure 1. Definition

Measurement Circuit

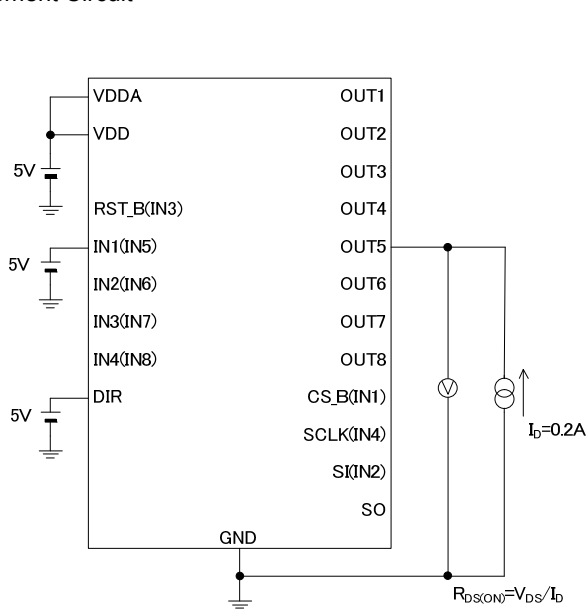


Figure 2. Output ON Resistance Measuring Circuit Diagram

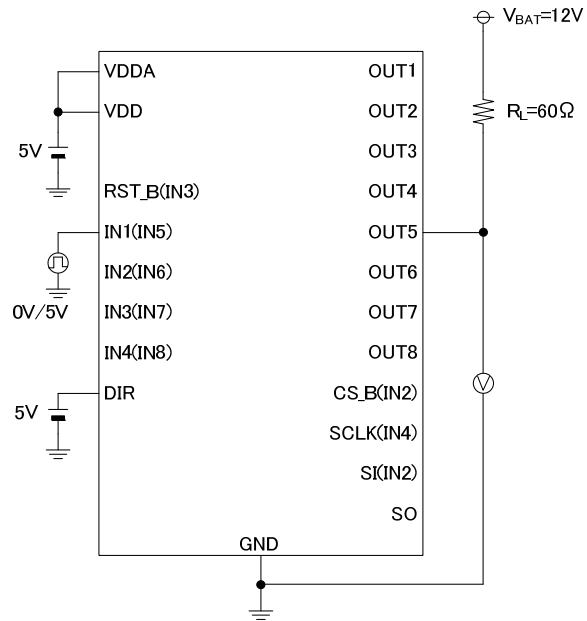


Figure 3. Switching Time Measuring Circuit Diagram

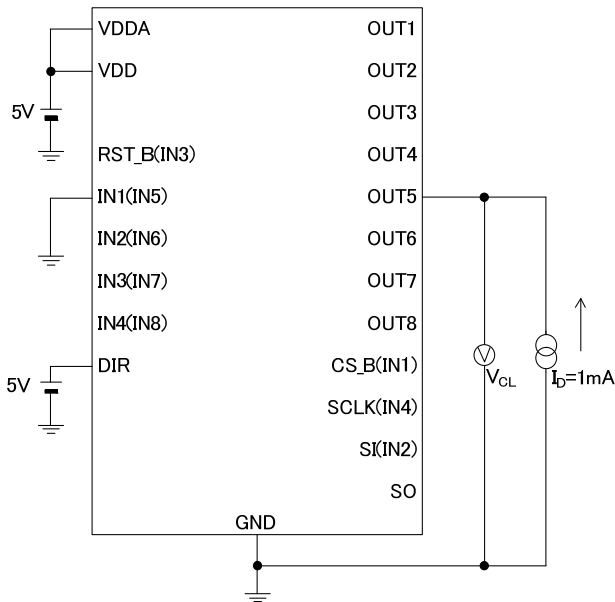


Figure 4. Output Clamp Voltage Measuring Circuit Diagram

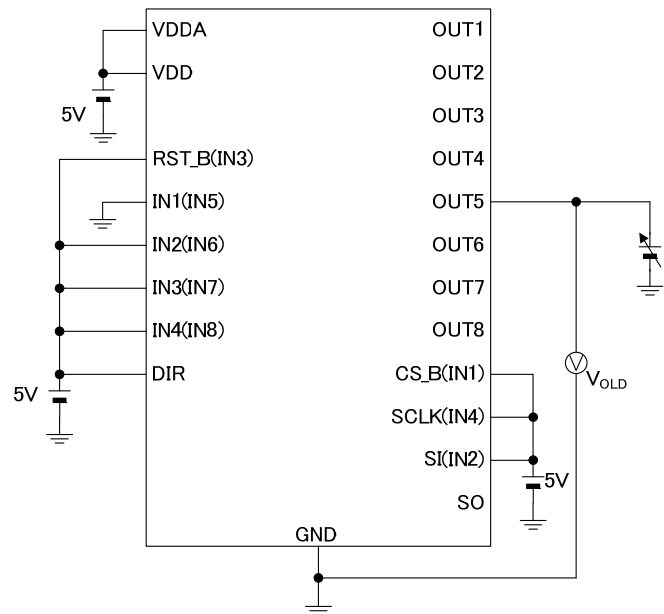


Figure 5. Open Detection Measuring Circuit Diagram

DIR(Direct)mode Diagnostic Output Truth Table

V_{IN}	TSD	OUTPUT		mode	V_{SO}	Output state
		V_{OUT}	I_{OUT}			
H	OFF	-	$I_D < 0.5A$	Normal	L	ON
			$I_D \geq 0.5 \text{ to } 2.0A$	Over current detection	H	OFF
	ON	-	-	Thermal shut down	H	OFF
L	-	$V_{DS} > 3.0V$	-	Normal	L	OFF
		$V_{DS} \leq 1.0 \text{ to } 3.0V$	-	Open load detection	H	OFF

Characteristic Data (Reference Data) ($V_{DD}=5V$, $V_{DDA}=5V$, $I_N=5V$, $T_j=25^{\circ}C$ unless otherwise is specified)

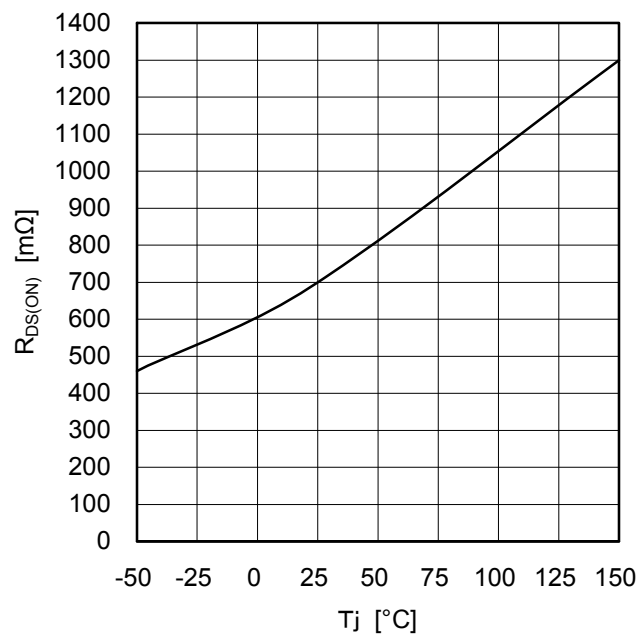


Figure 6. Output ON Resistance Characteristic [Temperature Characteristic]

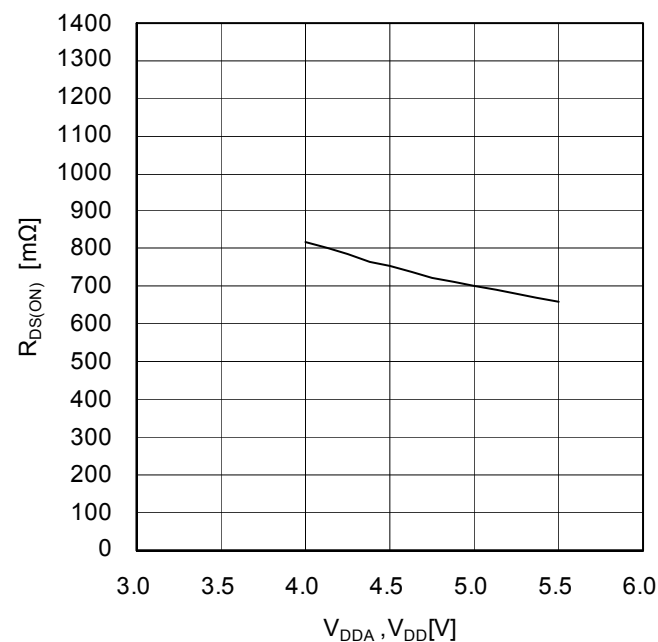


Figure 7. Output ON Resistance Characteristic [Source Voltage Characteristic]

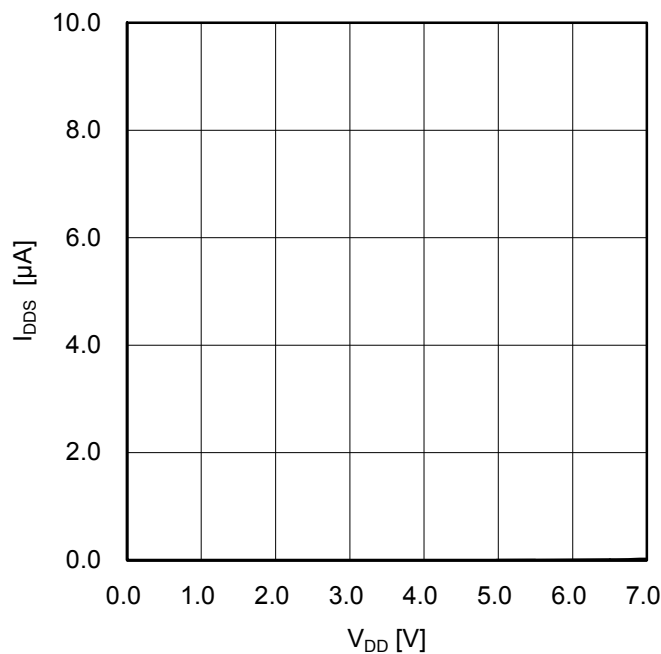


Figure 8. Standby Current Characteristic (VDD)

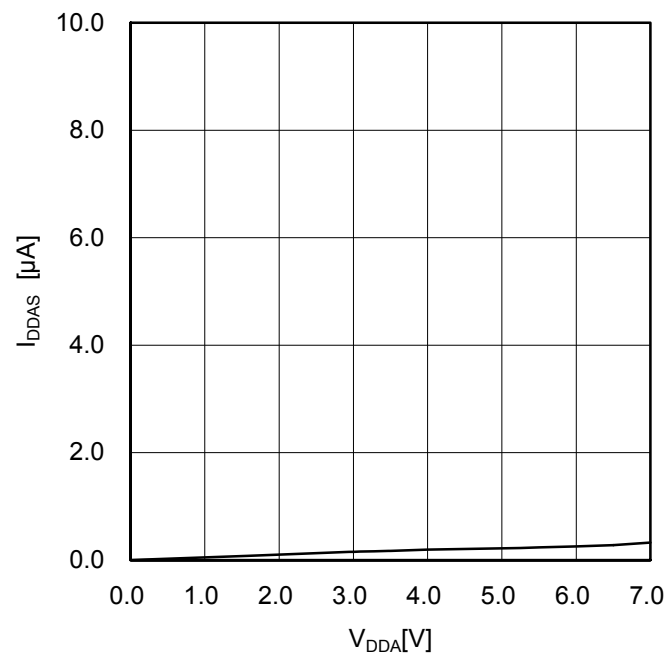


Figure 9. Standby Current Characteristic (VDDA)

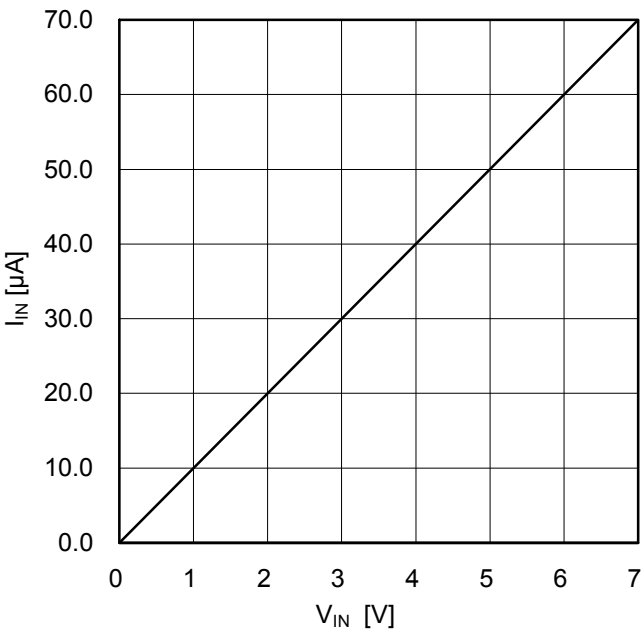


Figure 10. Input current Characteristic
(IN1~4, DIR, SCLK, SI, RST_B, CS_B^(Note 1))

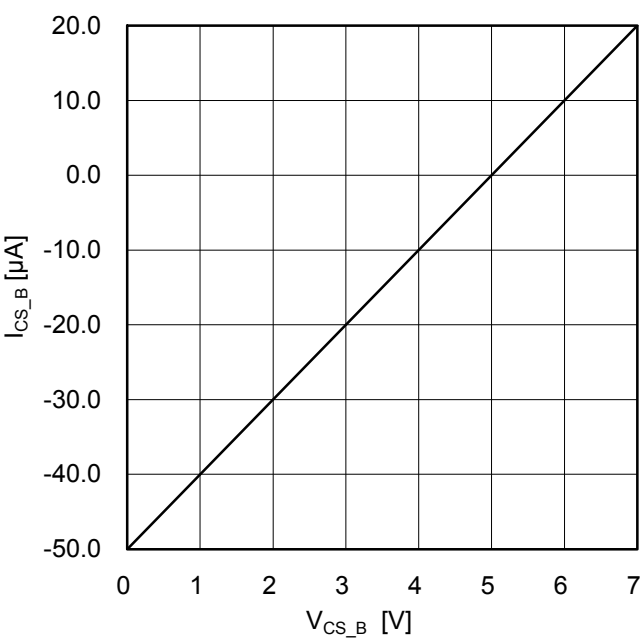


Figure 11. Input current Characteristic (CS_B)

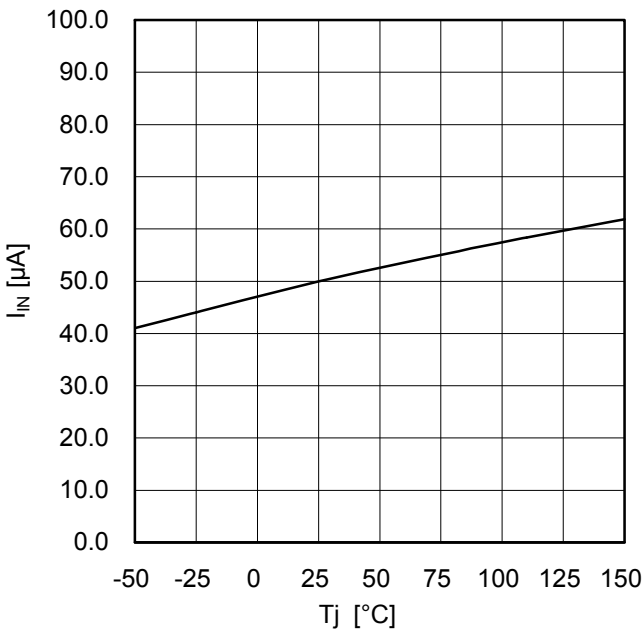


Figure 12. Input current Characteristic
[Temperature Characteristic]
(V_{IN1} to 4, V_{SCLK}, V_{SI}, V_{CS_B}^(Note 1), V_{RST_B}=5V)
(Note 1)DIRMode

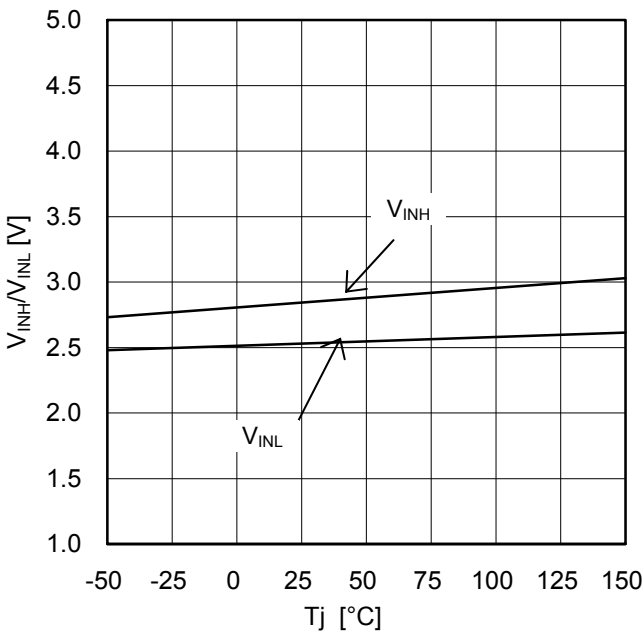


Figure 13. Input Voltage Threshold Characteristic
[Temperature Characteristic]

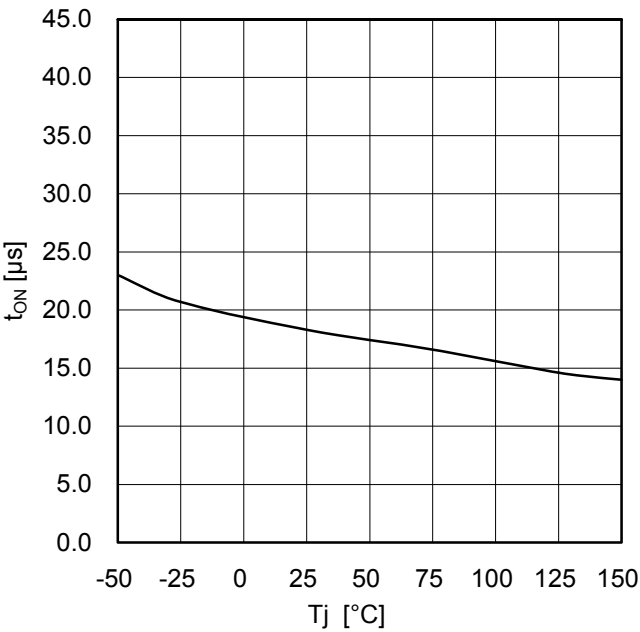


Figure 14. Switching Time (t_{ON})
[Temperature Characteristic]

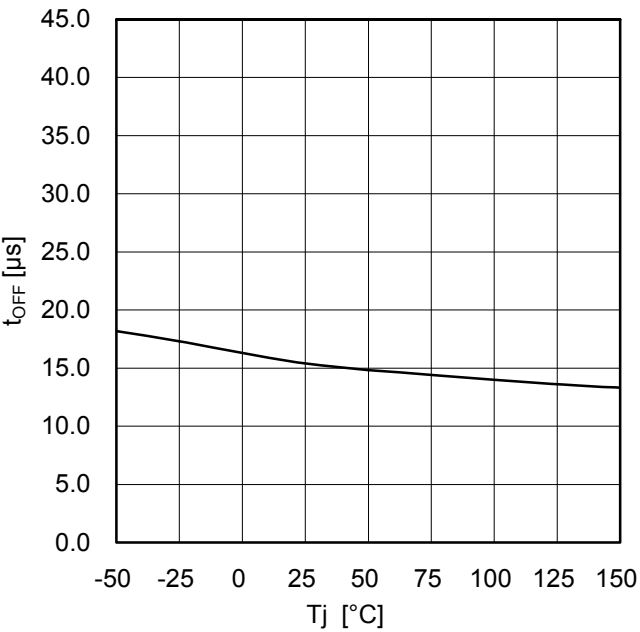


Figure 15. Switching Time (t_{OFF})
[Temperature Characteristic]

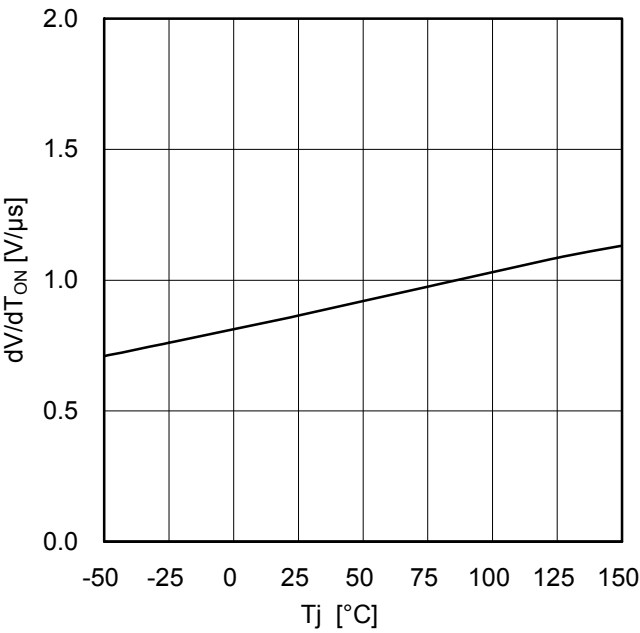


Figure 16. Slew Rate (at ON)
[Temperature Characteristic]

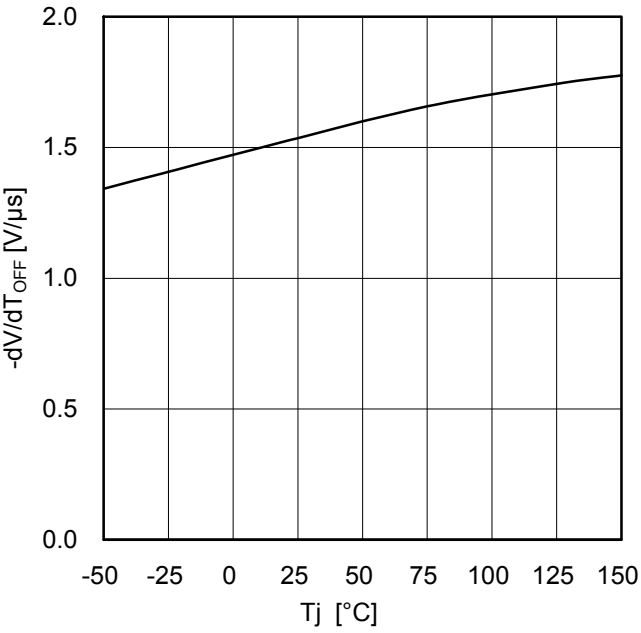


Figure 17. Slew Rate (at OFF)
[Temperature Characteristic]

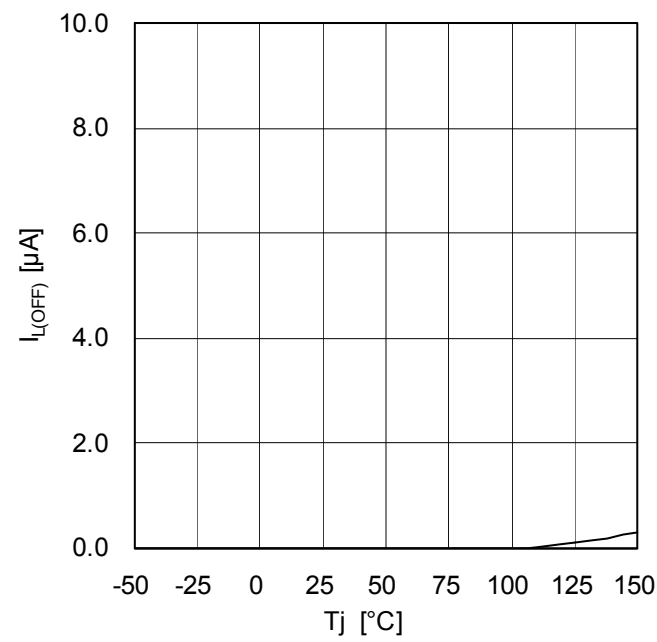


Figure 18. Output Leak Current
[Temperature Characteristic](V_{DS}=30V)

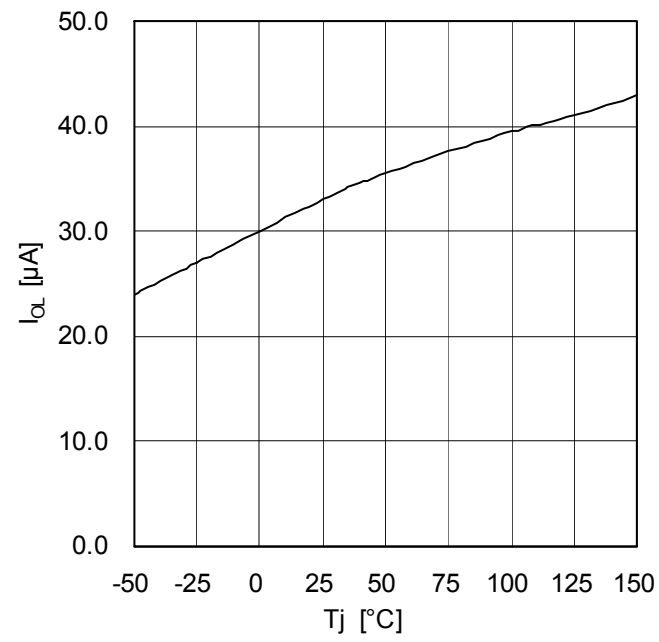


Figure 19. Output Leak Current (Open detect)
[Temperature Characteristic](V_{DS} =40V)

Switching Time Measurement

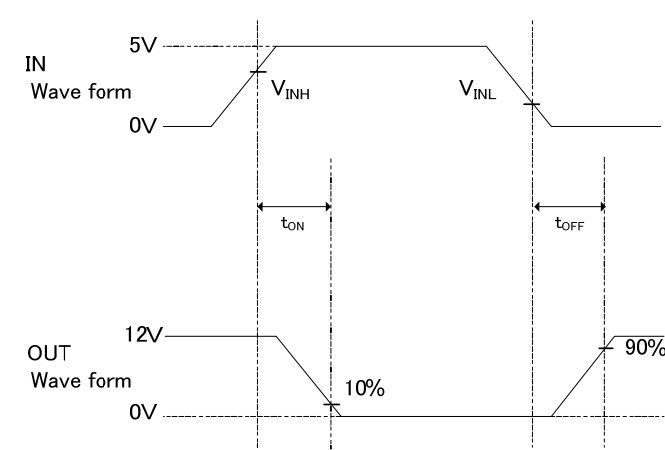


Figure 20. Switching Time

Timing Chart with Inductive Load

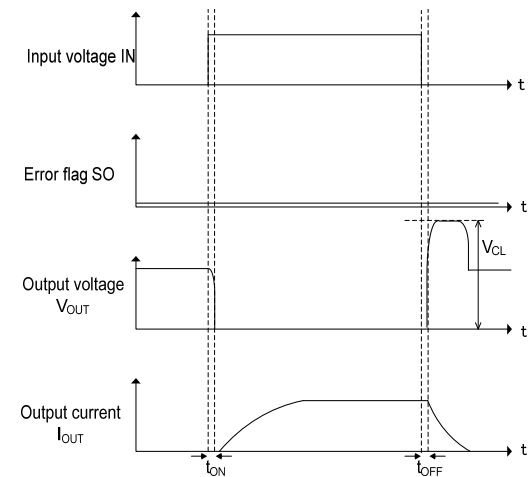
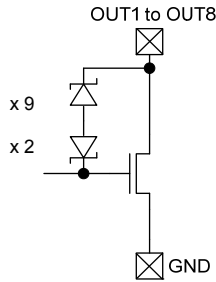
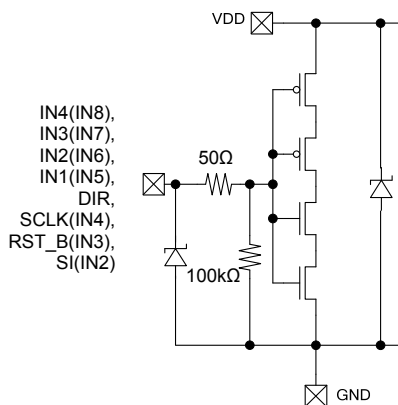
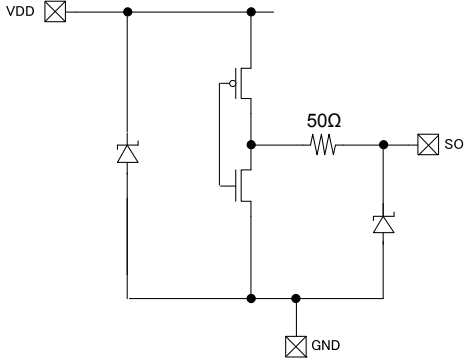
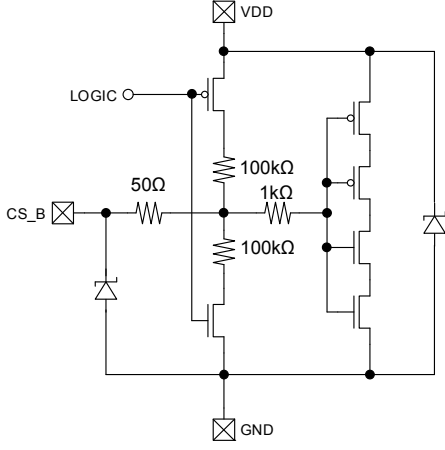


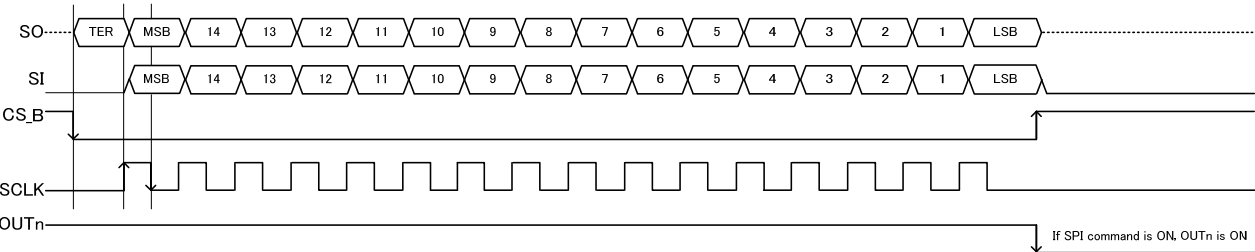
Figure 21. Timing Chart with inductive Load

I/O Equivalent Circuits

Pin	Symbol	I/O Equivalent Circuits
1,2, 11,12	GND	
3 to 10	OUT1 to OUT8	
13	VDD	
14 to 17 18 20 to 22	IN4(IN8), IN3(IN7), IN2(IN6), IN1(IN5), DIR, SCLK(IN4), RST_B(IN3), SI(IN2)	
19	SO	
23	CS_B	
24	VDDA	

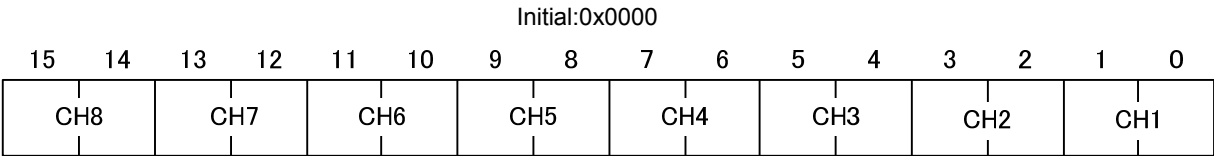
SPI mode

When CS_B=H,
SO Terminal become Hi-Z
When CS_B=L,
Internal state (TSD, OCP, OLD) is latched at falling edge of CS_B, and output to SO at rising edge of SCLK.
SI is taken in register at falling edge of SCLK.
Output corresponding to each resistor input is controlled at rising edge of CS_B.



Definitions of SI and SO signals are shown below.

SI signals



Bits	CHn	States of output and protective circuits			
		Output	OCP	TSD	OLD
15:14, 13:12, 11:10, 9:8, 7:6, 5:4, 3:2, 1:0	00	OFF	disable	disable	disable
	01	ON/OFF ^(Note 1)	enable/disable	enable/disable	disable/enable
	10	ON	enable	enable	disable
	11	OFF	disable	disable	enable

(Note 1) When INn=01, output is controlled by IN terminal.

Output controlled by each input is shown below.

Input	Controlled output
IN1(IN5)	OUT1
IN2(IN6)	OUT2
IN3(IN7)	OUT3
IN4(IN8)	OUT4
IN1(IN5)	OUT5
IN2(IN6)	OUT6
IN3(IN7)	OUT7
IN4(IN8)	OUT8

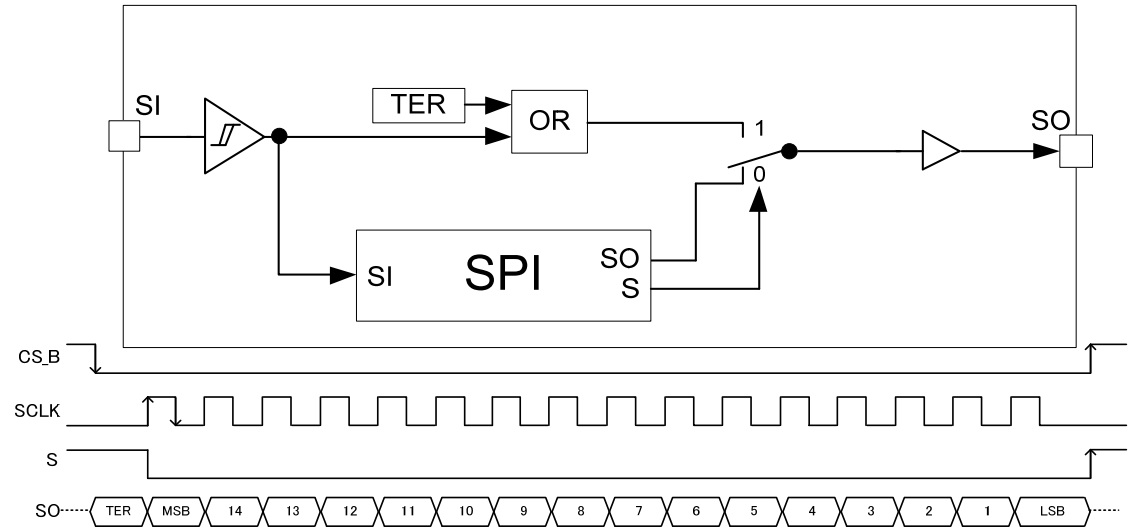
SO signals

When CS_B=H,
SO Terminal become Hi-Z
When CS_B=L,
Explanation of each Bit is shown below.

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TER	OL8	D8	OL7	D7	OL6	D6	OL5	D5	OL4	D4	OL3	D3	OL2	D2	OL1	D1
OUT8		OUT7		OUT6		OUT5		OUT4		OUT3		OUT2		OUT1		

Field	Bits	Data	STATE
TER	16 ^(Note 1)	0	Correspondence just after reset and normal operation
		1	Correspondence error of last time
OLn (n = 8 to 1)	15,13,11 9,7,5 3,1	0	Normal operation
		1	Load open
Dn (n = 8 to 1)	14,12 10,8,6 4,2,0	0	Normal operation
		1	OCD or TSD

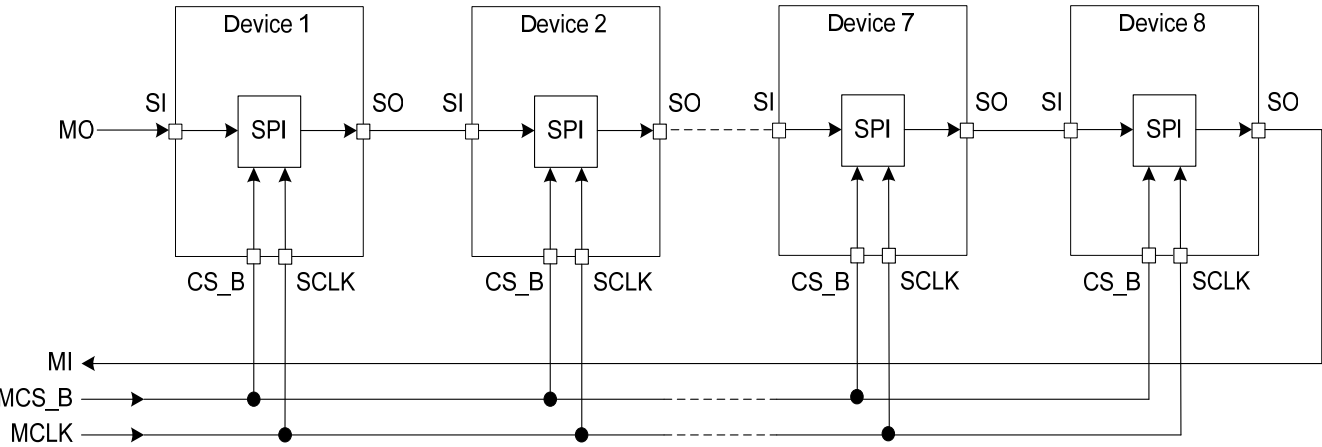
(Note 1) TER bit outputs logical sums of TER signal and input signal of this device with SI signal in the interval from fall of CS_B to rise of SCLK as shown below.
Block diagram and timing chart are shown below.



In order to select whether TER signal is output or SPI data output (OLn, Dn) signal is output, “S” signal is generated within IC and output is switched.

Seroal Daisy Chain

Plurality of devices can be connected as shown in the diagram below.
CS_B signal and SCLK signal connect common signal.
SI/SO line can connect SO of Device 1 to SI of Device 2 as shown in the diagram below.



Timing chart when 8 devices are connected is shown below.

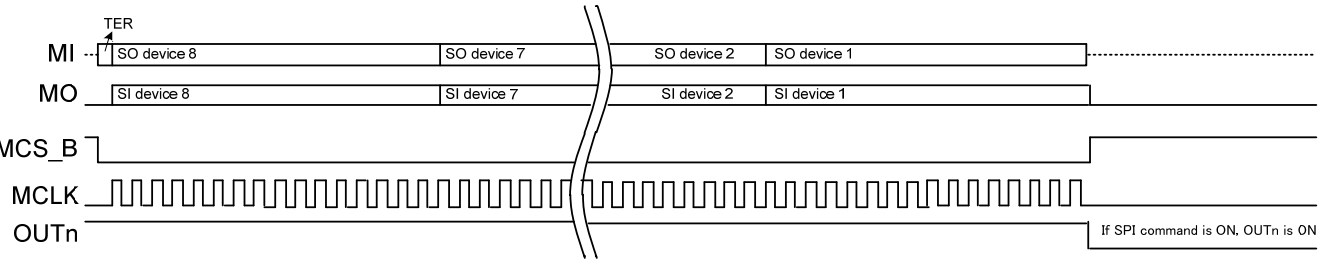
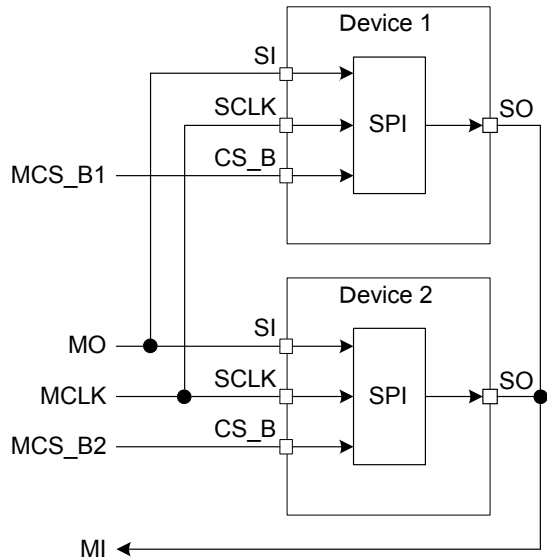


Figure 22. Timing chart when 8 devices are connected

Parallel Connection

Plurality of devices can be connected to parallel as shown in the diagram below.
SI signal, SCLK signal and SO signal connect common signal.
Each signal is necessary every each device for the CS_B signal.



Timing chart when 2 devices are connected is shown below.

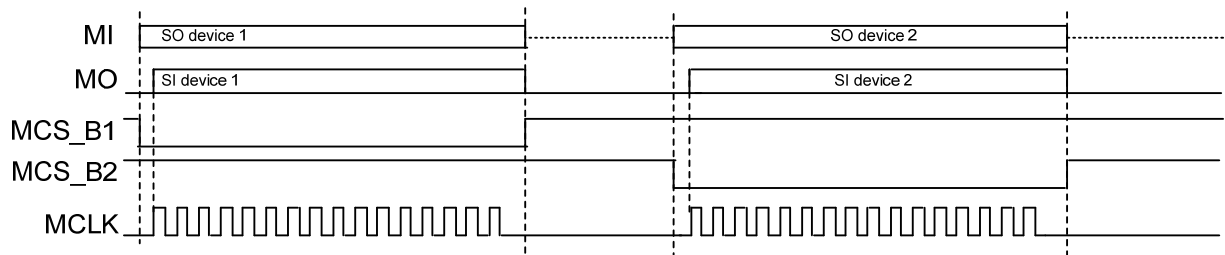


Figure 23. Timing chart when 2 devices are connected

SPI RST_B releasing sequence

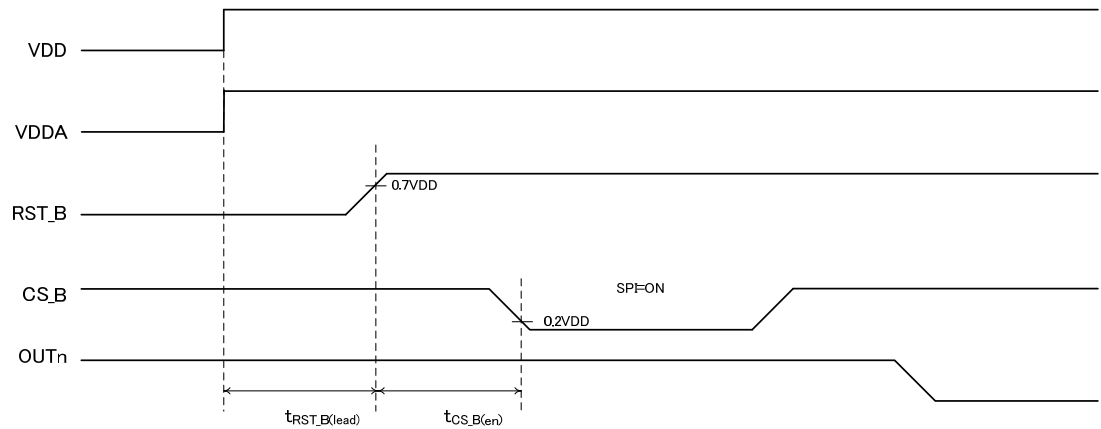


Figure 24. RST_B Releasing Sequence

Item	Symbol	Min	Typ	Max	Unit
RST_B lead time ^(Note 1) ^(Note 2)	t _{RST_B (lead)}	1	-	-	ms
CS_B enable time ^(Note 1)	t _{CS_B (en)}	10	-	-	μs

(Note 1) Not 100% tested
(Note 2) RST_B L time and H time must be over 10μs

SPI timing chart

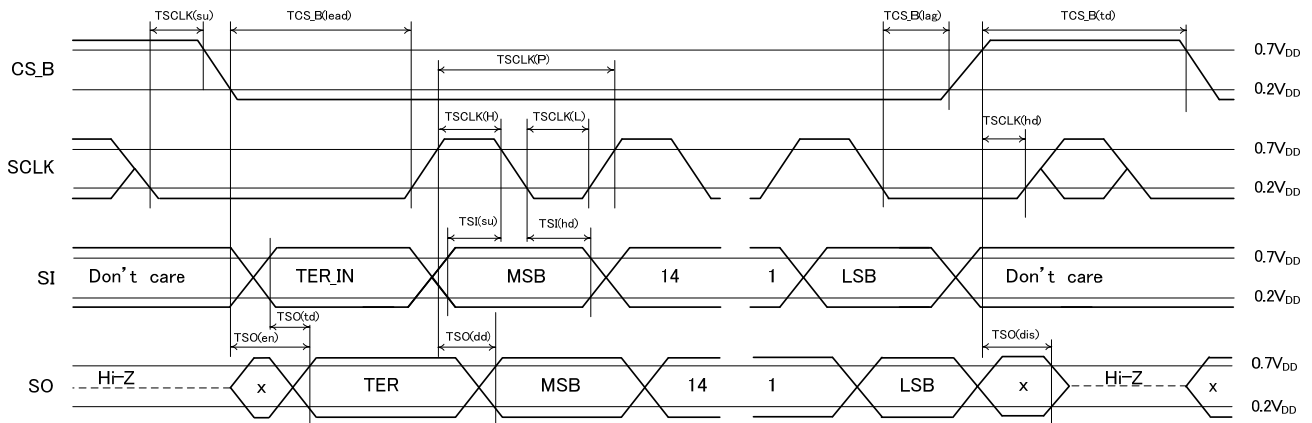
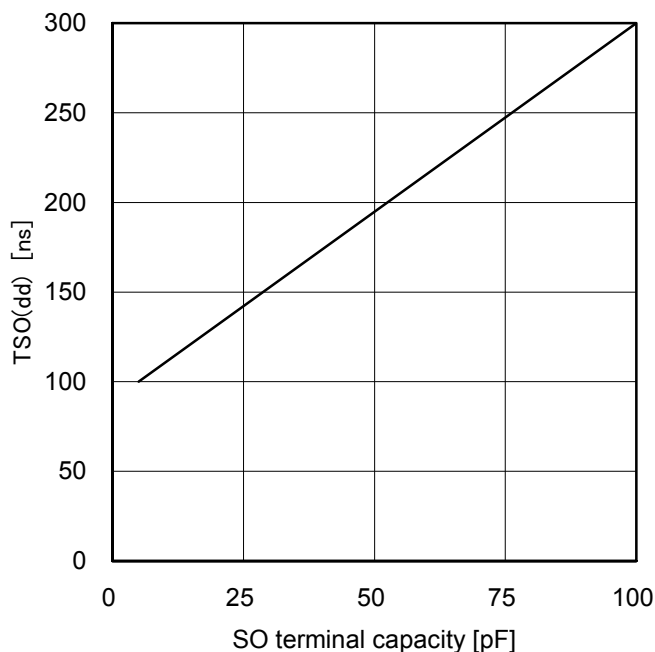
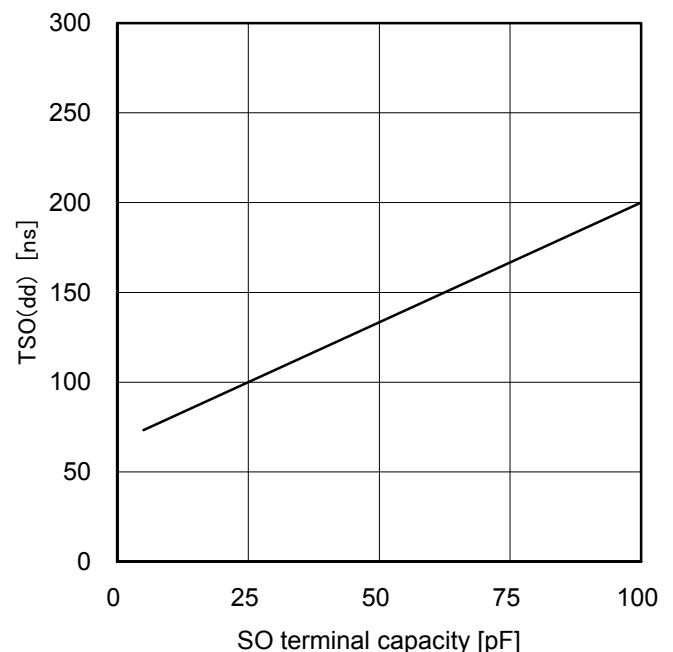


Figure 25. SPI Timing Chart

Item	Symbol	Min	Typ	Max	Unit
SCLK frequency	fSCLK	0	—	5	MHz
SCLK cycle length	TSCLK(P)	200	—	—	ns
SCLK high time	TSCLK(H)	50	—	—	ns
SCLK low time	TSCLK(L)	50	—	—	ns
SCLK setup time	TSCLK(su)	50	—	—	ns
SCLK hold time	TSCLK(hd)	50	—	—	ns
CS_B lead time	TCS_B(lead)	250	—	—	ns
CS_B lag time	TCS_B(lag)	250	—	—	ns
Transfer delay time	TCS_B(td)	250	—	—	ns
Data setup time	TSI(su)	20	—	—	ns
Data hold time	TSI(hd)	20	—	—	ns
SPI Output enable time ^(Note 1)	TSO(en)	—	—	200	ns
SPI Output disable time ^(Note 1)	TSO(dis)	—	—	250	ns
SPI Output Data delay time ^{(Note 1), (Note 2)}	TSO(dd)	—	—	100	ns
ERR Output Through delay time ^(Note 1)	TSO(td)	—	—	200	ns

(Note 1) Not 100% tested.

(Note 2) When SO terminal capacity=10pF, $3.0V \leq V_{DD} \leq 5.5V$. Refer to Figure 25 and Figure 26.Figure 26. Max of SPI Output Data delay time
($3.0V \leq V_{DD} < 4.5V$)Figure 27. Max of SPI Output Data delay time
($4.5V \leq V_{DD} \leq 5.5V$)

DIR (direct) mode

Transition to direct mode is brought about by switching DIR terminal to High.
Output controlled for each input is shown below.
Further, SPI input and RST_B input are not accepted during direct mode.

Input Pin	Controlled Output
CS_B(IN1)	OUT1
SI(IN2)	OUT2
RST_B(IN3)	OUT3
SCLK(IN4)	OUT4
IN1(IN5)	OUT5
IN2(IN6)	OUT6
IN3(IN7)	OUT7
IN4(IN8)	OUT8

DIR (direct) mode timing chart (1)

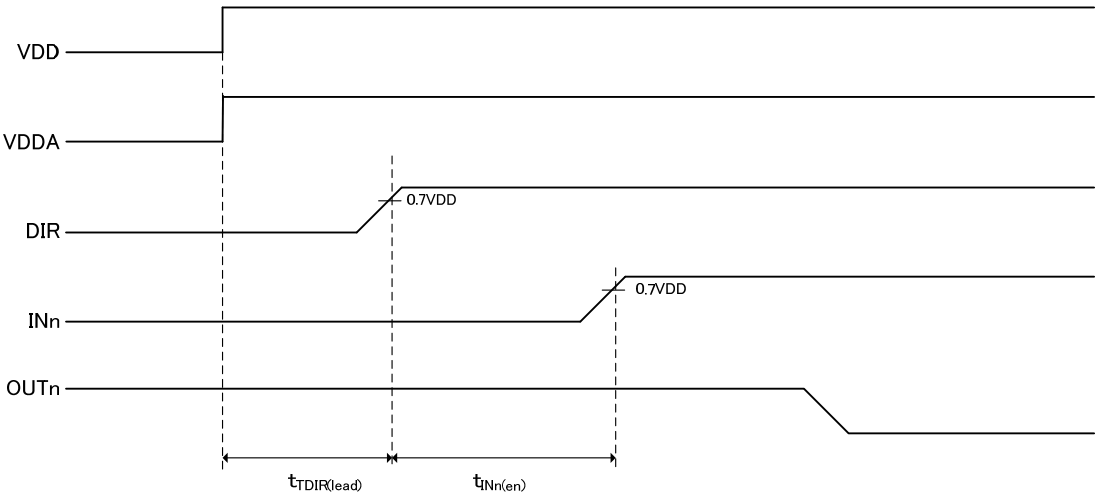


Figure 28. DIR Mode Timing Chart (1)

Item	Symbol	Min	Typ	Max	Unit
DIR lead time ^(Note 1)	t _{DIR(lead)}	1	-	-	ms
INn enable time ^(Note 1)	t _{INn(en)}	10	-	-	μs

(Note 1) Not 100% tested.

DIR (direct) mode timing chart (2)

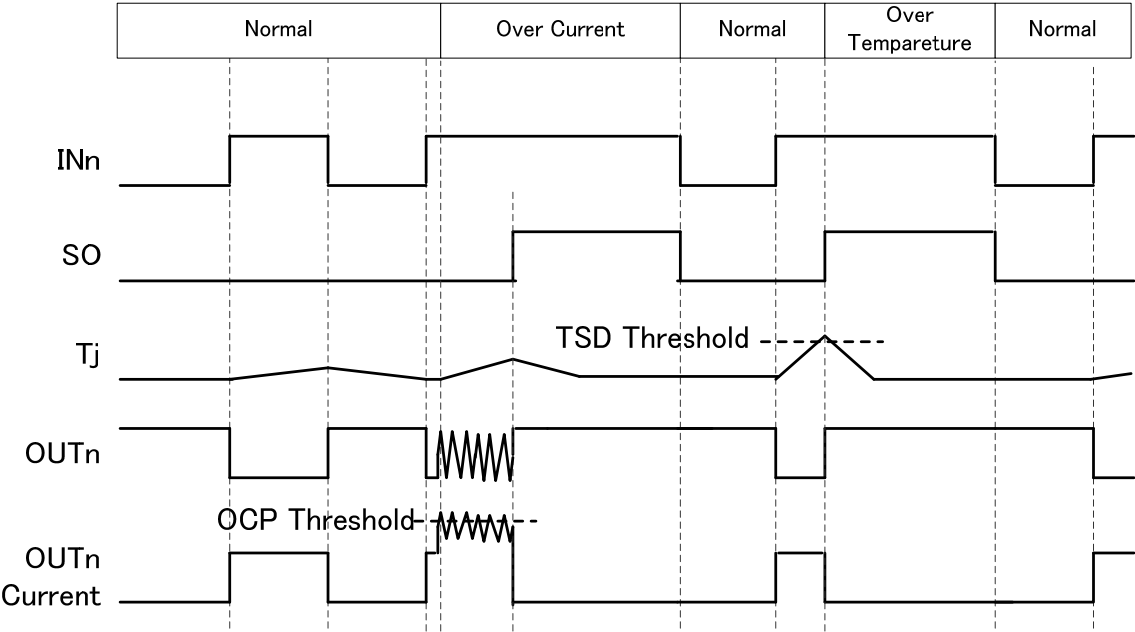


Figure 29. DIR Mode Timing Chart (2)

Direct mode operation current ($I_{DDA} + I_{DD}$) state transition

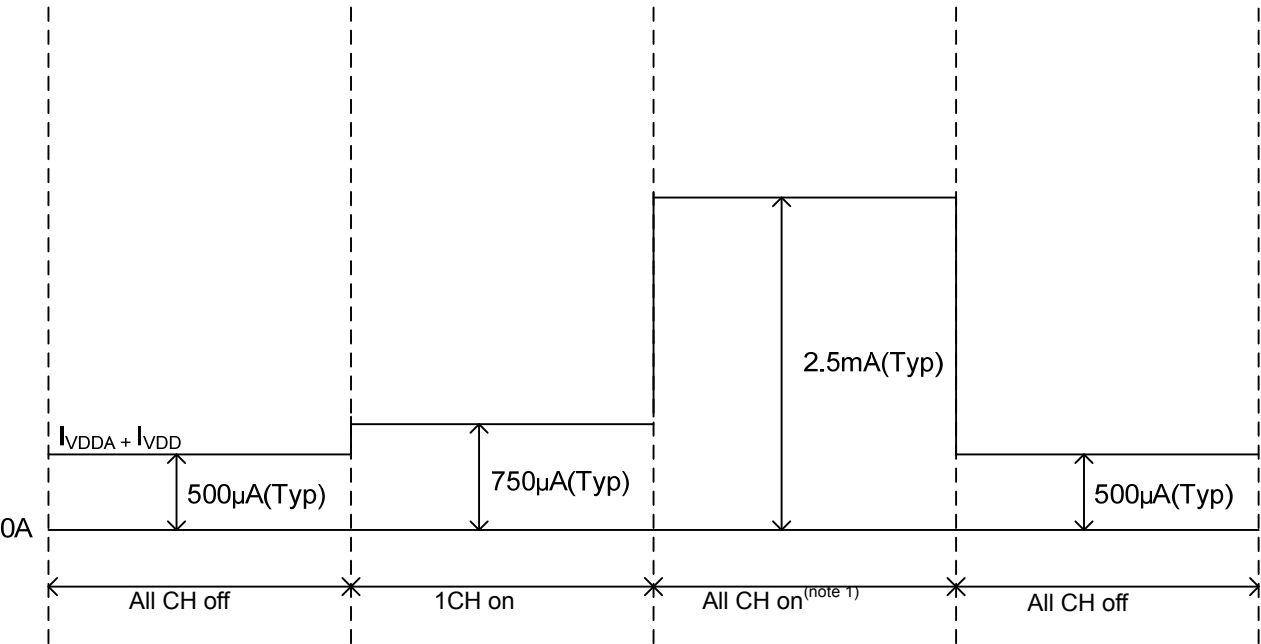


Figure 30. Operation Current State Transition Diagram

(Note 1) Sum of P.4 VDDA operation current (when all outputs are on) and VDD operation current (when all outputs are on).

Power source ON/OFF sequence

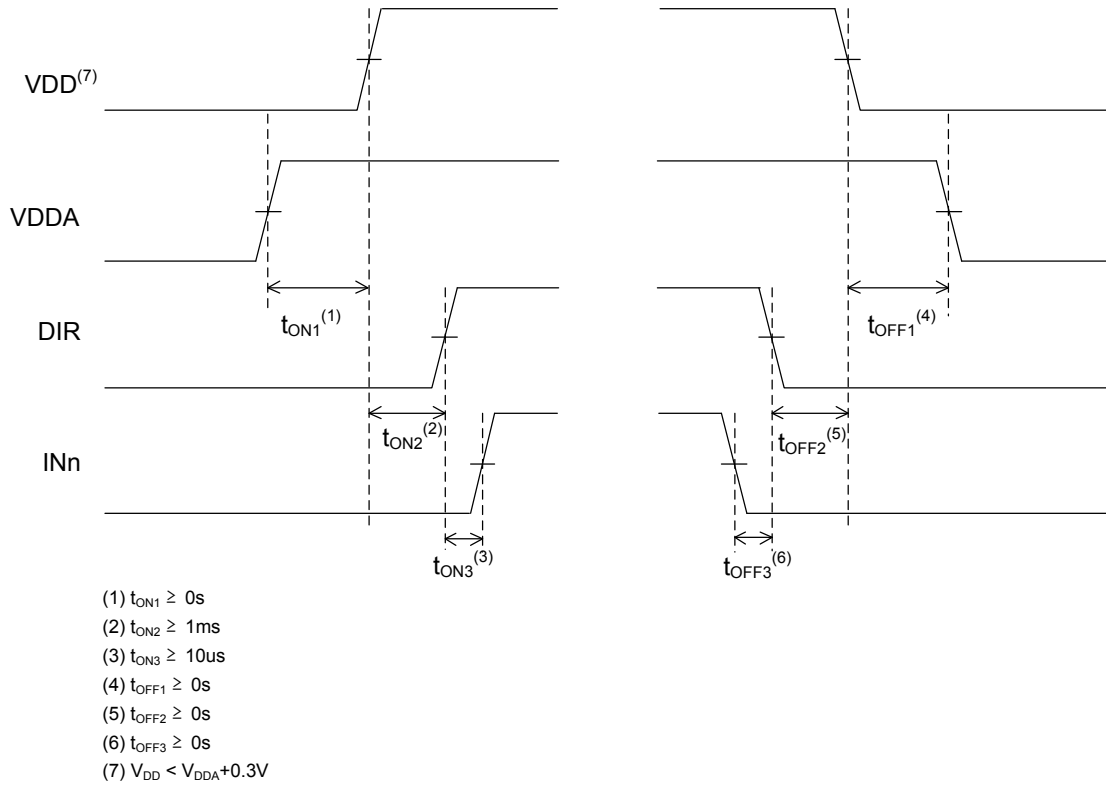


Figure 31. Power Source ON/OFF Sequence

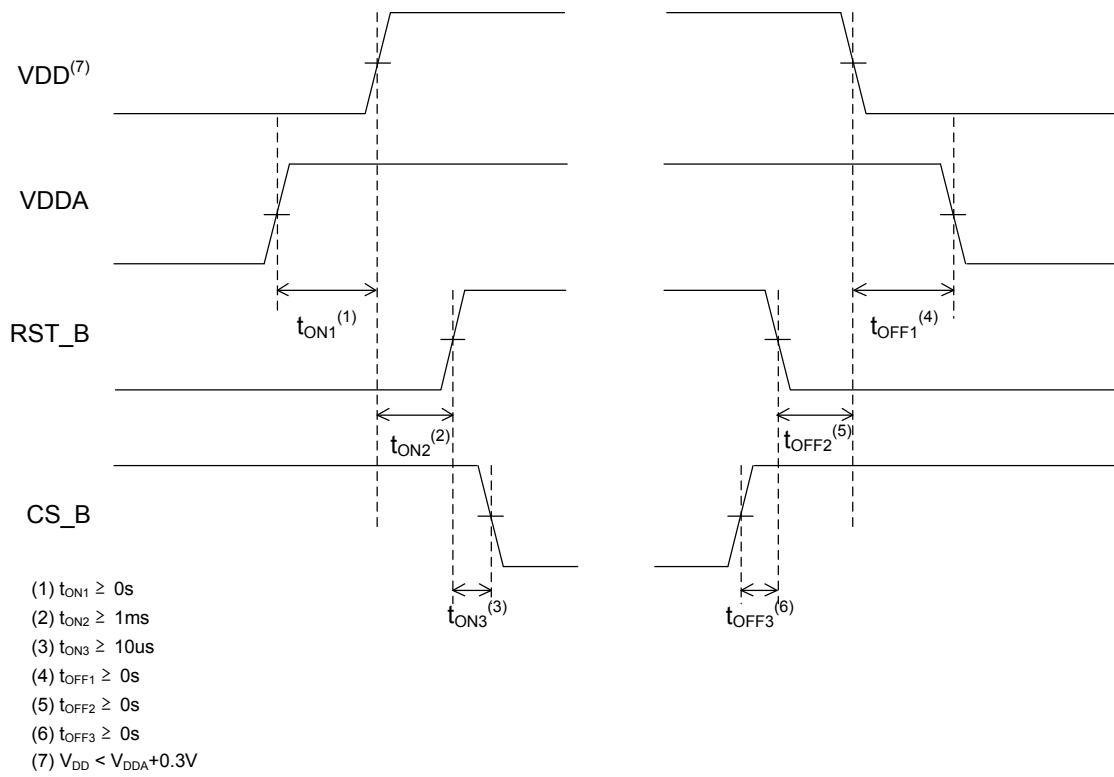


Figure 32. Power Source ON/OFF Sequence (SPI MODE)

Detection functions

① Overcurrent protection

When current of no less than 1.2A (Typ) is flown in output transistor of from OUT1 to OUT8 in 1000 μ s (Typ), the error flag is output. The error flag is released by OUTENn^(Note 1) becoming L^(Note 2).

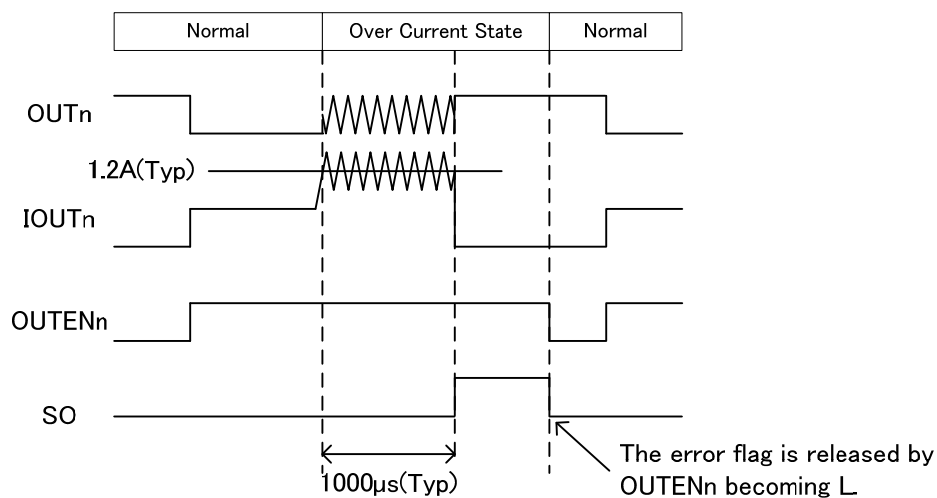


Figure 33. Overcurrent Protection Timing Chart

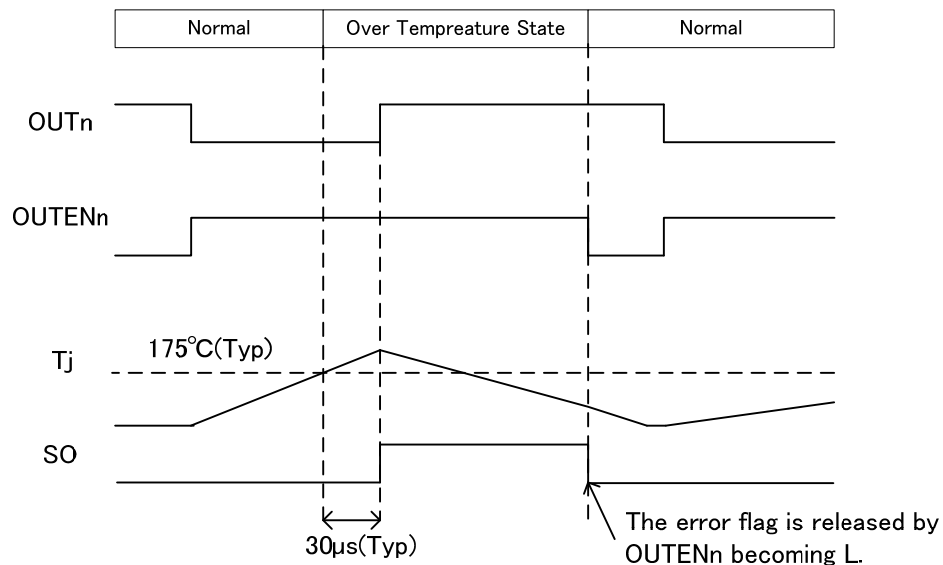
(Note 1) OUTENn shows the ON/OFF control signal of the OUT terminals. "n" shows the channel number.

(Note 2) The over current detection latch timer is cleared, and the error flag is not output when OUTENn become L before

Over current detection time(Typ:1000 μ s Max: 2200 μ s).

② Overheat protection

When T_j of from OUT1 to OUT8 reaches 175°C (Typ) or above and it passes for $30\mu\text{s}$ (Typ), output is turned off.
The error flag is released by OUTENn^(Note 1) becoming L^(Note 2).



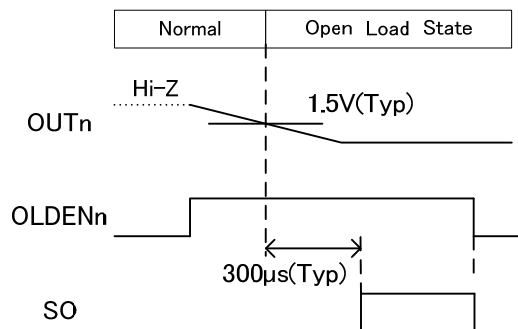
(Note 1) OUTENn shows the ON/OFF control signal of the OUT terminals. n shows the channel number.

(Note 2) The overheat detection latch timer is cleared, and the error flag is not output when OUTENn become L before
Overheat detection time(Typ:30μs Max: 65μs).

Figure 34. Overheat Protection Timing Chart

③ Open detection

In case of enable at Open detection function^(Note 3), when output voltage of from OUT1 to OUT8 falls below 1.5 V (Typ), open detection is detected and the error flag is output.



(Note 3) As for the DIR mode, OLDENn=H(open detection function becomes effective) in OUTENn =L.

$40\mu\text{A}$ (Typ) is flown from OUT to GND because $60\text{k}\Omega$ (Typ) is connected between OUT and GND.

As for the SPI mode, Please refer to Page 13.

"n" shows the channel number.

Figure 35. Open Detection Protection Timing Chart

Thermal resistance ^(Note 1)

Item	Symbol	Typ	Unit	Condition
HTSSOP-B24				
Junction-Ambient thermal resistance	θ_{JA}	42	°C / W	1s ^(Note 2)
		30	°C / W	2s ^(Note 3)
		23	°C / W	2s2p ^(Note 4)
Junction-Package upper side ^(Note 5) thermal characteristic parameter	Ψ_{JT}	4	°C / W	1s ^(Note 2)

(Note 1) Based on JESD51 - 2A (Still-Air), in case of 8ch ON state

(Note 2) Based on JESD51 - 3 FR4 114.3 mm x 76.2 mm x 1.57 mm 1 layer (1s)

(TOP Copper layer : ROHM original land pattern + wiring for measurement, copper thickness 2oz, copper area 600mm²)

(Note 3) Based on JESD51 -5 FR4 114.3 mm x 76.2 mm x 1.60 mm 2 layer(2s)

(TOP Copper layer : ROHM original land pattern + wiring for measurement, Bottom Copper area : 74.2 mm x 74.2 mm,

Copper thickness (Top and Bottom layers) 2oz)

(Note 4) Based on JESD51 -5 / -7 FR4 114.3 mm x 76.2 mm x 1.60 mm 4 layers (2s2p)

(TOP Copper layer : ROHM original land pattern + wiring for measurement / 2nd, 3rd, Bottom layer Copper area : 74.2 mm x 74.2 mm,

Copper thickness(Top and Bottom layers / Internal layers) 2oz / 1oz)

(Note 5) T_T : The central temperature on the surface of molding is measured.

① PCB Layout 1s

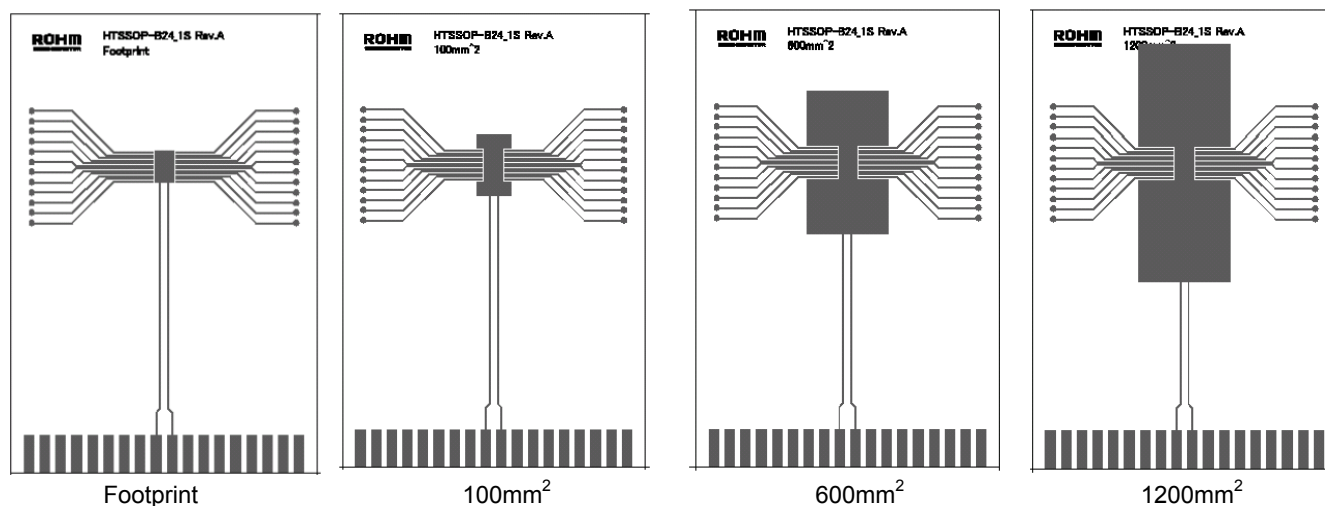


Figure 36. PCB Layout 1s

Dimension	Value
Board finish thickness	1.57 mm ± 10%
Board dimension	76.2 mm x 114.3 mm
Board material	FR4
Copper thickness (Top/Bottom layers)	0.070mm (Cu:2oz)
Heatsink copper area dimension	Footprint / 100mm ² / 600mm ² / 1200mm ²

② PCB Layout 2s

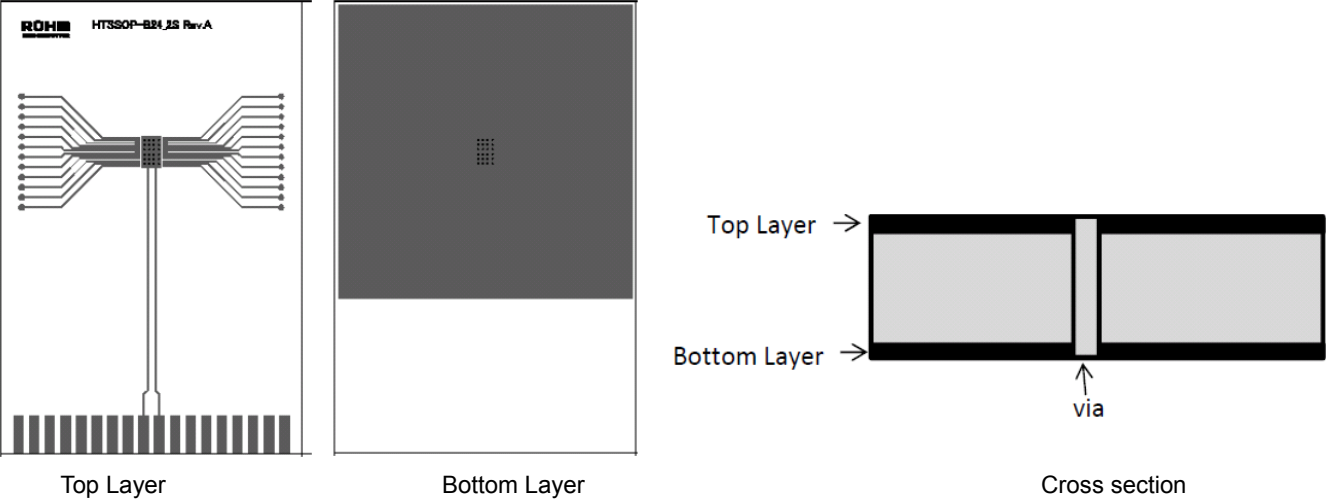


Figure 37. PCB Layout 2s

Dimension	Value
Board finish thickness	1.60 mm ± 10%
Board dimension	76.2 mm x 114.3 mm
Board material	FR4
Copper thickness (Top/Bottom layers)	0.070mm (Cu + Plating)
Therml vias separation / diameter	1.2mm / 0.3mm

③ PCB Layout 2s2p

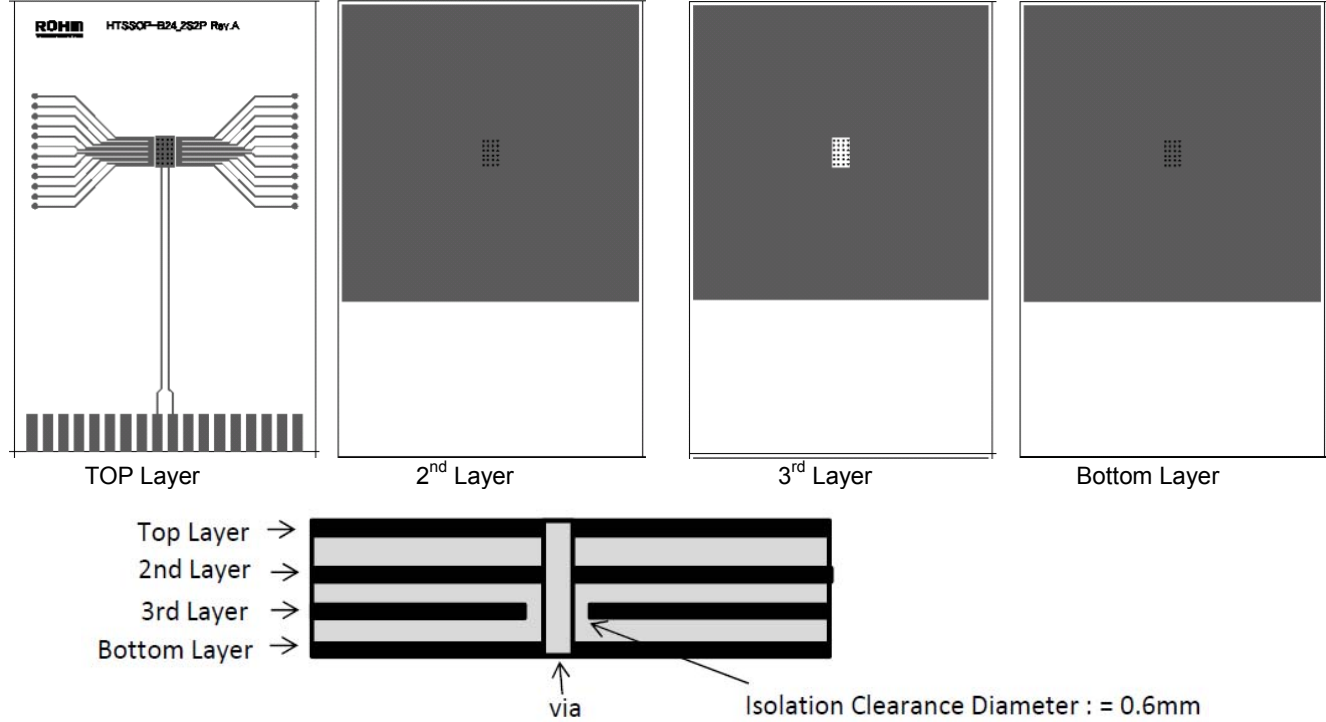


Figure 38. PCB Layout 2s2p

Dimension	Value
Board finish thickness	1.60 mm ± 10%
Board dimension	76.2 mm x 114.3 mm
Board material	FR4
Copper thickness (Top/Bottom layers)	0.070mm (Cu + Plating)
Copper thickness (Inner layers)	0.035mm
Therml vias separation / diameter	1.2mm / 0.3mm

④ Thermal impedance (Single pulse)

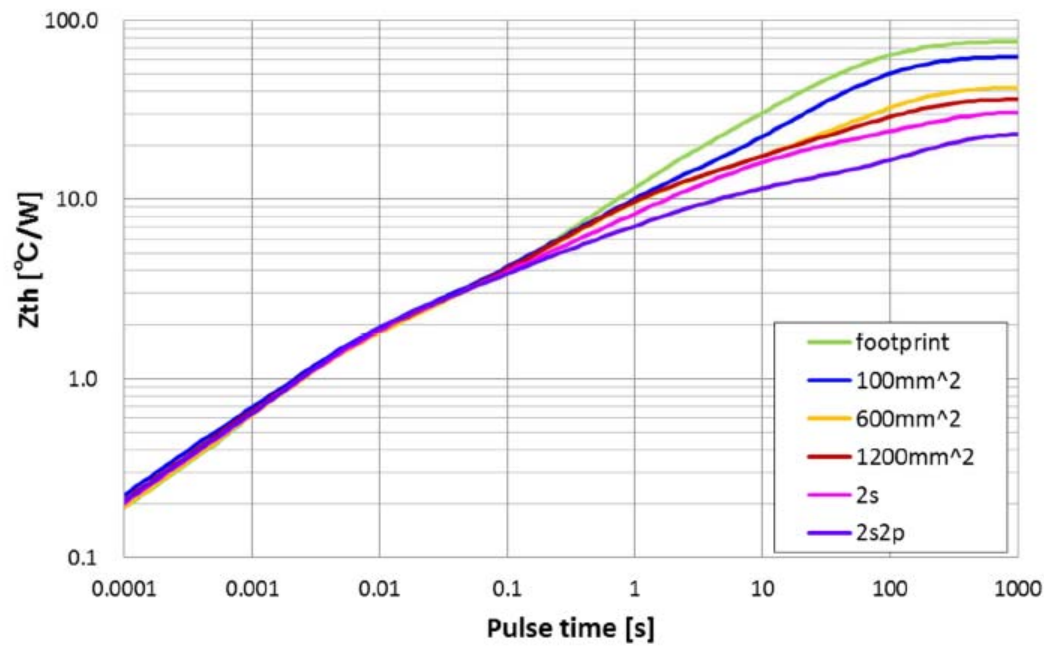


Figure 39. Thermal impedance

⑤ Thermal resistance (θ_{JA} / Ψ_{JT} vs PCB copper area - 1s)

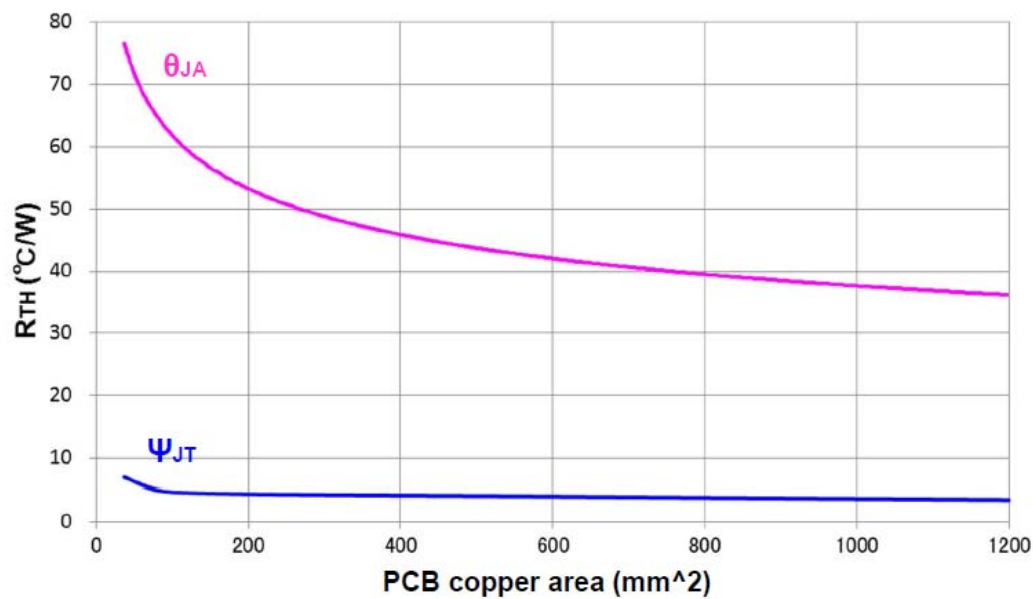


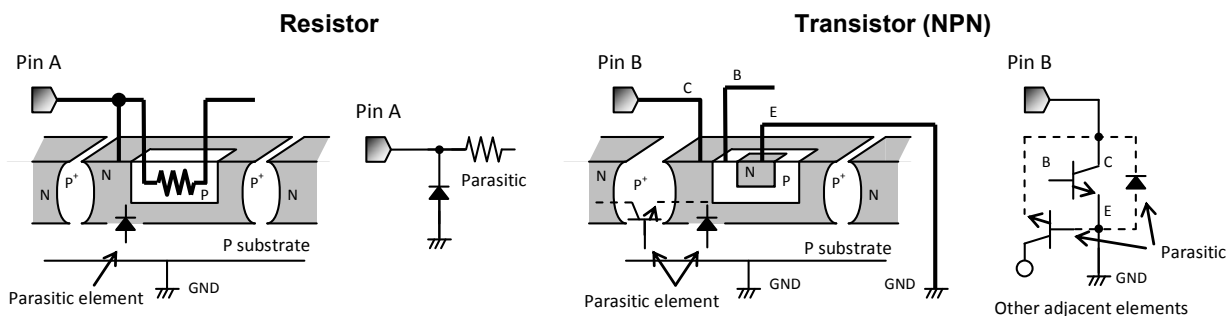
Figure 40. Thermal resistance

Operational Notes

- 1) **Absolute Maximum Ratings**
Operating the IC over the absolute maximum ratings may damage the IC. In addition, it is impossible to predict all destructive situations such as short-circuit modes or open circuit modes. Therefore, it is important to consider circuit protection measures, like adding a fuse, in case the IC is expected to be operated in a special mode exceeding the absolute maximum ratings.
- 2) **Reverse connection of power supply**
Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.
- 3) **Power supply lines**
Design the PCB layout pattern to provide low impedance ground and supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.
- 4) **GND Voltage**
The voltage of GND pin must be the lowest voltage of all pins of the IC at all operating conditions. Ensure that no pins are at a voltage below the ground pin at any time, even during transient condition.
- 5) **Thermal consideration**
Use a thermal design that allows for a sufficient margin by taking into account the permissible power dissipation (P_d) in actual operating conditions. Consider P_c that does not exceed P_d in actual operating conditions ($P_c \geq P_d$).
- 6) **Short between pins and mounting errors**
Be careful when mounting the IC on printed circuit boards. The IC may be damaged if it is mounted in a wrong orientation or if pins are shorted together. Short circuit may be caused by conductive particles caught between the pins.
- 7) **Operation Under Strong Electromagnetic Field**
Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.
- 8) **Thermal shutdown circuit (TSD)**
The IC incorporates a built-in thermal shutdown circuit, which is designed to turn off the IC when the internal temperature of the IC reaches 175°C (25°C hysteresis). It is not designed to protect the IC from damage or guarantee its operation. Do not continue to operate the IC after this function is activated. Do not use the IC in conditions where this function will always be activated.
- 9) **Over voltage protection (active clamp)**
There is a built-in over voltage protection circuit (active clamp) to absorb the induced current when inductive load is off (Power MOS = off). During active clamp and when $I_N=0V$, TSD will not function so keep IC temperature below 150°C.
- 10) **Over current protection circuit (OCP)**
The IC incorporates an over-current protection circuit that operates in accordance with the rated output capacity. This circuit protects the IC from damage when the load becomes shorted. It is also designed to limit the output current (without latching) in the event of more than 1.2A (typ) flow, such as from a large capacitor or other component connected to the output pin. This protection circuit is effective in preventing damage to the IC in cases of sudden and unexpected current surges. The IC should not be used in applications where the over current protection circuit will be activated continuously.
- 11) **Testing on application boards**
When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.
- 12) **Regarding input pins of the IC**
This monolithic IC contains P⁺ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When $GND > \text{Pin A}$ and $GND > \text{Pin B}$, the P-N junction operates as a parasitic diode.
 When $GND > \text{Pin B}$, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.



Example of monolithic IC structure

13) GND wiring pattern

When using both small-signal and large-current GND traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the GND traces of external components do not cause variations on the GND voltage. The power supply and ground lines must be as short and thick as possible to reduce line impedance.

14) Back electromotive force (BEMF)

There is a possibility that the BEMF is changed by using the operating condition, environment and the individual characteristics of motor. Please make sure there is no problem when operating the IC even though the BEMF is changed.

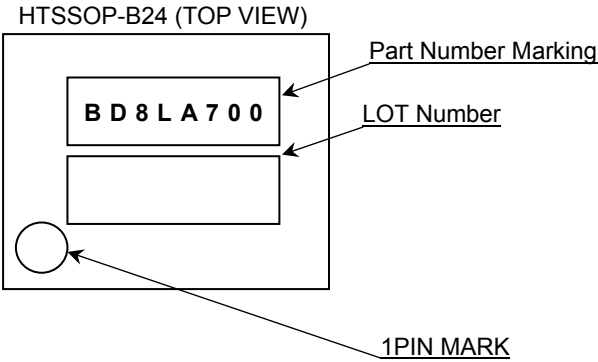
Ordering Information

B	D	8	L	A	7	0	0	E	F	V	-	CE2
---	---	---	---	---	---	---	---	---	---	---	---	-----

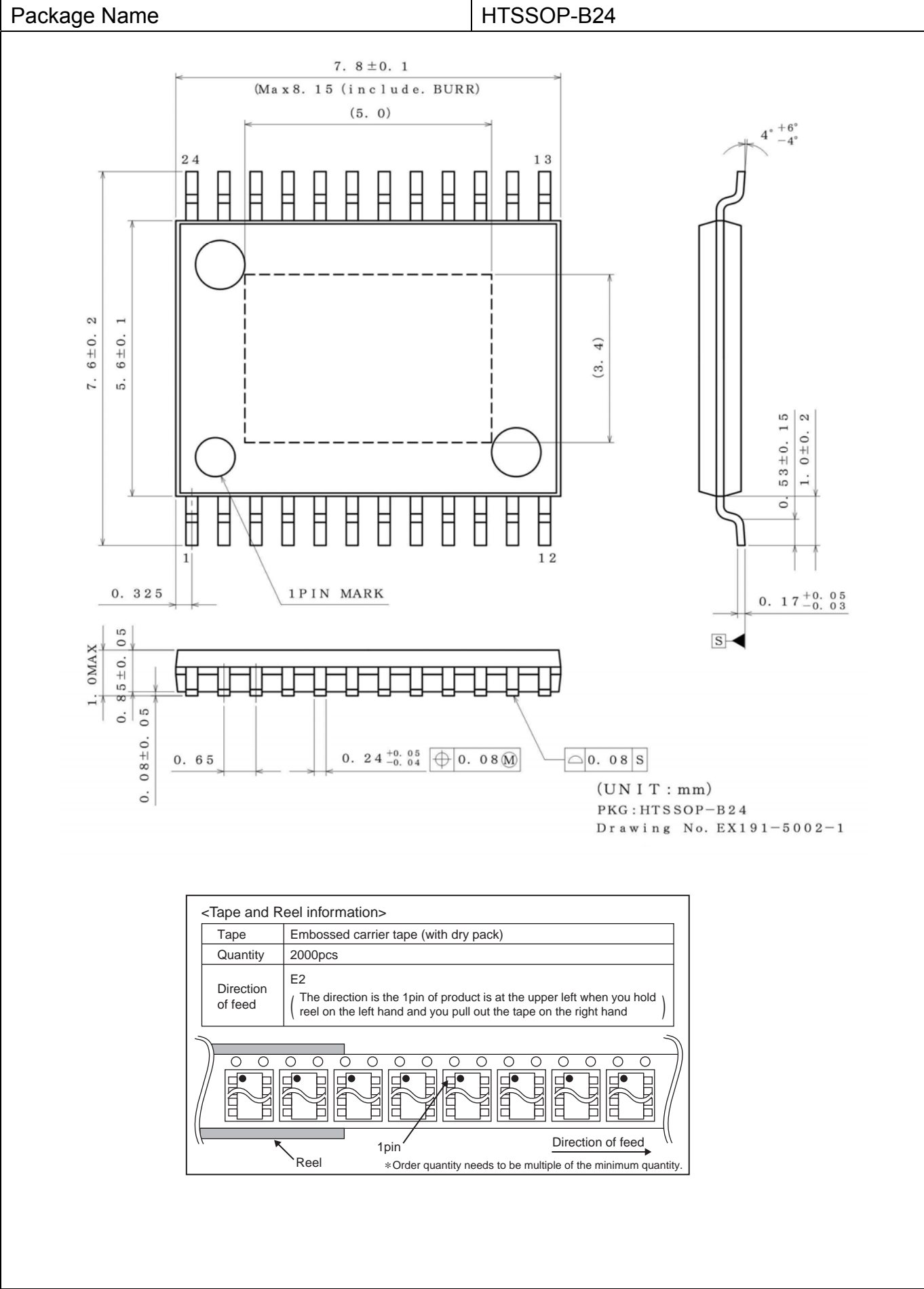
Package
EFV: HTSSOP-B24

Product Rank
C:for Automotive
Packaging Specification
E2:Embossed tape and reel

Marking Diagrams



Physical Dimension, Tape and Reel Information



Revision History

Date	Rev	Changes
16.Dec.2014	002	New Release
18.Aug.2015	003	<p>P.1 About "Feature", add a postscript to explanatory note of AEC-Q100.</p> <p>P.3 About "Absolute Maximum Ratings", add a postscript to explanatory note of Active Clamp Energy(repetitive).</p> <p>P.4 About "Output Sink Current", change the limit values of Typ & Max.</p> <p>P.4 About "Output Sink Current" & "Output Leak Current, add a postscript to V_{DIR} condition.</p> <p>P.12 About "I/O Equivalent Circuits", add a postscript to pull-down resistance of input terminal.</p>
23.May.2016	004	<p>P4 About name of Electrical Characteristics items, correct following name. Before: Output sink current ($I_{L(OFF)}$) After: Output leak current($I_{L(OFF)}$)</p> <p>About Output leak current (Open load detected), correct the limit values.</p> <p>P17 About Figure26., correct V_{DD} condition.</p> <p>P22 About Open detection Note of Detection functions, add an explanatory note.</p> <p>P26 About Operational Notes, correct No.5. About Operational Notes, correct No.10.</p> <p>P27 About Ordering Information, correct Package information.</p>

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JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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8. Confirm that operation temperature is within the specified range described in the product specification.
9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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 - [d] the Products are exposed to high Electrostatic
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