# SGM61330
# 3.8V to 36V Input, 3A, Synchronous Buck Converter

## GENERAL DESCRIPTION

The SGM61330 is internally compensated, synchronous Buck converter with a wide 3.8V to 36V input voltage range and 3A output current capability. This device can be easily used in various industrial applications powered from unregulated sources. Easy compensation and cycle-by-cycle current limit are obtained by peak current mode control. With 29μA (TYP) quiescent current and ultra-low 2.1μA (TYP) shutdown current, it is well suited for battery powered systems to prolong battery life. Internal compensation allows quick and low component count design.

The SGM61330 can operate at fixed frequency with moderate or heavy load condition. In light load condition, it enters in the pulse frequency modulation (PFM) mode to improve high efficiency.

The EN employs an enable divider to establish a precision threshold that simplifies UVLO adjustment, device on/off control and power sequencing. Thermal shutdown and output short-circuit protection (hiccup mode) are also provided.

The SGM61330 is available in Green TQFN-2×3-12AL and SOIC-8 (Exposed Pad) packages.

## FEATURES

- **Wide 3.8V to 36V Input Voltage Range**
- **Up to 3A Continuous Output Current**
- **SGM61330:**
  - **1V to 24V Output Voltage Range**
  - **PFM at Light Load Condition**
- **Fixed Switching Frequency**
  - **SGM61330A: 400kHz**
  - **SGM61330B: 1.4MHz**
  - **SGM61330C: 2.1MHz**
- **Power-Good Flag and Precision Enable**
- **Integrated $R_{DSON}$ Switches:**
  - **TQFN-2×3-12AL: 65mΩ/42mΩ (TYP)**
  - **SOIC-8 (Exposed Pad): 78mΩ/55mΩ (TYP)**
- **High Efficiency at Light Load Condition**
- **Ultra-Low Shutdown Current: 2.1μA (TYP)**
- **Low Quiescent Current: 29μA (TYP)**
- **Peak Current Mode Control**
- **Cycle-by-Cycle Current Limit**
- **4ms (TYP) Internal Soft-Start Time**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in Green TQFN-2×3-12AL and SOIC-8 (Exposed Pad) Packages**

## APPLICATIONS

Industrial Power Supplies
Telecom and Datacom Systems
General Purpose Wide $V_{IN}$ Regulation

## TYPICAL APPLICATION

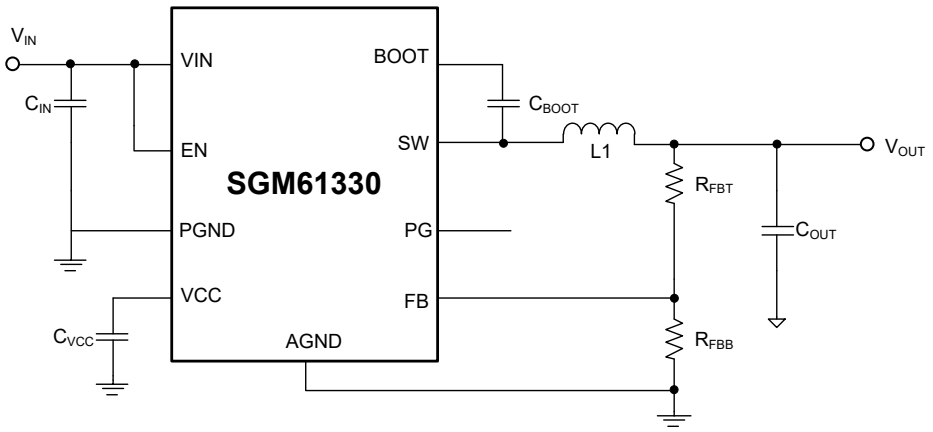


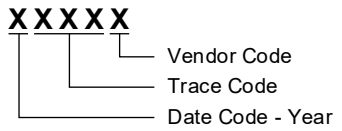

**Figure 1. Typical Application Circuit**

# PACKAGE/ORDERING INFORMATION

| MODEL | PACKAGE DESCRIPTION | SPECIFIED TEMPERATURE RANGE | ORDERING NUMBER | PACKAGE MARKING | PACKING OPTION |
|---|---|---|---|---|---|
| SGM61330A | SOIC-8 (Exposed Pad) | -40℃ to +125℃ | SGM61330AXPS8G/TR | SGM<br>04LXPS8<br>XXXXX | Tape and Reel, 4000 |
| | TQFN-2×3-12AL | -40℃ to +125℃ | SGM61330AXTST12G/TR | 04NST<br>XXXXX | Tape and Reel, 3000 |
| SGM61330B | SOIC-8 (Exposed Pad) | -40℃ to +125℃ | SGM61330BXPS8G/TR | SGM<br>0BQXPS8<br>XXXXX | Tape and Reel, 4000 |
| | TQFN-2×3-12AL | -40℃ to +125℃ | SGM61330BXTST12G/TR | 04PST<br>XXXXX | Tape and Reel, 3000 |
| SGM61330C | SOIC-8 (Exposed Pad) | -40℃ to +125℃ | SGM61330CXPS8G/TR | SGM<br>04MXPS8<br>XXXXX | Tape and Reel, 4000 |
| | TQFN-2×3-12AL | -40℃ to +125℃ | SGM61330CXTST12G/TR | 0BPST<br>XXXXX | Tape and Reel, 3000 |

## MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.




Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

## ABSOLUTE MAXIMUM RATINGS

Input Voltages:
- VIN to PGND ..... -0.3V to 42V
- EN to AGND ..... -0.3V to $V_{IN}$ + 0.3V
- EN to AGND (Less than 10ns Transients) ..... -5V to $V_{IN}$ + 0.3V
- FB to AGND ..... -0.3V to 4.5V
- AGND to PGND ..... -0.3V to 0.3V

Output Voltages:
- SW to PGND ..... -0.3V to $V_{IN}$ + 0.3V
- SW to PGND (Less than 10ns Transients) ..... -5V to 42V
- BOOT to SW ..... -0.3V to 5.5V
- VCC to AGND ..... -0.3V to 5.5V

Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM ..... TBDV
CDM ..... TBDV

## RECOMMENDED OPERATING CONDITIONS

Input Voltages:
- VIN to PGND ..... 3.8V to 36V
- EN to AGND ..... 0V to 36V
- FB to AGND ..... -0.3V to 1.2V

Output Voltage Range ..... 1V to 24V
Output Current Range ..... 0A to 3A
Operating Ambient Temperature Range ..... -40℃ to +125℃
Operating Junction Temperature Range ..... -40℃ to +125℃

## OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

## ESD SENSITIVITY CAUTION

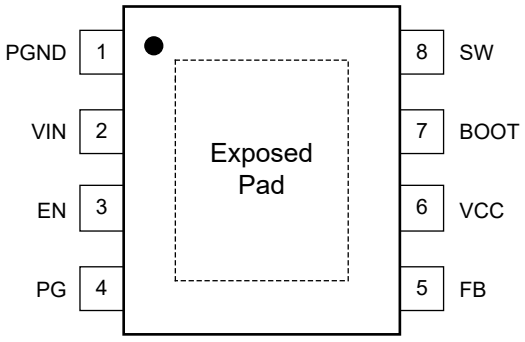
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

## DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

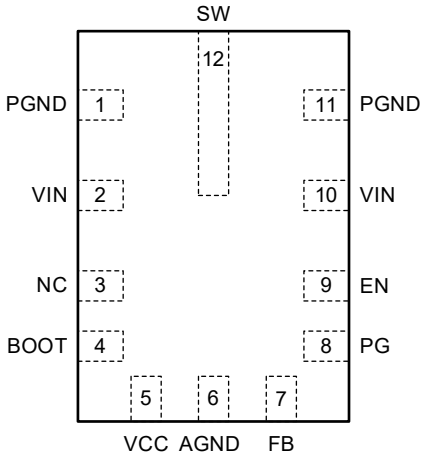
## PIN CONFIGURATIONS

(TOP VIEW)




SOIC-8 (Exposed Pad)

(TOP VIEW)




TQFN-2×3-12AL

## PIN DESCRIPTION

| PIN | | | | FUNCTION |
|---|---|---|---|---|
| SOIC-8 (Exposed Pad) | TQFN-2×3-12AL | NAME | TYPE (1) | |
| 1 | 1, 11 | PGND | G | Power Ground. It is internally connected to converter return. Returns of the $C_{IN}$ and $C_{OUT}$ capacitors should be connected close to this pin. Connect to system ground, exposed pad and AGND together. |
| 2 | 2, 10 | VIN | P | Power Supply Input Pin. Connect $C_{IN}$ as close as possible between this pin and PGND pin. |
| 3 | 9 | EN | A | Active High Enable Input. Do not float.<br>EN: This pin can be connected to VIN pin via a resistor if the shutdown feature is not required or to a resistor divider to adjust UVLO threshold. |
| 4 | 8 | PG | A | Open-Drain Power Good Flag Output. Connect to suitable voltage supply through a current limiting resistor. High = power ok, Low = power bad. Flag pulls low when EN = Low. Can be left open when not used. |
| 5 | 7 | FB | A | Feedback Input. Connect the midpoint of the feedback resistor divider. |
| 6 | 5 | VCC | P | LDO (Internal Bias) Output. This pin is provided for bypassing to AGND only. Never load VCC. |
| 7 | 4 | BOOT | P | Bootstrap Input. Bootstrap supply for high-side driver. Connect a 100nF ceramic capacitor between BOOT and SW pins. |
| 8 | 12 | SW | P | Switching Node Output. Switching node of the internal synchronous Buck converter with N-MOSFET switches. Connect to the output inductor and bootstrap capacitor. |
| - | 6 | AGND | G | Analog Ground. Reference for internal analog signals and logic. Connect it to system ground. |
| - | 3 | NC | - | On the TQFN package, connect the SW pin to NC on the PCB. This simplifies the connection from the $C_{BOOT}$ capacitor to the SW pin. This pin has no internal connection to the regulator. |
| - | - | Exposed Pad | G | Thermal Exposed Pad. Must be connected to ground plane on PCB. It is the main thermal relief path for the die. |

NOTE: 1. A = analog, P = power, G = ground.

# ELECTRICAL CHARACTERISTICS

($V_{IN}$ = 12V, $T_J$ = -40℃ to +125℃, typical values are at $T_J$ = +25℃, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Power Supply** | | | | | | |
| Input Voltage Range | $V_{IN}$ | | 3.8 | | 36 | V |
| Input UVLO Rising Threshold | $V_{IN\_UVLO\_H}$ | Rising threshold | | 3.66 | | V |
| | $V_{IN\_UVLO\_L}$ | Falling threshold | | 3.12 | | |
| Input UVLO Hysteresis | $V_{UVLO\_HYS}$ | Falling hysteresis | | 540 | | mV |
| Shutdown Current into VIN | $I_{SHDN}$ | $V_{EN}$ = 0V | | 2.1 | | μA |
| Quiescent Current into VIN | $I_Q$ | $V_{IN}$ = 12V, $V_{FB}$ = 1.2V, PFM mode, Non-switching | | 29 | | μA |
| **Enable** | | | | | | |
| EN Input Level Required to Turn On Internal LDO | $V_{EN\text{-}VCC\_H}$ | | | 0.72 | | V |
| EN Input Level Required to Turn Off Internal LDO | $V_{EN\text{-}VCC\_L}$ | | | 0.64 | | V |
| EN Input Level Required to Start Switching | $V_{EN\_H}$ | Rising threshold | | 1.233 | | V |
| Enable Hysteresis | $V_{EN\_HYS}$ | | | 100 | | mV |
| Input Leakage Current at EN Pin | $I_{EN}$ | $V_{EN}$ = 4V | | 4 | | nA |
| **Voltage Reference** | | | | | | |
| Reference Voltage | $V_{REF}$ | $V_{IN}$ = 6V to 36V | | 1 | | V |
| Input Leakage Current at FB Pin | $I_{LKG\_FB}$ | $V_{FB}$ = 1V | | 2.5 | | nA |
| **Internal LDO** | | | | | | |
| Internal LDO Output Voltage | $V_{CC}$ | $V_{IN}$ = 6V to 36V | | 5.0 | | V |
| Bootstrap Voltage Under-Voltage Lock-Out Threshold (1) | $V_{BOOT\_UVLO\_H}$ | Rising threshold | | 2.91 | | V |
| | $V_{BOOT\_UVLO\_L}$ | Falling threshold | | 2.42 | | |
| **Integrated MOSFETs** | | | | | | |
| High-side MOSFET On-Resistance | $R_{DSON\_HS}$ | $V_{IN}$ = 12V, $I_{OUT}$ = 0.8A, in TQFN package | | 65 | | mΩ |
| | | $V_{IN}$ = 12V, $I_{OUT}$ = 0.8A, in SOIC package | | 78 | | |
| Low-side MOSFET On-Resistance | $R_{DSON\_LS}$ | $V_{IN}$ = 12V, $I_{OUT}$ = 0.8A, in TQFN package | | 42 | | mΩ |
| | | $V_{IN}$ = 12V, $I_{OUT}$ = 0.8A, in SOIC package | | 55 | | |
| **Current Limit** | | | | | | |
| Peak Inductor Current Limit | $I_{HS\_LIMIT}$ | $T_J$ = +25℃ | | 4.5 | | A |
| Valley Inductor Current Limit | $I_{LS\_LIMIT}$ | $T_J$ = +25℃ | | 3.5 | | A |
| Minimum Peak Inductor Current (1) | $I_{PEAK\_MIN}$ | | | 0.5 | | A |
| Zero Cross Current Limit (1) | $I_{L\_ZC}$ | | | 0.05 | | A |
| **Hiccup Mode** | | | | | | |
| Number of Cycles that HS Current Limit is Tripped to Enter Hiccup Mode (1) | $N_{OC}$ | | | 32 | | Cycles |
| Hiccup Retry Delay Time (1) | $t_{OC}$ | | | 80 | | ms |
| **Soft-Start** | | | | | | |
| Internal Soft-Start Time | $t_{SS}$ | The time of internal reference to increase from 0V to 0.8V. | | 4 | | ms |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{IN}$ = 12V, $T_J$ = -40℃ to +125℃, typical values are at $T_J$ = +25℃, unless otherwise noted.)

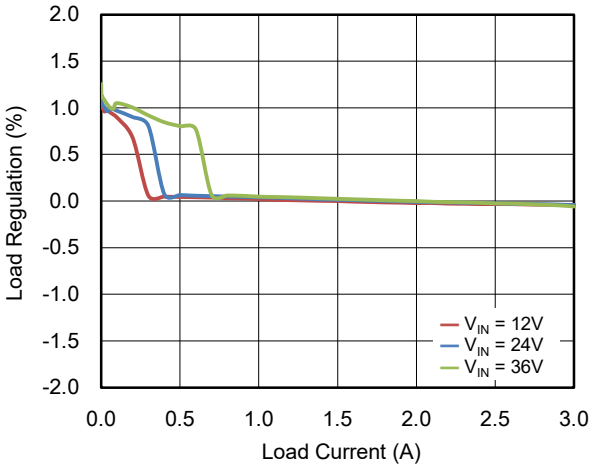
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Power Good (PG Pin)** | | | | | | |
| Power-Good Upper Threshold - Rising | $V_{PG\_HIGH\_UP}$ | % of FB voltage | | 108% | | |
| Power-Good Upper Threshold - Falling | $V_{PG\_HIGH\_DN}$ | % of FB voltage | | 105% | | |
| Power-Good Lower Threshold - Rising | $V_{PG\_LOW\_UP}$ | % of FB voltage | | 95% | | |
| Power-Good Lower Threshold - Falling | $V_{PG\_LOW\_DN}$ | % of FB voltage | | 92% | | |
| Power-Good Glitch Filter Delay | $t_{PG\_RISE}$ | | | 133 | | μs |
| | $t_{PG\_FALL}$ | | | 118 | | |
| Power-Good Flag $R_{DSON}$ $V_{PG\_HIGH\_UP}$ | $R_{PG}$ | $V_{IN}$ = 12V, $V_{EN}$ = 4V | | 40 | | Ω |
| | | $V_{EN}$ = 0V | | 40 | | |
| Minimum Input Voltage for Proper PG Function | $V_{IN\_PG}$ | 50μA, EN = 0V | | 0.83 | | V |
| PG Logic Low Output | $V_{PG}$ | 50μA, EN = 0V, $V_{IN}$ = 2V | | 0.002 | | V |
| Maximum Switch Duty Cycle | $D_{MAX}$ | | | 98.5% | | |
| **SW (SW Pin)** | | | | | | |
| Switching Frequency | $f_{SW}$ | SGM61330A | | 400 | | kHz |
| | | SGM61330B | | 1.4 | | MHz |
| | | SGM61330C | | 2.1 | | MHz |
| Minimum Turn-On Time (1) | $t_{ON\_MIN}$ | In TQFN package | | 75 | | ns |
| | | In SOIC package | | 75 | | |
| Minimum Turn-Off Time (1) | $t_{OFF\_MIN}$ | In TQFN package | | 90 | | ns |
| | | In SOIC package | | 90 | | |
| **Thermal Shutdown** | | | | | | |
| Thermal Shutdown Threshold | $T_{SHDN}$ | | | 165 | | ℃ |
| Thermal Shutdown Hysteresis | $T_{HYS}$ | | | 15 | | ℃ |

NOTE: 1. Guaranteed by design.

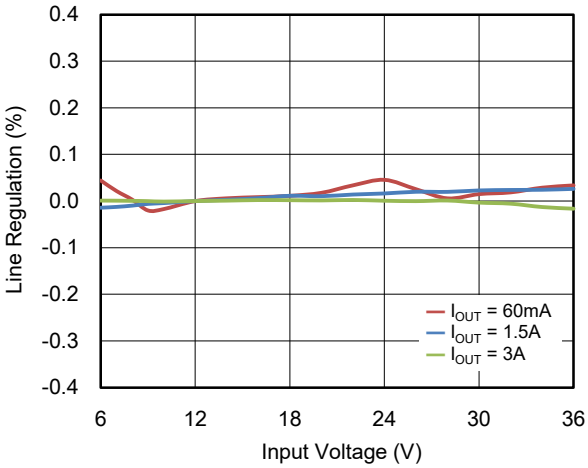
## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN}$ = 12V, $f_{SW}$ = 400kHz, L = 8.2μH, $C_{OUT}$ = 88μF, $T_A$ = 25℃, unless otherwise noted.

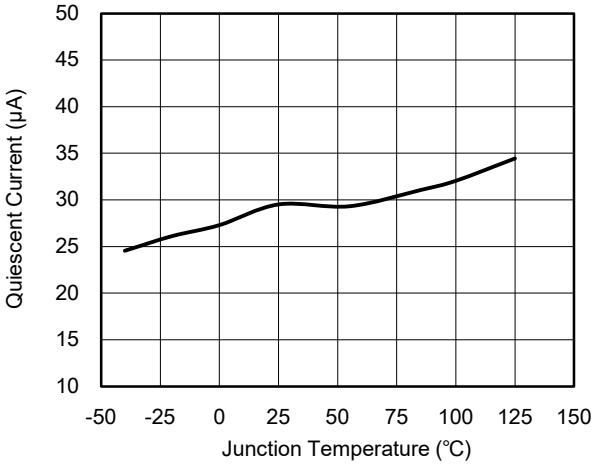
Load Regulation



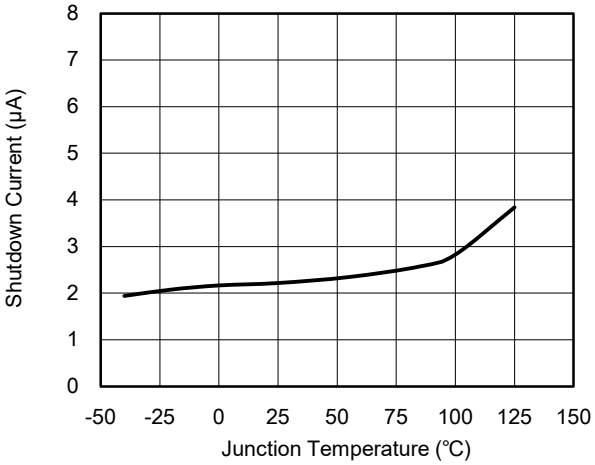

Line Regulation



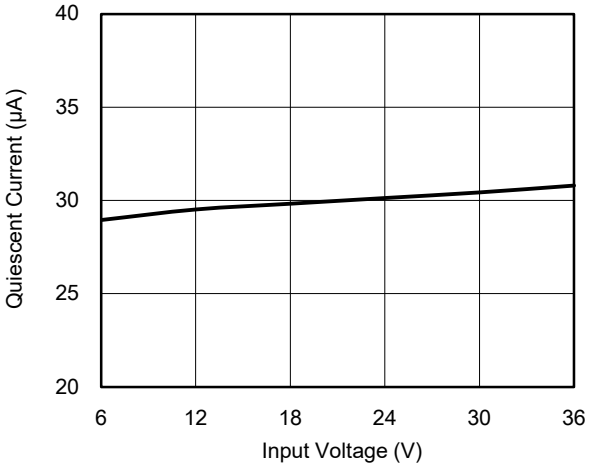

Quiescent Current vs. Junction Temperature



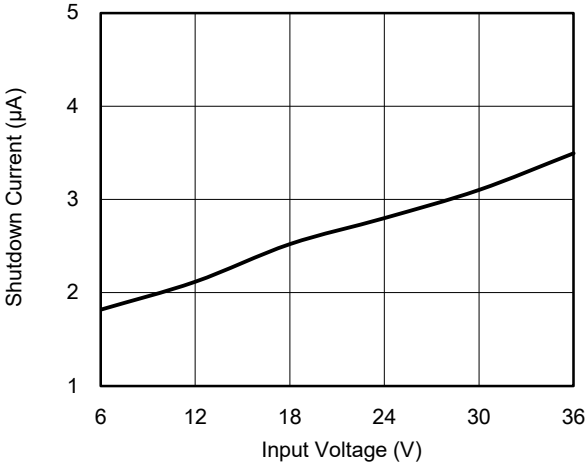

Shutdown Current vs. Junction Temperature




Quiescent Current vs. Input Voltage



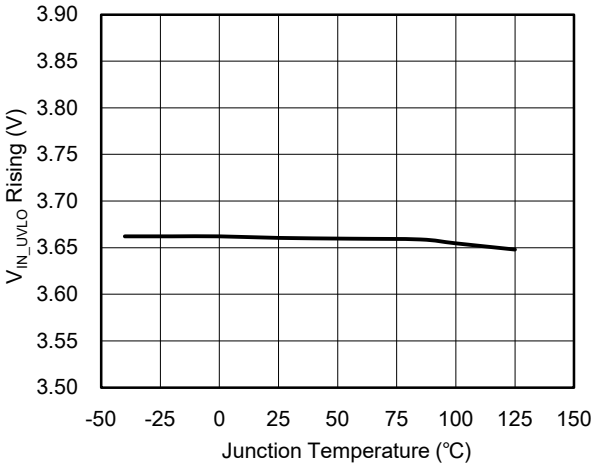

Shutdown Current vs. Input Voltage



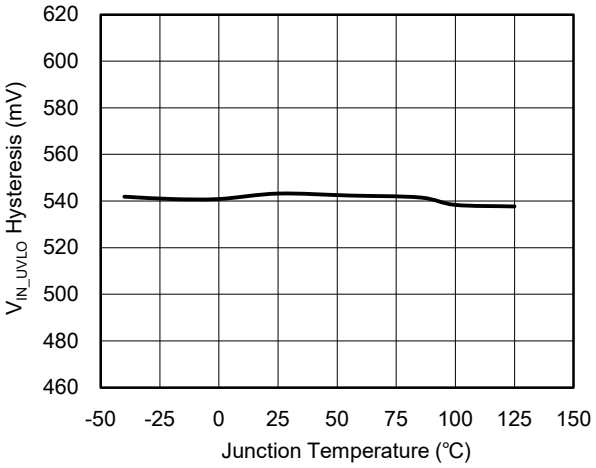
## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN}$ = 12V, $f_{SW}$ = 400kHz, L = 8.2μH, $C_{OUT}$ = 88μF, $T_A$ = 25℃, unless otherwise noted.

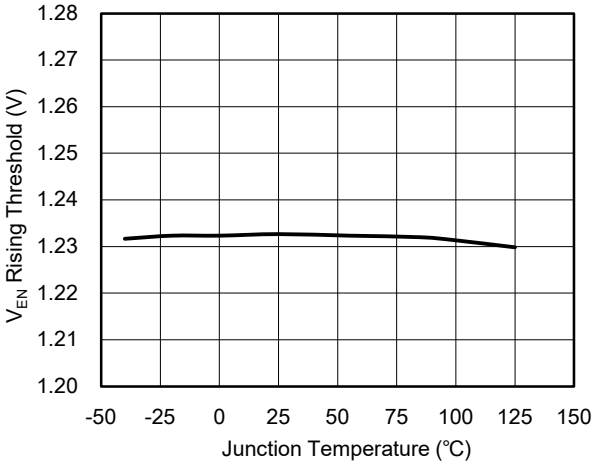
$V_{IN\_UVLO}$ Rising vs. Junction Temperature



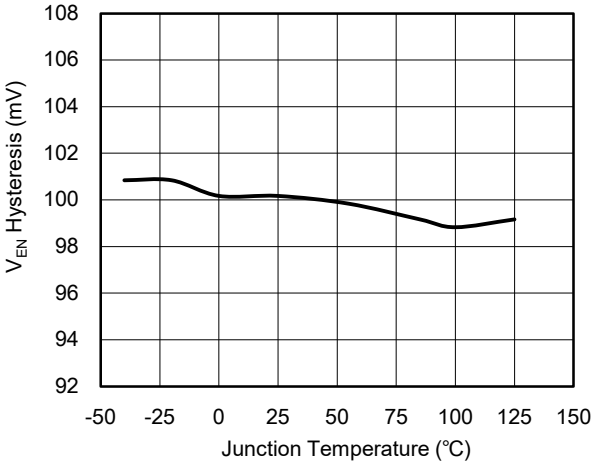

$V_{IN\_UVLO}$ Hysteresis vs. Junction Temperature



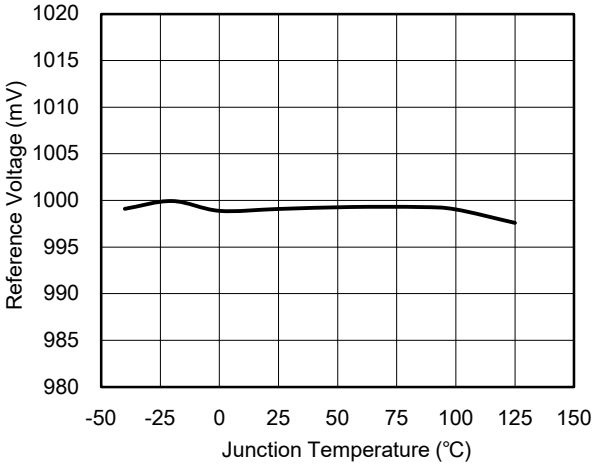

$V_{EN}$ Rising Threshold vs. Junction Temperature



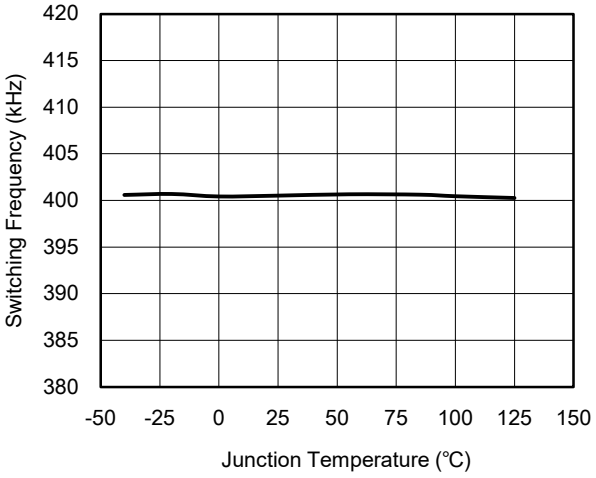

$V_{EN}$ Hysteresis vs. Junction Temperature




Reference Voltage vs. Junction Temperature



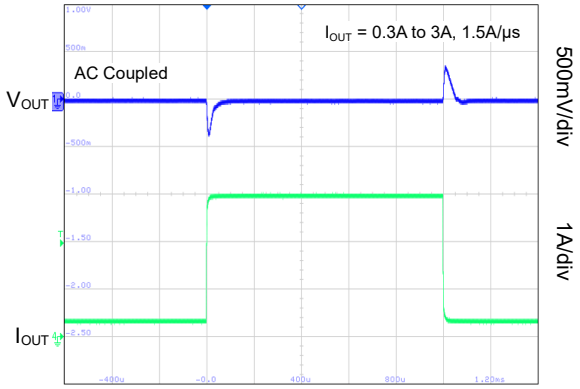

Switching Frequency vs. Temperature



## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

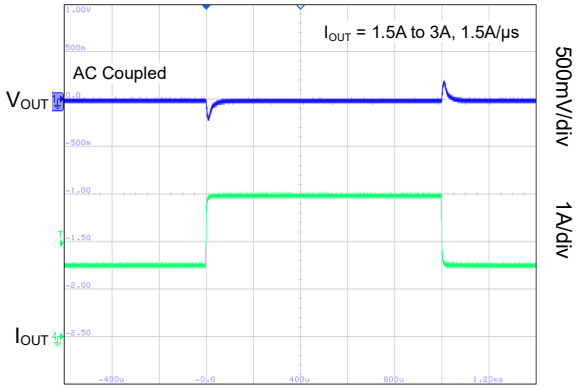
$V_{IN}$ = 12V, $V_{OUT}$ = 5V, $f_{SW}$ = 400kHz, L = 8.2μH, $C_{OUT}$ = 88μF, $T_A$ = 25℃, unless otherwise noted.

SGM61330A Load Transient



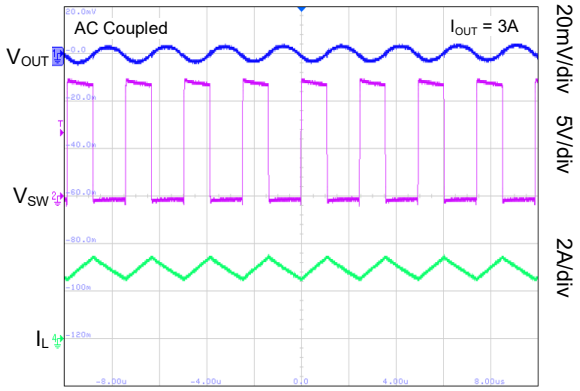

Time (200μs/div)

SGM61330A Load Transient



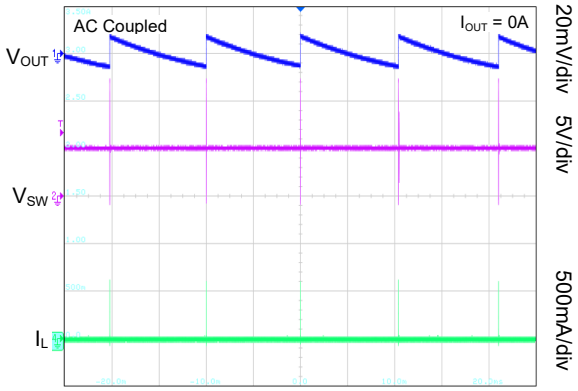

Time (200μs/div)

CCM Mode



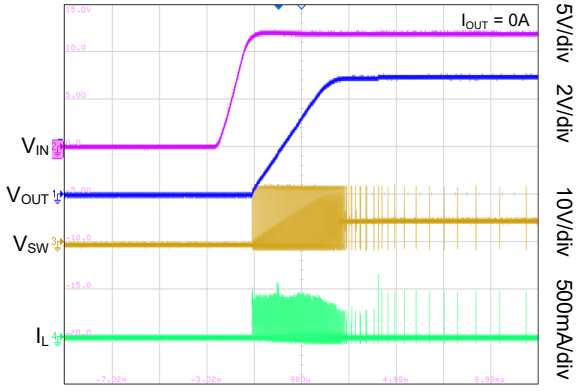

Time (2μs/div)

PSM Mode



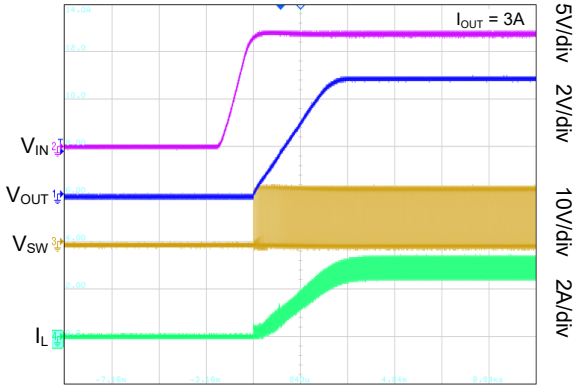

Time (5ms/div)

Start-Up by VIN




Time (2ms/div)

Start-Up by VIN

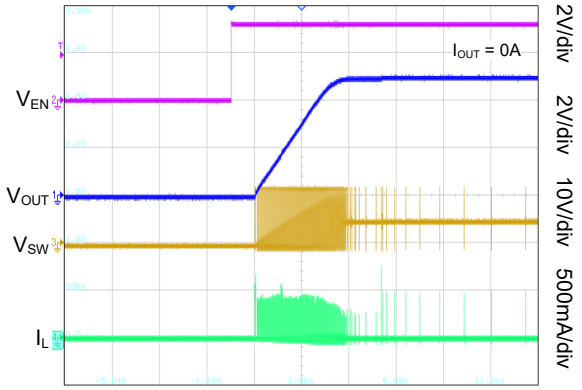



Time (2ms/div)

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

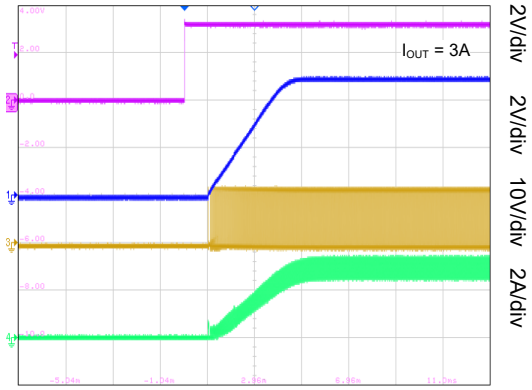
$V_{IN}$ = 12V, $V_{OUT}$ = 5V, $f_{SW}$ = 400kHz, L = 8.2μH, $C_{OUT}$ = 88μF, $T_A$ = 25℃, unless otherwise noted.

Start-Up by EN



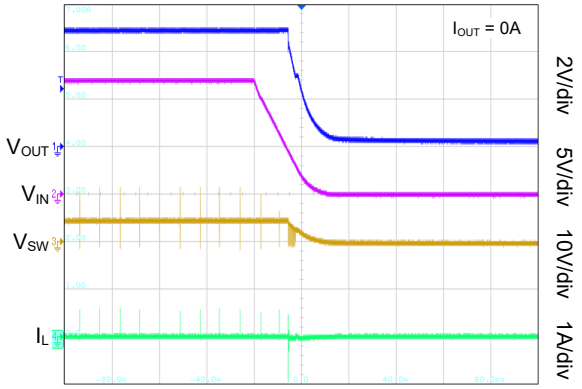

Time (2ms/div)

Start-Up by EN



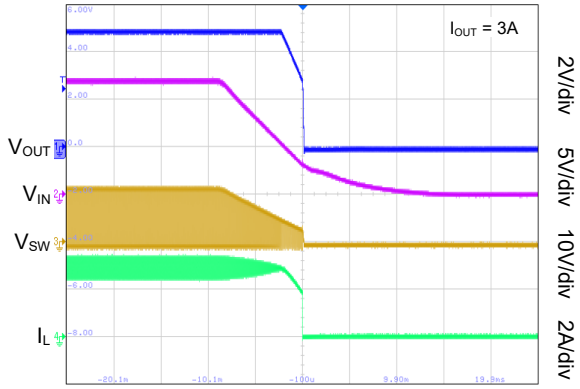

Time (2ms/div)

Shutdown by VIN



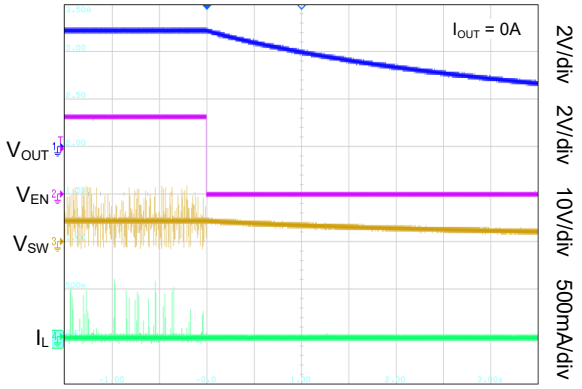

Time (20ms/div)

Shutdown by VIN



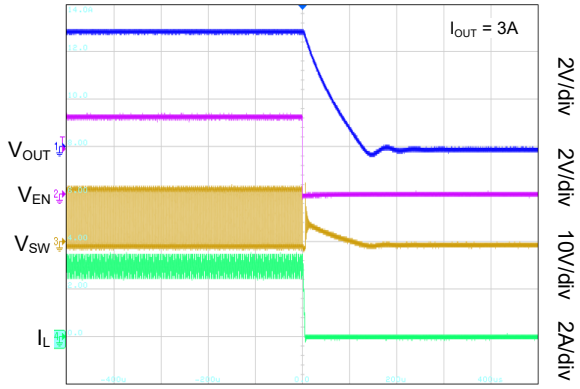

Time (5ms/div)

Shutdown by EN




Time (500ms/div)

Shutdown by EN

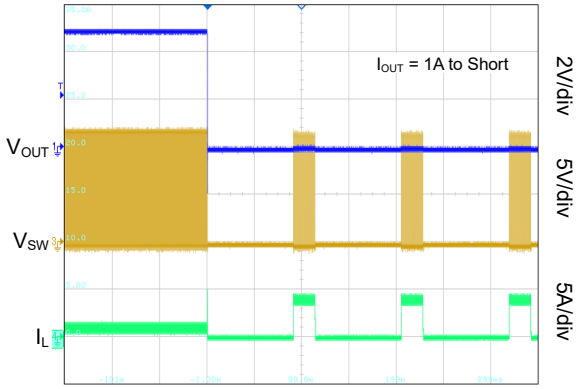



Time (100μs/div)

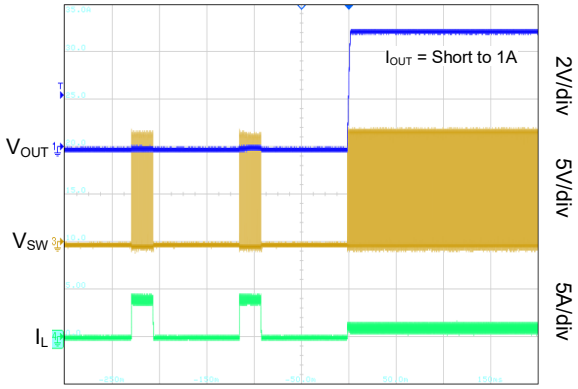
## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN}$ = 12V, $V_{OUT}$ = 5V, $f_{SW}$ = 400kHz, L = 8.2μH, $C_{OUT}$ = 88μF, $T_A$ = 25℃, unless otherwise noted.

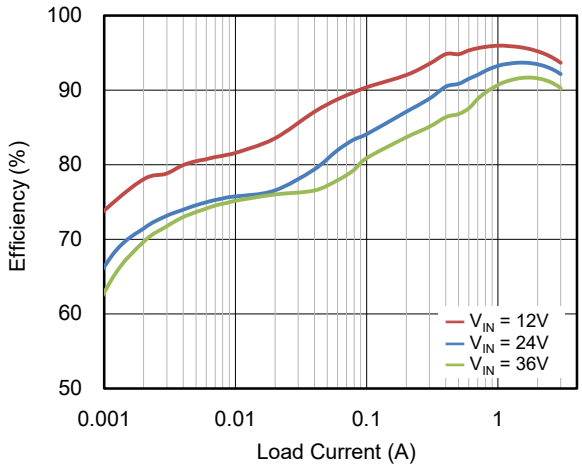
SCP Entry




SCP Recovery




Efficiency vs. Load Current



## FUNCTIONAL BLOCK DIAGRAM

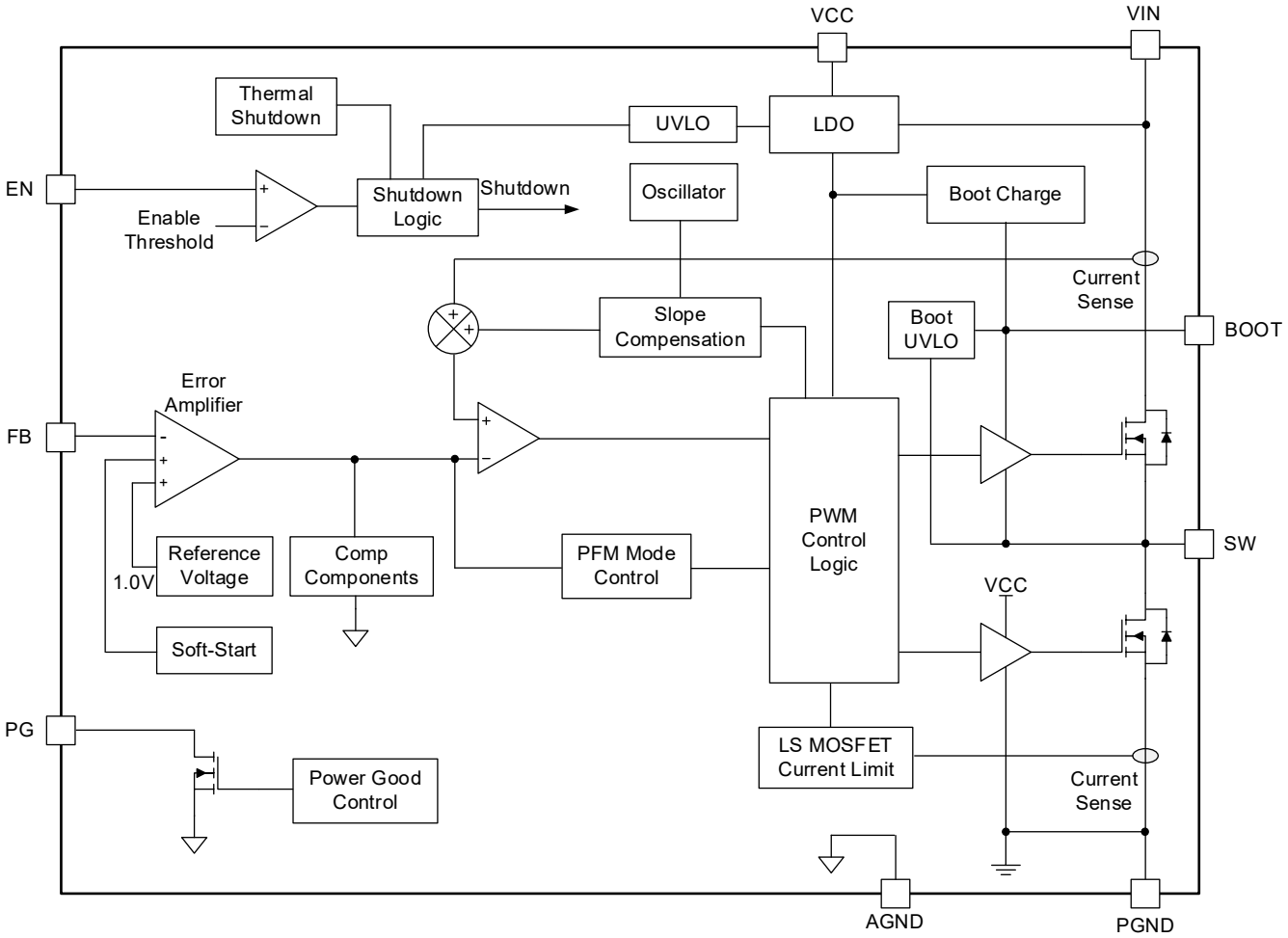



**Figure 2. Block Diagram**

# DETAILED DESCRIPTION

## Overview

The SGM61330 is a 36V synchronous Buck converter with two integrated N-MOSTETs and 3A continuous output current capability. Its internally compensated peak current mode control simplifies the design process and reduces the need for external components.

The minimum operating input voltage of the device is 3.8V. The output voltage can be set down to 1V (reference voltage). Typical no switching operating current is 29μA (TYP). The shutdown current is 2.1μA (TYP) if the device is disabled. High efficiency is achieved through the integrated low $R_{DSON}$ high-side switch (65mΩ for TQFN package) and low-side switch (42mΩ for TQFN package).

The bootstrap diode is integrated, and only a small capacitor ($C_{BOOT}$) between BOOT and SW pins is needed for the high-side MOSFET gate driving bias. The device also features a separate UVLO circuit that monitors $C_{BOOT}$ voltage and turns off the high-side switch if $C_{BOOT}$ voltage falls below a preset threshold.

Additional features such as thermal shutdown, over-voltage protection, and short-circuit protection (hiccup mode) are also provided.

## Minimum Input Voltage (3.8V) and UVLO

The recommended minimum operating input voltage is 3.8V. The device can operate with lower input voltages that are above the $V_{IN}$ rising UVLO threshold (3.66V TYP). The $V_{IN}$ UVLO threshold has a hysteresis of 540mV (TYP). If $V_{IN}$ falls below the falling UVLO voltage, the device will stop switching. If the EN pin is pulled high and $V_{IN}$ exceeds the rising UVLO threshold, the device will start up with a soft-start.

## Enable Input and UVLO Adjustment

The EN pin serves as an on/off control for the device. When the EN voltage is greater than $V_{EN\text{-}VCC\_H}$ (0.72V TYP), the device enters standby mode, where it supplies power to the internal VCC but does not generate an output voltage. To fully enable the device, continue to increase the EN voltage until it is above $V_{EN\_H}$ (1.23V TYP). If the EN voltage falls below $V_{EN\_H}$ - $V_{EN\_HYS}$ (1.13V TYP), the device will stop switching and enter standby mode. When the EN voltage is below $V_{EN\text{-}VCC\_L}$ (0.64V TYP), the device will be completely shut down.

If an application requires increasing the $V_{IN}$ turn-on threshold and adding hysteresis to the $V_{IN}$ UVLO, a voltage divider as shown in Figure 3 is required. Use Equation 1 and 2 to calculate these resistors. $V_{START}$ is the input start (turn-on) threshold voltage and $V_{STOP}$ is the input stop (turn-off) threshold voltage. In addition, if this feature is not required, the EN input can be connected directly to VIN, but make sure it is not left floating.

$$R_{EN1} = \left( \frac{V_{START}}{V_{EN\_H}} - 1 \right) \times R_{EN2} \quad (1)$$

$$V_{STOP} = V_{START} \times \left( 1 - \frac{V_{EN\_HYS}}{V_{EN\_H}} \right) \quad (2)$$

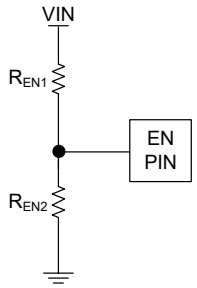



**Figure 3. VIN UVLO Adjustment**

## Power Good

The SGM61330 features a power-good (PG) pin that indicates whether the output voltage is at the desired level. This pin is an open-drain output that requires a resistor of 100kΩ pulled up to a DC voltage.

Figure 4 illustrates that when the FB voltage is within the power-good range, the PG switch is turned off, and the PG pin is pulled up to high. Conversely, when the FB voltage is outside the power-good range, the PG switch is turned on, and the PG pin is pulled down to low. If the power-good function is not required, the PG pin must be left floating. When EN is pulled low, the flag output will also be forced low.

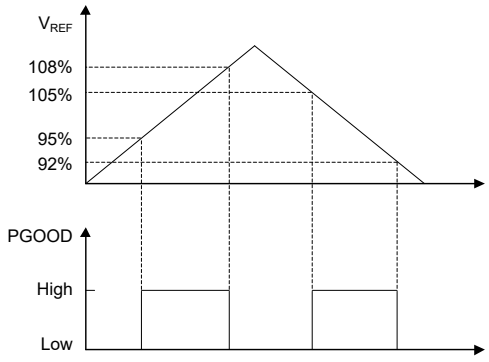



**Figure 4. Power-Good Flag**

## DETAILED DESCRIPTION (continued)

### Bootstrap Gate Driving (BOOT)

An internal voltage regulator provides bias voltage to the gate driver through an external small ceramic capacitor placed between the BOOT and SW pins. A 0.1μF ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor must have a 10V or higher voltage rating. Typically, $C_{BOOT}$ is charged during each cycle when the LS switch is turned on and discharged to the boot regulator when the HS switch is turned.

### Light Load Operation with PFM

The SGM61330 employs pulse frequency modulation (PFM) to achieve a lower switching frequency and maintain regulation. This leads to a reduction in switching losses along with an enhancement in efficiency. The device operates in PFM mode when the output load is low and shifts to pulse width modulation (PWM) mode when the load increases to a certain level.

### Low Dropout

As input voltage drops, the difference between input voltage and output voltage decreases, causing off-time of the high-side MOSFET to approach its minimum possible value. Dropout occurs when input voltage falls below the required minimum for the regulator to maintain output voltage. To maintain output voltage at nominal value, SGM61330 will decrease its switching frequency and increase duty cycle.

### Minimum Switch On-Time

The minimum controllable on-time of SGM61330 is affected by the inherent delay and blanking time of the control circuit. The minimum on-time reduces the conversion ratio of the system, restricts some applications to high input voltages and low output voltages at high switching frequencies. To solve this problem, SGM61330 maintains a constant turn-on time when it reaches the minimum turn-on time and decreases its switching frequency, resulting in an increased conversion ratio.

### Over-Current Protection

Current mode control provides over-current protection (OCP) by HS current sensing, which compares the sensed HS switch current with the HS current-limit threshold in each cycle. When the HS current reaches that threshold, the HS switch is turned off. Then the low-side (LS) switch is turned on, the conduction current is monitored by the internal circuitry. In each cycle, the sensed LS switch current is compared to the internally LS current-limit threshold only when the HS current-limit threshold is triggered. If the sensed LS switch current is higher than the LS current-limit threshold during LS conduction, the HS does not turn on and the LS stays on when the clock signal comes. When the sensed LS switch current is below the LS current-limit threshold, for SGM61330A (TQFN), the HS switch waits until the clock signal arrives before turning on again; whereas for other versions, the HS switch turns on again immediately.

In addition, if the HS current reaches the current-limit threshold and FB drops below 40% of $V_{REF}$, then the device shuts down and restarts after 80ms (TYP). If OCP or SCP persists for more than 20ms (TYP) after the automatic restart, a new hiccup cycle will be initiated. Hiccup mode is a protective measure designed to prevent overheating and severe damage from over-current conditions.

### Thermal Shutdown (TSD)

If the junction temperature ($T_J$) exceeds +165℃ (TYP), the TSD protection circuit will stop the switch from operating to protect the device from overheating. After the junction temperature drops below +150℃ (TYP), the device automatically restarts and goes through the power-up procedure.

# APPLICATION INFORMATION

The design method for the SGM61330 Buck converter is explained in this section. A typical application circuit for the SGM61330 is shown in Figure 5. It is used for converting a 6V to 36V supply voltage to a lower 5V output voltage with a maximum output current of 3A.

The external components are designed based on the application requirements and device stability. Some suitable parameters for different output voltages are provided in Table 1 to simplify the selection of components. The $C_{OUT}$ values in Table 1 are rated values.

## Typical Application

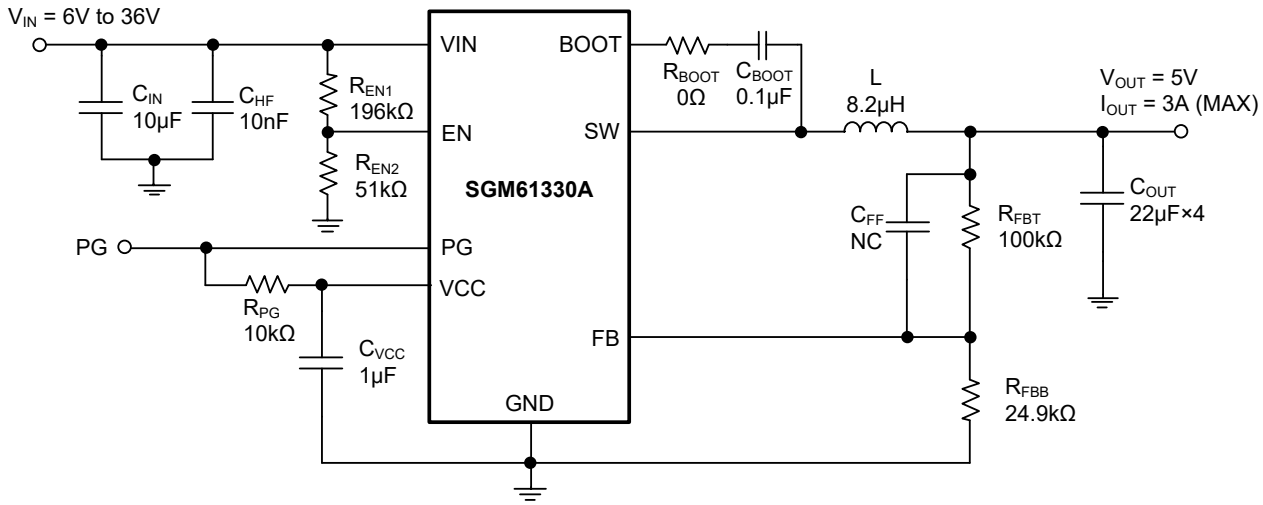



**Figure 5. SGM61330A Typical Application Circuit**

**Table 1. Some Typical Parameters for Stable Operation**

| $f_{SW}$ (kHz) | $V_{OUT}$ (V) | L (μH) | $C_{OUT}$ (μF) | $R_{FBT}$ (kΩ) | $R_{FBB}$ (kΩ) | $C_{FF}$ (pF) |
|---|---|---|---|---|---|---|
| 400 | 3.3 | 6.8 | 4×22 | 100 | 43.2 | NC |
| 2100 | 3.3 | 1.2 | 2×22 | 100 | 43.2 | 22pF |
| 400 | 5 | 8.2 | 4×22 | 100 | 24.9 | NC |
| 2100 | 5 | 1.5 | 2×22 | 100 | 24.9 | 22pF |
| 400 | 12 | 15 | 4×22 | 100 | 9.09 | NC |
| 2100 | 12 | 3.3 | 4×10 | 100 | 9.09 | NC |

## Requirements

The design parameters required for the design example are given in Table 2.

**Table 2. Design Parameters**

| Design Parameter | Example Value |
|---|---|
| Input Voltage | 12V nominal |
| Output Voltage | 5V |
| Output Current Rating | 3A |
| Operating Frequency | 400kHz |

## Switching Frequency

The SGM61330 has three frequencies to choose from: 400kHz (TYP) for the SGM61330A, 1.4MHz (TYP) for the SGM61330B, and 2.1MHz (TYP) for the SGM61330C. For this design, a switching frequency of 400kHz was chosen as an example.

## APPLICATION INFORMATION (continued)

### Input Capacitors Design

A high-quality ceramic capacitor (X5R or X7R or better dielectric grade) must be used for input decoupling of the SGM61330. At least 3μF of effective capacitance (after derating) is needed at the input. In some applications, additional bulk capacitance may also be required for the input, for example, when the SGM61330 is more than 5cm away from the input source. The input capacitor ripple current rating must also be greater than the maximum input current ripple. The input current ripple can be calculated using Equation 3 and the maximum value occurs at 50% duty cycle. Using the design example values, $I_{OUT}$ = 3A, yields an RMS input ripple current of 1.5A.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times V_{IN}}} = I_{OUT} \times \sqrt{D \times (1-D)} \quad (3)$$

For this design, a ceramic capacitor with at least 50V voltage rating is required to support the maximum input voltage. Therefore, a 10μF/50V capacitor is selected for VIN to cover all DC bias, thermal and aging derating. The input capacitance determines the regulator input voltage ripple. This ripple can be calculated from Equation 4.

$$\Delta V_{IN} = \frac{I_{OUT} \times D \times (1-D)}{C_{IN} \times f_{SW}} \quad (4)$$

It is recommended to place an additional small size 10nF/0603 ceramic capacitor ($C_{HF}$) right beside VIN and GND pins for high frequency filtering.

### Inductor Design

Equation 5 is conventionally used to calculate the output inductance of a Buck converter. The ratio of inductor current ripple ($\Delta I_L$) to the maximum output current ($I_{OUT}$) is represented as $K_{IND}$ factor ($K_{IND}$ = $\Delta I_L/I_{OUT}$). The inductor ripple current is bypassed and filtered by the output capacitor and the inductor DC current is passed to the output. Inductor ripple is selected based on a few considerations. The peak inductor current ($I_{OUT}$ + $\Delta I_L/2$) must have a safe margin from the saturation current of the inductor in the worst-case conditions. For peak current mode converter, selecting an inductor with saturation current must be above the switch current limit. Typically, a 20% to 40% current ripple is selected ($K_{IND}$ = 0.2 ~ 0.4).

$$L = \frac{V_{IN} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN} \times f_{SW}} \quad (5)$$

In this example, the calculated inductance will be 8.1μH with $K_{IND}$ = 0.3 at $V_{IN}$ = 12V, therefor the nearest larger inductance of 8.2μH is selected. The ripple, RMS and peak inductors current calculations are summarized in Equations 6, 7 and 8 respectively.

$$\Delta I_L = \frac{V_{IN} - V_{OUT}}{L} \times \frac{V_{OUT}}{V_{IN} \times f_{SW}} \quad (6)$$

$$I_{L\_RMS} = \sqrt{I_{OUT}^2 + \frac{\Delta I_L^2}{12}} \quad (7)$$

$$I_{L\_PEAK} = I_{OUT} + \frac{\Delta I_L}{2} \quad (8)$$

## APPLICATION INFORMATION (continued)

### Output Capacitor Design

There are three main criteria that must be considered when designing the output capacitor ($C_{OUT}$): (1) the converter pole location, (2) the output voltage ripple, (3) the transient response to a large change in load current. The selected value must satisfy all of them. The desired transient response is usually expressed as maximum overshoot, maximum undershoot, or maximum recovery time of $V_{OUT}$ in response to a large load step. Transient response is usually the more stringent criteria in low output voltage applications. The output capacitor must provide the increased load current or absorb the excess inductor current until the control loop can re-adjust the current of the inductor to the new load level. Typically, it requires two or more cycles for the loop to detect and respond to the output change. Another requirement may also be expressed as desired hold-up time in which the output capacitor must hold the output voltage above a certain level for a specified period if the input power is removed. It may also be expressed as the maximum output voltage drop or rise when the full load is connected or disconnected (100% load step). Equation 9 can be used to calculate the minimum output capacitance that is needed to supply a current step ($\Delta I_{OUT}$) for at least 2 cycles until the control loop responds to the load change with a maximum allowed output transient of $\Delta V_{OUT}$ (overshoot or undershoot).

$$C_{OUT} > \frac{2 \times \Delta I_{OUT}}{f_{SW} \times \Delta V_{OUT}} \quad (9)$$

where:

- $\Delta I_{OUT}$ is the change in output current.
- $\Delta V_{OUT}$ is the allowable change in the output voltage.

For example, if the acceptable transient from 1.5A to 3A load step is 5%, by inserting $\Delta V_{OUT}$ = 0.05 × 5V = 0.25V and $\Delta I_{OUT}$ = 1.5A, the minimum required capacitance will be 30μF. Note that the impact of output capacitor ESR on the transient is not considered in Equation 9. For ceramic capacitors, the ESR is generally small enough to ignore its impact on the calculation of $\Delta V_{OUT}$ transient.

The output capacitor must also be sized to absorb energy stored in the inductor when transitioning from a high to low load current. The energy stored in the inductor can produce an output voltage overshoot when the load current rapidly decreases. The excess energy absorbed in the output capacitor increases the voltage on the capacitor. The capacitor must be sized to maintain the desired output voltage during these transient periods. Equation 10 calculates the minimum capacitance required to keep the output-voltage overshoot to a desired value.

$$C_{OUT} > L \times \frac{I_{OUT\_H}^2 - I_{OUT\_L}^2}{\left(V_{OUT} + \Delta V_{OUT}\right)^2 - V_{OUT}^2} \quad (10)$$

where:

- $I_{OUT\_H}$ is the output current under heavy load.
- $I_{OUT\_L}$ is the output current under light load.

For example, if the acceptable transient from 3A to 1.5A load step is 5%, by inserting $\Delta V_{OUT}$ = 0.05 × 5V = 0.25V, the minimum required capacitance will be 21.6μF.

Equation 11 can be used for the output ripple criteria and finding the minimum output capacitance needed. $V_{OUT\_RIPPLE}$ is the maximum acceptable ripple. In this example, the allowed ripple is 50mV that results in minimum capacitance of 5.6μF.

$$C_{OUT} > \frac{\Delta I_L}{8 \times f_{SW} \times V_{OUT\_RIPPLE}} \quad (11)$$

## APPLICATION INFORMATION (continued)

Note that the impact of output capacitor ESR on the ripple is not considered in Equation 11. For a specific output capacitance value, use Equation 12 to calculate the maximum acceptable ESR of the output capacitor to meet the output voltage ripple requirement.

$$ESR_{COUT} < \frac{V_{OUT\_RIPPLE}}{\Delta I_L} - \frac{1}{8 \times f_{SW} \times C_{OUT}} \quad (12)$$

Higher nominal capacitance value must be chosen due to aging, temperature, and DC bias derating of the output capacitors. In this example, four 22μF/25V ceramic capacitors are used. The amount of ripple current that a capacitor can handle without damage or overheating is limited. The inductor ripple is bypassed through the output capacitor. Equation 13 calculates the RMS current that the output capacitor must support.

$$I_{COUT\_RMS} = \frac{V_{OUT} \times \left(V_{IN\_MAX} - V_{OUT}\right)}{\sqrt{12} \times V_{IN\_MAX} \times L \times f_{SW}} \quad (13)$$

### Bootstrap Capacitor Selection

Use a 0.1μF high-quality ceramic capacitor (X7R or X5R) with 10V or higher voltage rating for the bootstrap capacitor ($C_{BOOT}$). It is recommended to add a resistor $R_{BOOT}$ in series with $C_{BOOT}$ to slow down switch-on speed of the HS switch and improve radiated EMI problems. For most applications, $R_{BOOT}$ is used around 5Ω ~ 10Ω. Too high values for $R_{BOOT}$ may cause insufficient $C_{BOOT}$ charging in high duty-cycle applications. Slower switch switch-on peed will also increase switch losses and reduce efficiency.

### UVLO Setting

The input UVLO can be programmed using an external voltage divider on the EN pin of the SGM61330, as shown in Figure 3. In this design, the turn-on (enable to start switching) occurs when $V_{IN}$ rises above 6V (UVLO rising threshold). When the regulator is working, it will not stop switching until the input falls below 5.5V (UVLO falling threshold). Equations 1 and 2 are provided to calculate $R_{EN1}$ and $V_{STOP}$, respectively.

### Feedback Resistors Setting

Use resistor dividers ($R_{FBT}$ and $R_{FBB}$) to set the output voltage using Equation 14 and 15.

$$R_{FBB} = \frac{R_{FBT} \times V_{REF}}{V_{OUT} - V_{REF}} \quad (14)$$

$$V_{OUT} = V_{REF} \times \left(\frac{R_{FBT}}{R_{FBB}} + 1\right) \quad (15)$$

Recommended to choose $R_{FBT}$ around 100kΩ and calculate $R_{FBB}$ from Equation 14. Use accurate and stable resistors (1% or better) to enhance output accuracy. For this example, the selected values are $R_{FBT}$ = 100kΩ and $R_{FBB}$ = 24.9kΩ, resulting in a 5.016V output voltage.

### $C_{FF}$ Selection

Even though the SGM61330 is internally compensated, with low ESR ceramic capacitors, the phase margin can be low depending on the $V_{OUT}$ and $f_{SW}$ values. By adding an external feed-forward capacitor ($C_{FF}$) in parallel with the $R_{FBT}$, the phase margin can be improved (phase boost around crossover frequency). Without $C_{FF}$, and if ESR is very small, the crossover frequency ($f_X$) can be estimated from Equation 16, in which $C_{OUT}$ is the actual derated value:

$$f_X = \frac{K}{V_{OUT} \times C_{OUT}} \quad (16)$$

where:

- K = 7.273 for SGM61330A.
- K = 9.697 for SGM61330B.
- K = 11.141 for SGM61330C.

Then $C_{FF}$ value can be estimated from:

$$C_{FF} = \frac{1}{2\pi \times f_X \times R_{FBT}} \quad (17)$$

For slightly larger ESR values, choose a $C_{FF}$ value that is less than Equation 17 estimate. For larger ESR values, $C_{FF}$ is not needed. Table 1 gives a quick starting point.

# APPLICATION INFORMATION (continued)

## Layout Considerations

Examples of PCB layouts for SGM61330 in SOIC-8 and TQFN packages are provided in in Figure 6 and Figure 7, respectively. These layouts have been shown to bring good results, although other layout designs may also obtain good performance.

- Bypass the VIN pin to GND pin with low-ESR ceramic capacitors (10μF/X5R or better) and place them as close as possible to the device.
- Share the same GND connection point with the input and output capacitors.
- Connect the device GND to the PCB ground plane right at the GND pin.
- Minimize the length and the area of the connection route from SW pin to the inductor to reduce the noise coupling from this area.
- Consider sufficient ground plane area on the top side for proper heat dissipation. Connect the large internal or back-side ground planes to the top-side ground near the device with thermal vias for better heat dissipation.

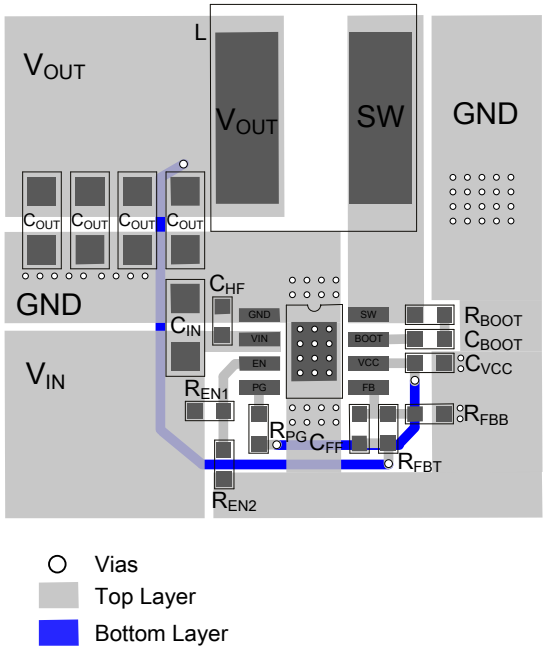



Figure 6. Example of PCB layouts for SOIC-8 package

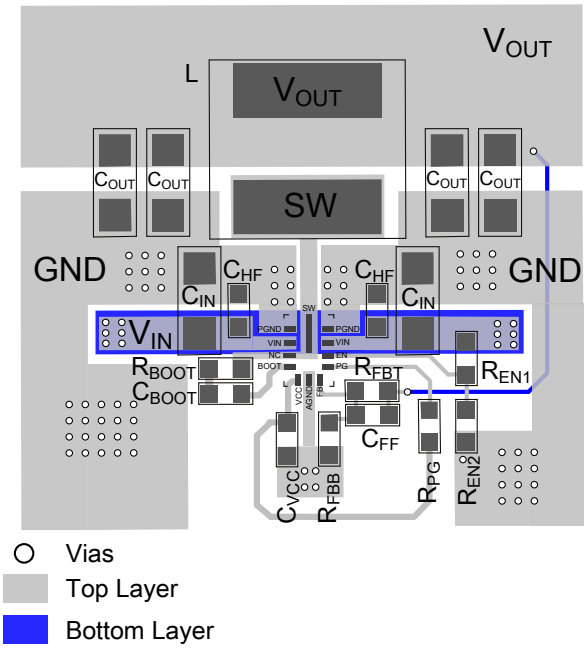
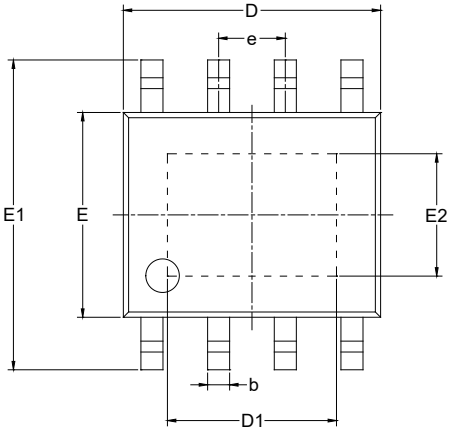
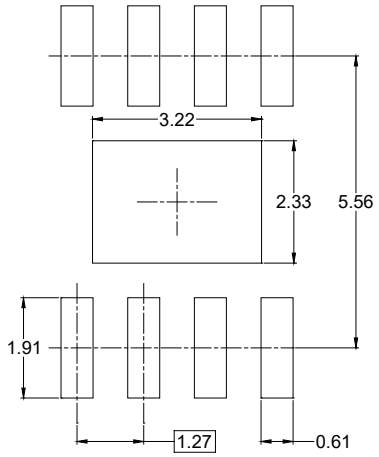



Figure 7. Example of PCB layouts for TQFN package

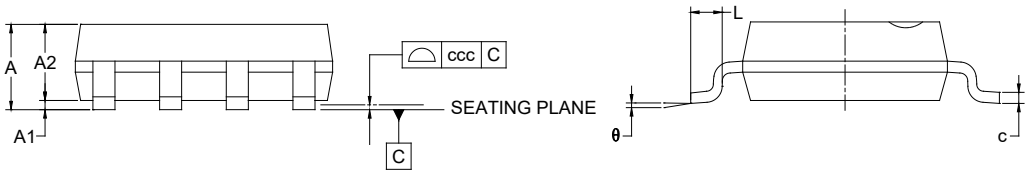
# PACKAGE OUTLINE DIMENSIONS

## SOIC-8 (Exposed Pad)




**RECOMMENDED LAND PATTERN** (Unit: mm)

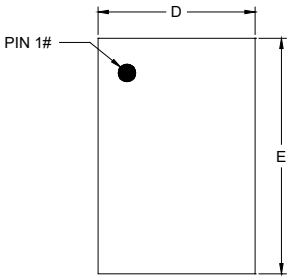



| Symbol | Dimensions In Millimeters | | |
|---|---|---|---|
| | MIN | MOD | MAX |
| A | | | 1.700 |
| A1 | 0.000 | - | 0.150 |
| A2 | 1.250 | - | 1.650 |
| b | 0.330 | - | 0.510 |
| c | 0.170 | - | 0.250 |
| D | 4.700 | - | 5.100 |
| D1 | 3.020 | - | 3.420 |
| E | 3.800 | - | 4.000 |
| E1 | 5.800 | - | 6.200 |
| E2 | 2.130 | - | 2.530 |
| e | 1.27 BSC | | |
| L | 0.400 | - | 1.270 |
| θ | 0° | - | 8° |
| ccc | 0.100 | | |

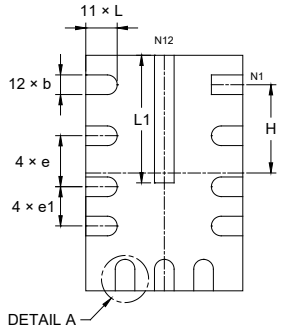
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MS-012.

# PACKAGE OUTLINE DIMENSIONS

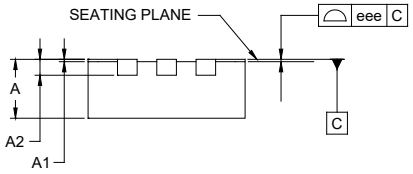
## TQFN-2×3-12AL




TOP VIEW

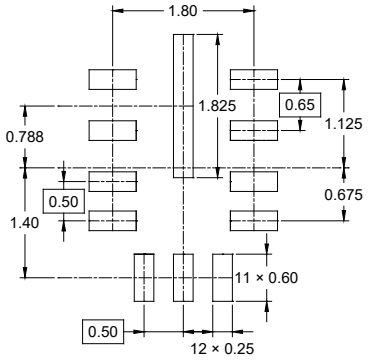



BOTTOM VIEW




SIDE VIEW


**DETAIL A**
ALTERNATE TERMINAL CONSTRUCTION



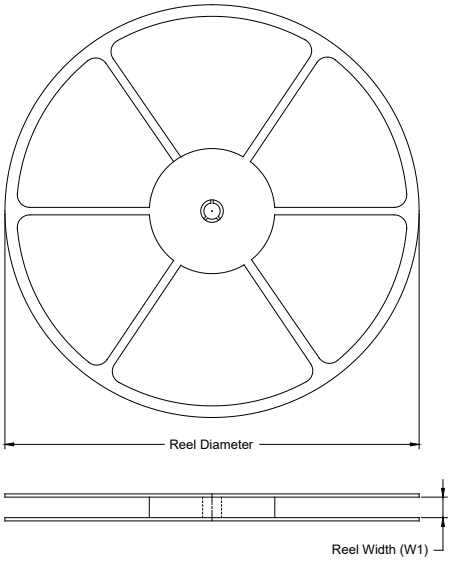

**RECOMMENDED LAND PATTERN** (Unit: mm)

| Symbol | Dimensions In Millimeters | | |
|---|---|---|---|
| | MIN | MOD | MAX |
| A | 0.700 | - | 0.800 |
| A1 | 0.000 | - | 0.050 |
| A2 | 0.203 REF | | |
| b | 0.200 | - | 0.300 |
| D | 1.900 | - | 2.100 |
| E | 2.900 | - | 3.100 |
| e | 0.650 BSC | | |
| e1 | 0.500 BSC | | |
| H | 1.125 BSC | | |
| L | 0.300 | - | 0.500 |
| L1 | 1.525 | - | 1.725 |
| eee | 0.080 | | |

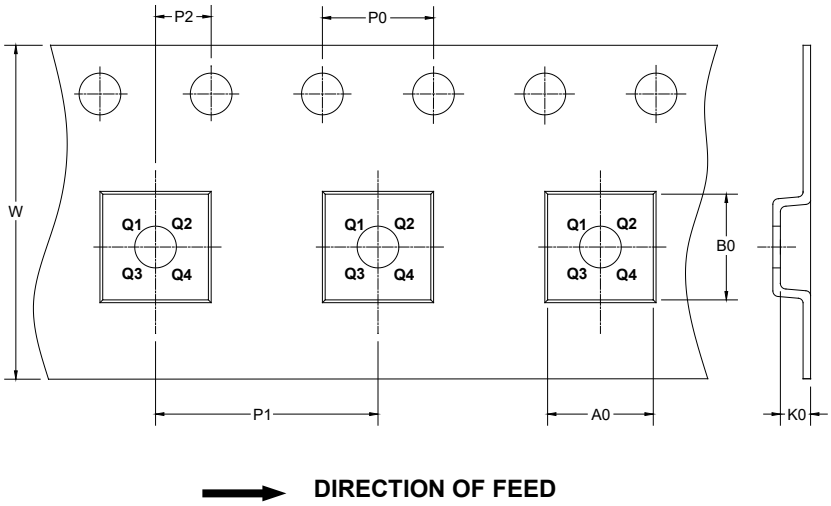
NOTE: This drawing is subject to change without notice.

# TAPE AND REEL INFORMATION

### REEL DIMENSIONS




### TAPE DIMENSIONS




NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF TAPE AND REEL

| Package Type | Reel Diameter | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | P1 (mm) | P2 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|
| SOIC-8 (Exposed Pad) | 13" | 12.4 | 6.40 | 5.40 | 2.10 | 4.0 | 8.0 | 2.0 | 12.0 | Q1 |
| TQFN-2×3-12AL | 7" | 9.5 | 2.30 | 2.30 | 1.00 | 4.0 | 4.0 | 2.0 | 8.0 | Q1 |

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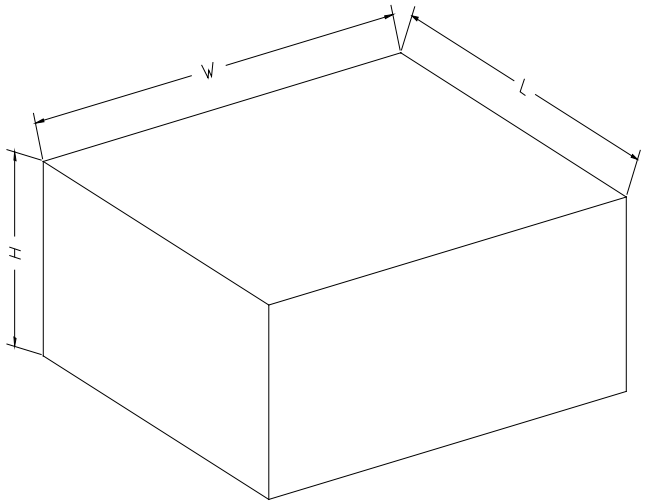
## CARTON BOX DIMENSIONS




NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF CARTON BOX

| Reel Type | Length (mm) | Width (mm) | Height (mm) | Pizza/Carton |
|---|---|---|---|---|
| 7″ (Option) | 368 | 227 | 224 | 8 |
| 7″ | 442 | 410 | 224 | 18 |
| 13″ | 386 | 280 | 370 | 5 |

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