Analog Multiplexers / Demultiplexers with LSTTL Compatible Inputs

High−Performance Silicon−Gate CMOS

MC74HCT4051A, MC74HCT4052A, MC74HCT4053A

The MC74HCT4051A, MC74HCT4052A and MC74HCT4053A utilize silicon−gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF leakage currents. These analog multiplexers/demultiplexers control analog voltages that may vary across the complete power supply range (from V_{CC} to V_{EE}).

The HCT4051A, HCT4052A and HCT4053A are identical in pinout to the metal−gate MC14051AB, MC14052AB and MC14053AB. The Channel−Select inputs determine which one of the Analog Inputs/Outputs is to be connected, by means of an analog switch, to the Common Output/Input. When the Enable pin is HIGH, all analog switches are turned off.

The Channel−Select and Enable inputs are compatible with standard CMOS and LSTTL outputs.

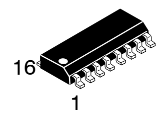
These devices have been designed so that the ON resistance (R_{on}) is more linear over input voltage than R_{on} of metal−gate CMOS analog switches.

For a multiplexer/demultiplexer with injection current protection, see HC4851A and HCT4851A.

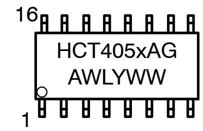
Features

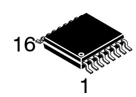
- Fast Switching and Propagation Speeds
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power Supply Range (V_{CC} − V_{EE}) = 2.0 to 12.0 V
- Digital (Control) Power Supply Range (V_{CC} − GND) = 2.0 to 6.0 V
- Improved Linearity and Lower ON Resistance Than Metal−Gate Counterparts
- Low Noise
- In Compliance with the Requirements of JEDEC Standard No. 7 A
- Chip Complexity: HCT4051A − 184 FETs or 46 Equivalent Gates
HCT4052A − 168 FETs or 42 Equivalent Gates
HCT4053A − 156 FETs or 39 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

MARKING DIAGRAMS

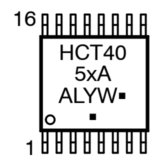


SOIC−16
D SUFFIX
CASE 751B





TSSOP−16
DT SUFFIX
CASE 948F



x	= 1, 2, 3
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week
G or ▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

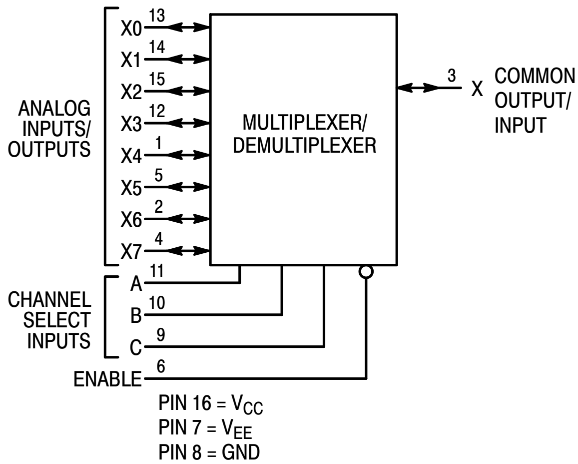


Figure 1. Logic Diagram − MC74HCT4051A Single−Pole, 8−Position Plus Common Off

FUNCTION TABLE − MC74HCT4051A

Control Inputs				
	Select			
Enable	**C**	**B**	**A**	**ON Channels**
L	L	L	L	X0
L	L	L	H	X1
L	L	H	L	X2
L	L	H	H	X3
L	H	L	L	X4
L	H	L	H	X5
L	H	H	L	X6
L	H	H	H	X7
H	X	X	X	NONE

X = Don't Care

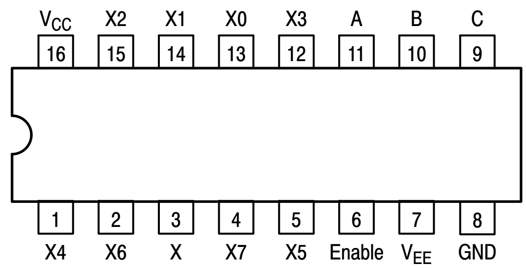


Figure 2. Pinout: MC74HCT4051A
(Top View)

FUNCTION TABLE − MC74HCT4052A

Control Inputs			ON Channels	
	Select			
Enable	**B**	**A**		
L	L	L	Y0	X0
L	L	H	Y1	X1
L	H	L	Y2	X2
L	H	H	Y3	X3
H	X	X	NONE	

X = Don't Care

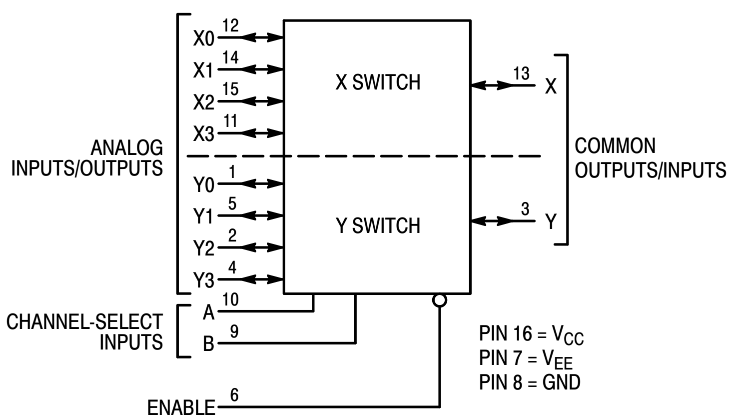


Figure 3. Logic Diagram − MC74HCT4052A Double−Pole, 4−Position Plus Common Off

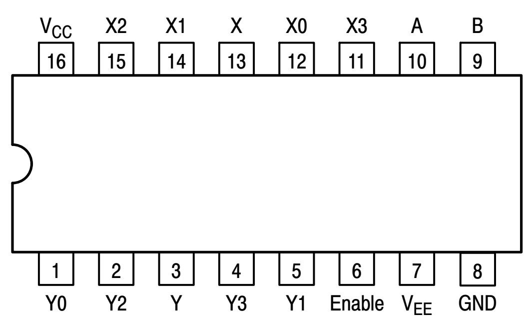
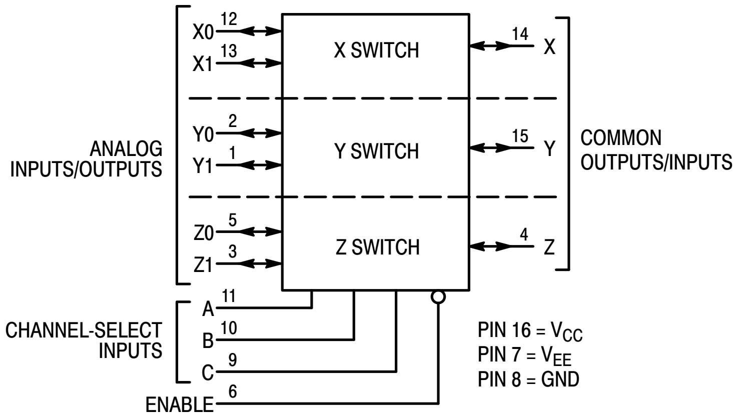


Figure 4. Pinout: MC74HCT4052A (Top View)



NOTE: This device allows independent control of each switch. Channel−Select Input A controls the X−Switch, Input B controls the Y−Switch and Input C controls the Z−Switch

Figure 5. Logic Diagram − MC74HCT4053A
Triple Single−Pole, Double−Position Plus Common Off

FUNCTION TABLE − MC74HCT4053A

Control Inputs				ON Channels		
	Select					
Enable	C	B	A			
L	L	L	L	Z0	Y0	X0
L	L	L	H	Z0	Y0	X1
L	L	H	L	Z0	Y1	X0
L	L	H	H	Z0	Y1	X1
L	H	L	L	Z1	Y0	X0
L	H	L	H	Z1	Y0	X1
L	H	H	L	Z1	Y1	X0
L	H	H	H	Z1	Y1	X1
H	X	X	X		NONE	

X = Don't Care

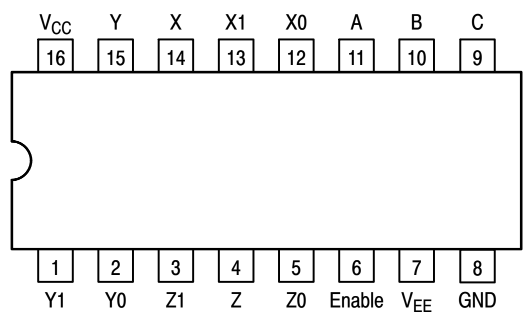


Figure 6. Pinout: MC74HCT4053A (Top View)

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND) (Referenced to V_{EE})	–0.5 to +7.0 –0.5 to +14.0	V
V_{EE}	Negative DC Supply Voltage (Referenced to GND)	–7.0 to +5.0	V
V_{IS}	Analog Input Voltage	V_{EE} – 0.5 to V_{CC} + 0.5	V
V_{in}	Digital Input Voltage (Referenced to GND)	–0.5 to V_{CC} + 0.5	V
I	DC Current, Into or Out of Any Pin	±25	mA
P_D	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature Range	–65 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
†Derating – SOIC Package: – 7 mW/°C from 65°C to 125°C
TSSOP Package: – 6.1 mW/°C from 65°C to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND) (Referenced to V_{EE})	2.0 2.0	6.0 12.0	V
V_{EE}	Negative DC Supply Voltage, Output (Referenced to GND)	−6.0	GND	V
V_{IS}	Analog Input Voltage	V_{EE}	V_{CC}	V
V_{in}	Digital Input Voltage (Referenced to GND)	GND	V_{CC}	V
V_{IO}*	Static or Dynamic Voltage Across Switch		1.2	V
T_A	Operating Temperature Range, All Package Types	−55	+125	°C
t_r, t_f	Input Rise/Fall Time (Channel Select or Enable Inputs) V_{CC} = 2.0 V V_{CC} = 3.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0 0	1000 600 500 400	ns

*For voltage drops across switch greater than 1.2 V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC CHARACTERISTICS − Digital Section (Voltages Referenced to GND) V_{EE} = GND, Except Where Noted

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit −55 to 25°C	≤85°C	≤125°C	Unit
V_{IH}	Minimum High−Level Input Voltage, Channel−Select or Enable Inputs	R_{on} = Per Spec	4.5 to 5.5	2.0	2.0	2.0	V
V_{IL}	Maximum Low−Level Input Voltage, Channel−Select or Enable Inputs	R_{on} = Per Spec	4.5 to 5.5	0.8	0.8	0.8	V
I_{in}	Maximum Input Leakage Current, Channel−Select or Enable Inputs	V_{in} = V_{CC} or GND, V_{EE} = − 6.0 V	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	Channel Select, Enable and V_{IS} = V_{CC} or GND; V_{IO} = 0 V V_{EE} = GND V_{EE} = − 6.0	 6.0 6.0	 1 4	 10 40	 20 80	μA

DC CHARACTERISTICS − Analog Section

Symbol	Parameter	Condition	V_{CC}	V_{EE}	Guaranteed Limit −55 to 25°C	≤85°C	≤125°C	Unit
R_{on}	Maximum "ON" Resistance	V_{in} = V_{IL} or V_{IH}; V_{IS} = V_{CC} to V_{EE}; I_S ≤ 2.0 mA (Figures 7, 8)	4.5 4.5 6.0	0.0 −4.5 −6.0	190 120 100	240 150 125	280 170 140	Ω
		V_{in} = V_{IL} or V_{IH}; V_{IS} = V_{CC} or V_{EE} (Endpoints); I_S ≤ 2.0 mA (Figures 7, 8)	4.5 4.5 6.0	0.0 −4.5 −6.0	150 100 80	190 125 100	230 140 115	
ΔR_{on}	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	V_{in} = V_{IL} or V_{IH}; V_{IS} = 1/2 (V_{CC} − V_{EE}); I_S ≤ 2.0 mA	4.5 4.5 6.0	0.0 −4.5 −6.0	30 12 10	35 15 12	40 18 14	Ω
I_{off}	Maximum Off−Channel Leakage Current, Any One Channel	V_{in} = V_{IL} or V_{IH}; V_{IO} = V_{CC} − V_{EE}; Switch Off (Figure 9)	5.0	−5.0	0.1	0.5	1.0	μA
	Maximum Off−Channel Leakage Current, Common Channel HCT4051A HCT4052A HCT4053A	V_{in} = V_{IL} or V_{IH}; V_{IO} = V_{CC} − V_{EE}; Switch Off (Figure 10)	5.0 5.0 5.0	−5.0 −5.0 −5.0	0.2 0.1 0.1	2.0 1.0 1.0	4.0 2.0 2.0	
I_{on}	Maximum On−Channel Leakage Current, Channel−to−Channel HCT4051A HCT4052A HCT4053A	V_{in} = V_{IL} or V_{IH}; Switch−to−Switch = V_{CC} − V_{EE}; (Figure 11)	5.0 5.0 5.0	−5.0 −5.0 −5.0	0.2 0.1 0.1	2.0 1.0 1.0	4.0 2.0 2.0	μA

AC CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Channel−Select to Analog Output (Figure 15)	2.0 3.0 4.5 6.0	270 90 59 45	320 110 79 65	350 125 85 75	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Analog Input to Analog Output (Figure 16)	2.0 3.0 4.5 6.0	40 25 12 10	60 30 15 13	70 32 18 15	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Enable to Analog Output (Figure 17)	2.0 3.0 4.5 6.0	160 70 48 39	200 95 63 55	220 110 76 63	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Enable to Analog Output (Figure 17)	2.0 3.0 4.5 6.0	245 115 49 39	315 145 69 58	345 155 83 67	ns
C_{in}	Maximum Input Capacitance, Channel−Select or Enable Inputs		10	10	10	pF
$C_{I/O}$	Maximum Capacitance (All Switches Off) Analog I/O		35	35	35	pF
	Common O/I: HCT4051A HCT4052A HCT4053A		130 80 50	130 80 50	130 80 50	
	Feed−through		1.0	1.0	1.0	

			Typical @ 25°C, V_{CC} = 5.0 V, V_{EE} = 0 V	
C_{PD}	Power Dissipation Capacitance (Figure 19)*	HCT4051A HCT4052A HCT4053A	45 80 45	pF

*Used to determine the no−load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0 V)

Symbol	Parameter	Condition	V_{CC} V	V_{EE} V	Limit* 25°C '51	'52	'53	Unit
BW	Maximum On−Channel Bandwidth or Minimum Frequency Response (Figure 12)	f_{in} = 1 MHz Sine Wave; Adjust f_{in} Voltage to Obtain 0 dBm at V_{OS}; Increase f_{in} Frequency Until dB Meter Reads −3 dB; R_L = 50 Ω, C_L = 10 pF	2.25 4.50 6.00	−2.25 −4.50 −6.00	80 80 80	95 95 95	120 120 120	MHz
–	Off−Channel Feed−through Isolation (Figure 13)	f_{in} = Sine Wave; Adjust f_{in} Voltage to Obtain 0 dBm at V_{IS} f_{in} = 10 kHz, R_L = 600 Ω, C_L = 50 pF	2.25 4.50 6.00	−2.25 −4.50 −6.00	−50 −50 −50			dB
		f_{in} = 1.0 MHz, R_L = 50 Ω, C_L = 10 pF	2.25 4.50 6.00	−2.25 −4.50 −6.00	−40 −40 −40			
–	Feedthrough Noise. Channel−Select Input to Common I/O (Figure 14)	V_{in} ≤ 1 MHz Square Wave (t_r = t_f = 6 ns); Adjust R_L at Setup so that I_S = 0 A; Enable = GND R_L = 600 Ω, C_L = 50 pF	2.25 4.50 6.00	−2.25 −4.50 −6.00	25 105 135			mV_{PP}
		R_L = 10 kΩ, C_L = 10 pF	2.25 4.50 6.00	−2.25 −4.50 −6.00	35 145 190			
–	Crosstalk Between Any Two Switches (Figure 18) (Test does not apply to HCT4051A)	f_{in} = Sine Wave; Adjust f_{in} Voltage to Obtain 0 dBm at V_{IS} f_{in} = 10 kHz, R_L = 600 Ω, C_L = 50 pF	2.25 4.50 6.00	−2.25 −4.50 −6.00	−50 −50 −50			dB
		f_{in} = 1.0 MHz, R_L = 50 Ω, C_L = 10 pF	2.25 4.50 6.00	−2.25 −4.50 −6.00	−60 −60 −60			
THD	Total Harmonic Distortion (Figure 20)	f_{in} = 1 kHz, R_L = 10 kΩ, C_L = 50 pF THD = $THD_{measured}$ − THD_{source} V_{IS} = 4.0 V_{PP} sine wave V_{IS} = 8.0 V_{PP} sine wave V_{IS} = 11.0 V_{PP} sine wave	2.25 4.50 6.00	−2.25 −4.50 −6.00	0.10 0.08 0.05			%

*Limits not tested. Determined by design and verified by qualification.

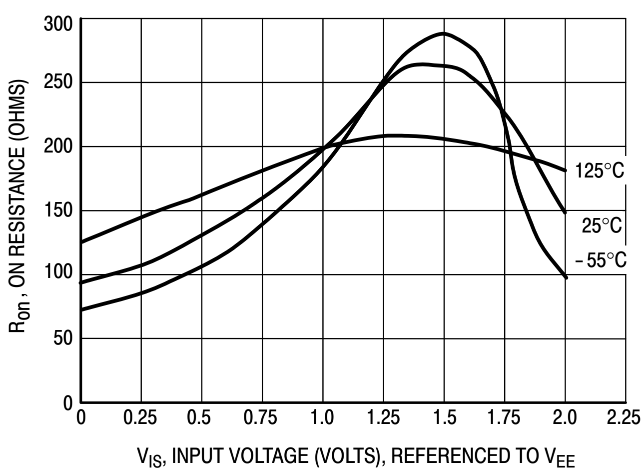


Figure 7a. Typical On Resistance, V_{CC} − V_{EE} = 2.0 V

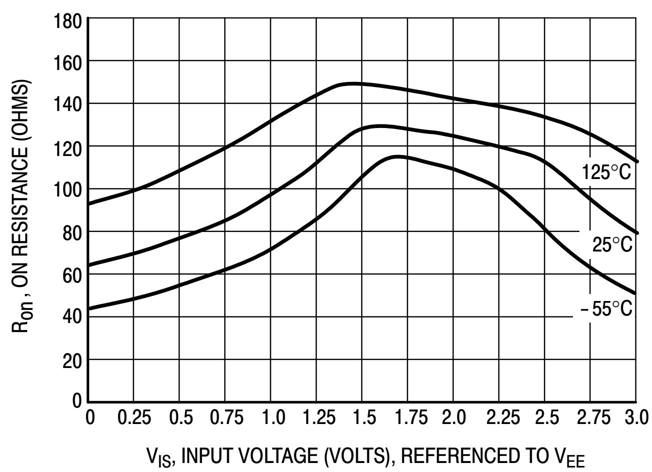


Figure 7b. Typical On Resistance, V_{CC} − V_{EE} = 3.0 V

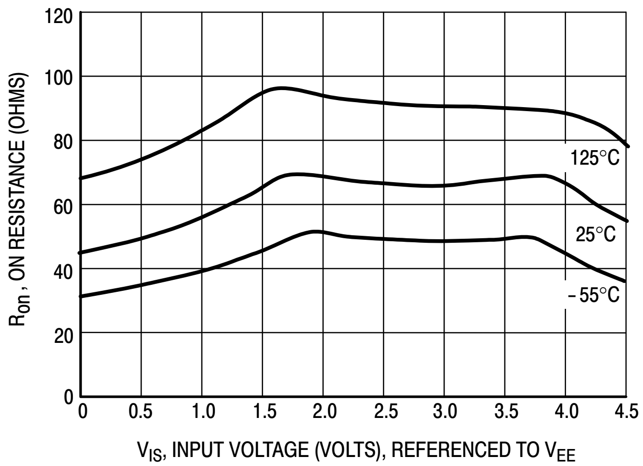


Figure 7c. Typical On Resistance, $V_{CC} - V_{EE}$ = 4.5 V

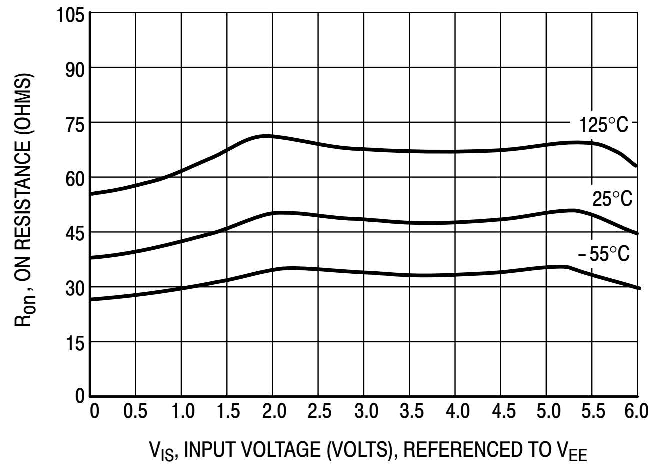


Figure 7d. Typical On Resistance, $V_{CC} - V_{EE}$ = 6.0 V

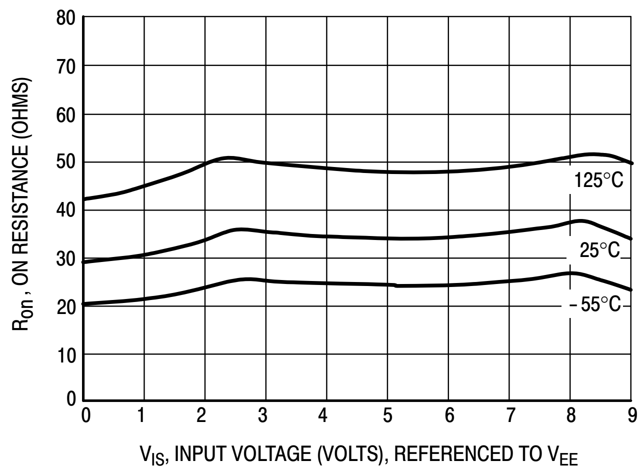


Figure 7e. Typical On Resistance, $V_{CC} - V_{EE}$ = 9.0 V

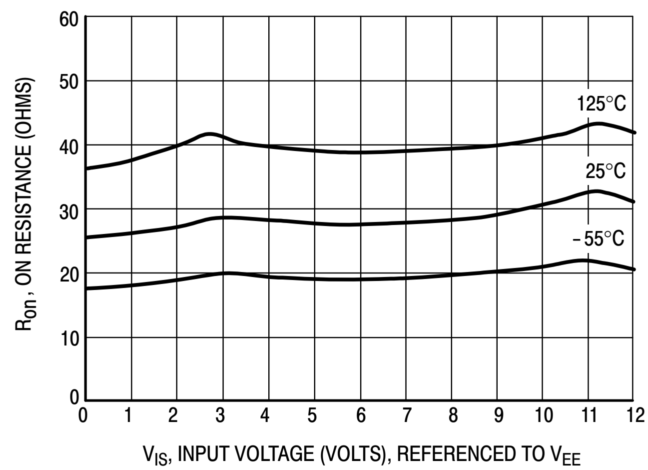


Figure 7f. Typical On Resistance, $V_{CC} - V_{EE}$ = 12.0 V

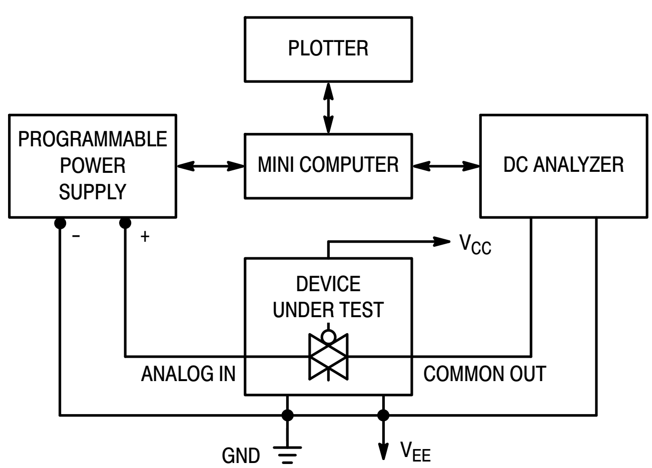


Figure 8. On Resistance Test Set−Up

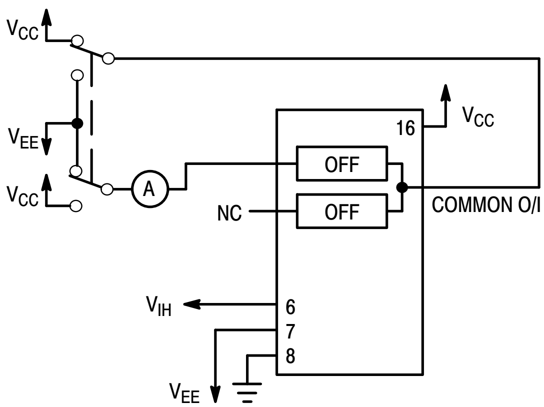


Figure 9. Maximum Off Channel Leakage Current, Any One Channel, Test Set−Up

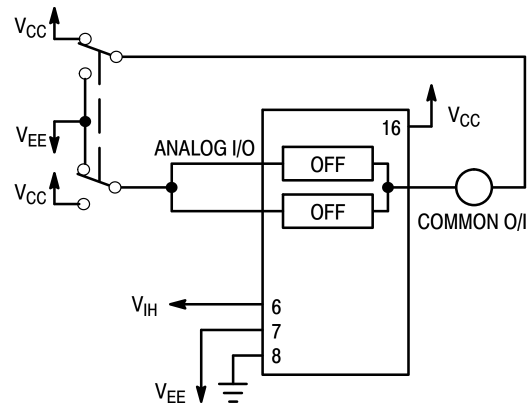


Figure 10. Maximum Off Channel Leakage Current, Common Channel, Test Set−Up

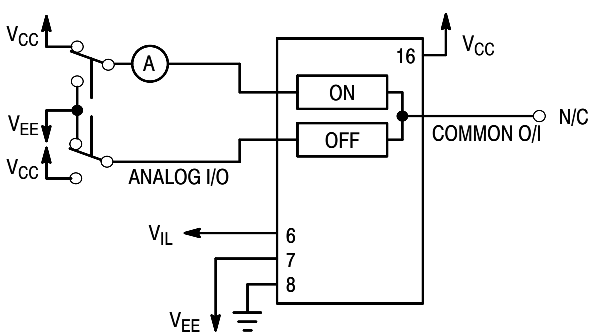
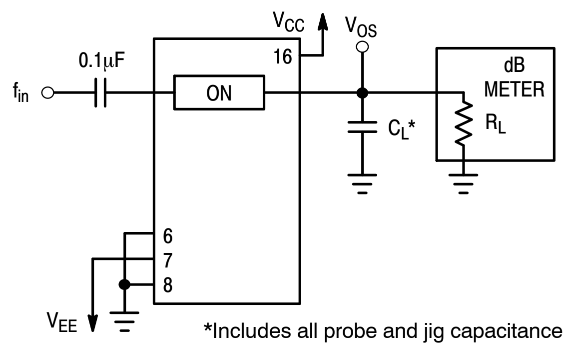
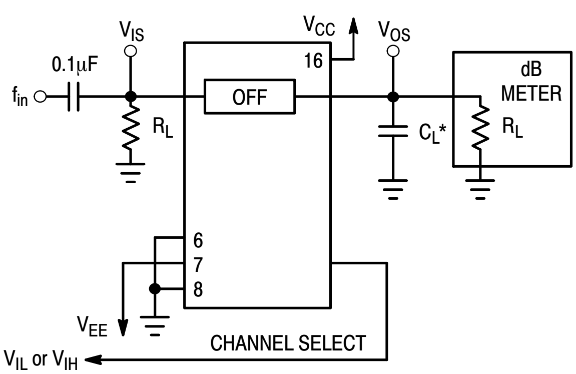


Figure 11. Maximum On Channel Leakage Current, Channel to Channel, Test Set−Up



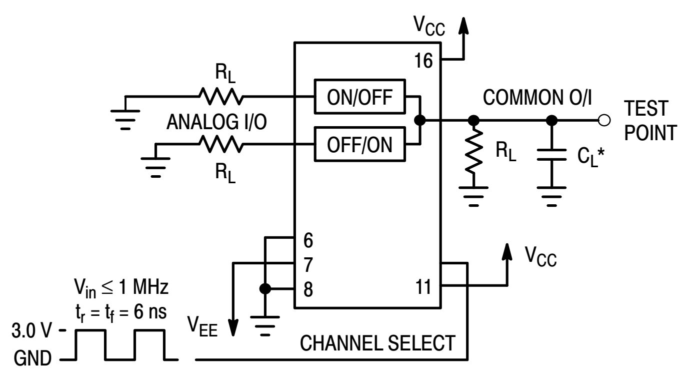
*Includes all probe and jig capacitance

Figure 12. Maximum On Channel Bandwidth, Test Set−Up



*Includes all probe and jig capacitance

Figure 13. Off Channel Feedthrough Isolation, Test Set−Up



*Includes all probe and jig capacitance

Figure 14. Feedthrough Noise, Channel Select to Common Out, Test Set−Up

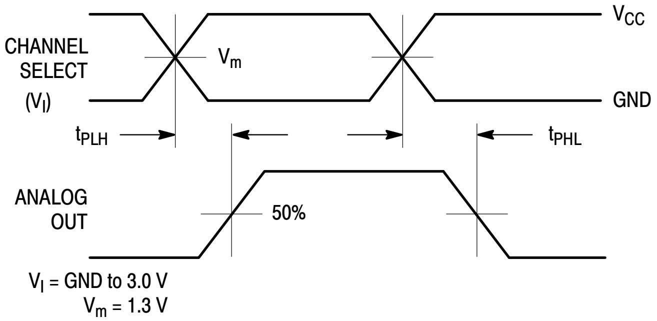
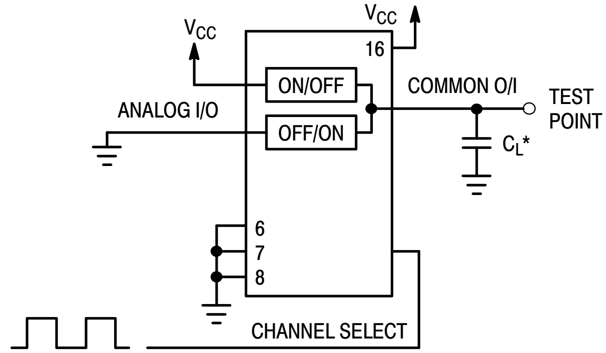


Figure 15a. Propagation Delays, Channel Select to Analog Out



*Includes all probe and jig capacitance

Figure 15b. Propagation Delay, Test Set−Up Channel Select to Analog Out

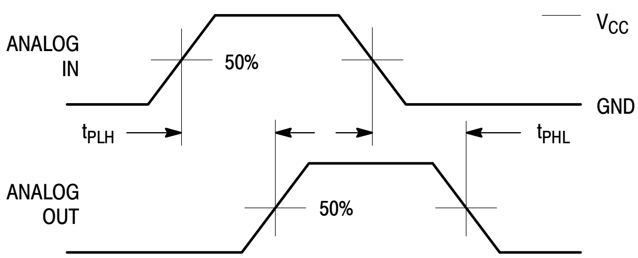
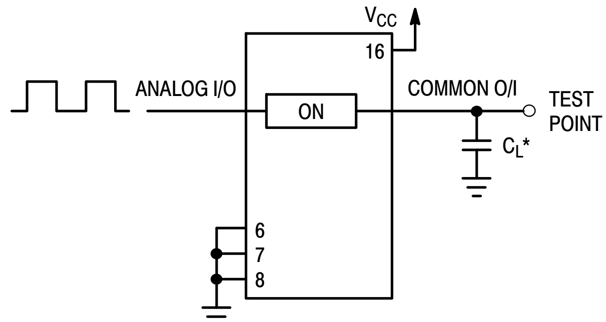


Figure 16a. Propagation Delays, Analog In to Analog Out



*Includes all probe and jig capacitance

Figure 16b. Propagation Delay, Test Set−Up Analog In to Analog Out

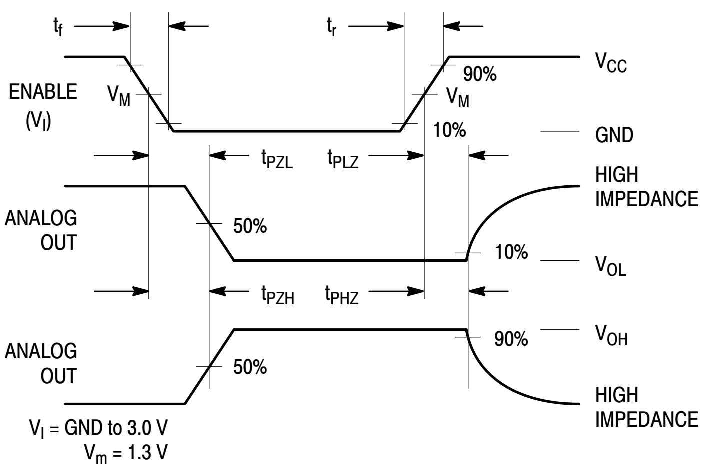


Figure 17a. Propagation Delays, Enable to Analog Out

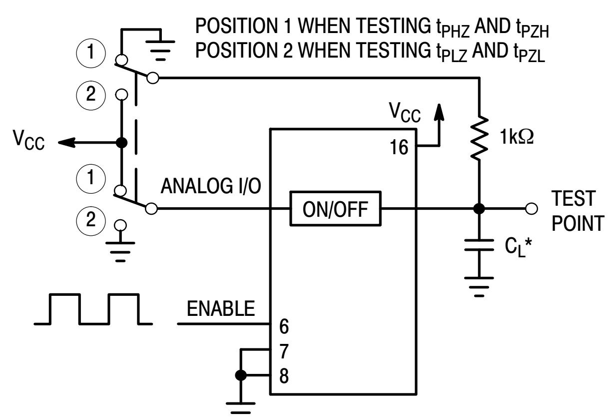
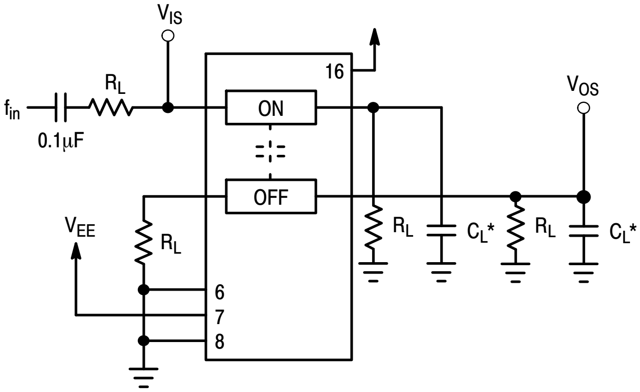


Figure 17b. Propagation Delay, Test Set−Up Enable to Analog Out



*Includes all probe and jig capacitance

Figure 18. Crosstalk Between Any Two Switches, Test Set−Up

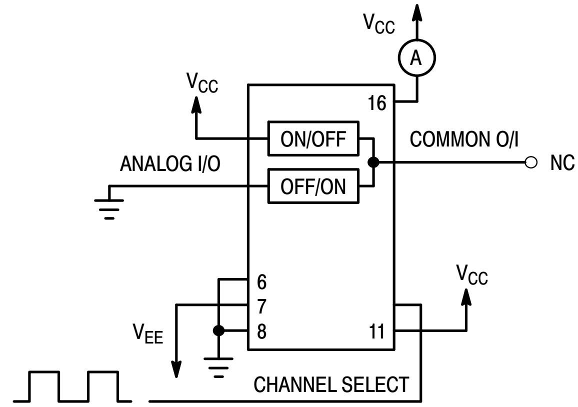
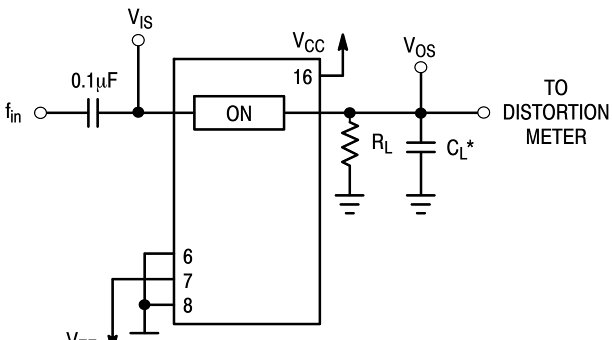


Figure 19. Power Dissipation Capacitance, Test Set−Up



*Includes all probe and jig capacitance

Figure 20a. Total Harmonic Distortion, Test Set−Up

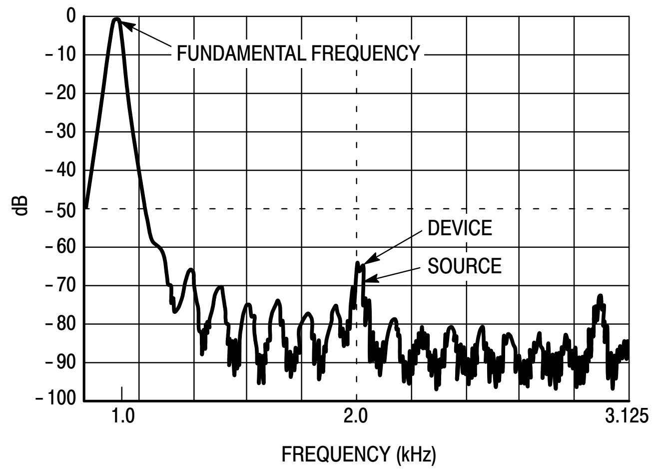


Figure 20b. Plot, Harmonic Distortion

APPLICATIONS INFORMATION

The maximum analog voltage swings are determined by the supply voltages V_{CC} and V_{EE}. The positive peak analog voltage should not exceed V_{CC}. Similarly, the negative peak analog voltage should not go below V_{EE}. In this example, the difference between V_{CC} and V_{EE} is ten volts. Therefore, using the configuration of Figure 21, a maximum analog signal of ten volts peak−to−peak can be controlled. Unused analog inputs/outputs may be left floating (i.e., not connected). However, tying unused analog inputs and outputs to V_{CC} or GND through a low value resistor helps minimize crosstalk and feed−through noise that may be picked up by an unused switch.

Although used here, balanced supplies are not a requirement. The only constraints on the power supplies are that:

$$V_{CC} - GND = 2 \text{ to } 6 \text{ V}$$
$$V_{EE} - GND = 0 \text{ to } -6 \text{ V}$$
$$V_{CC} - V_{EE} = 2 \text{ to } 12 \text{ V}$$
$$\text{and } V_{EE} \leq GND$$

When voltage transients above V_{CC} and/or below V_{EE} are anticipated on the analog channels, external Germanium or Schottky diodes (D_x) are recommended as shown in Figure 22. These diodes should be able to absorb the maximum anticipated current surges during clipping.

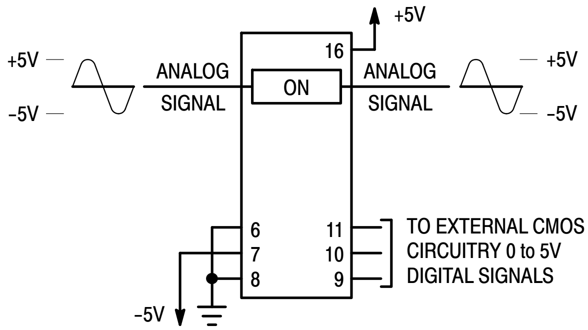


Figure 21. Application Example

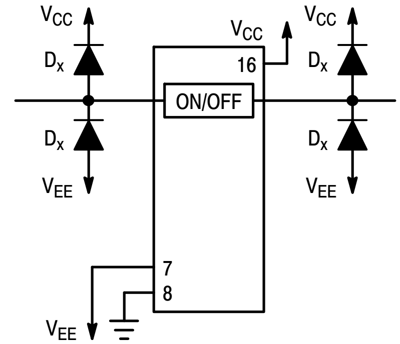
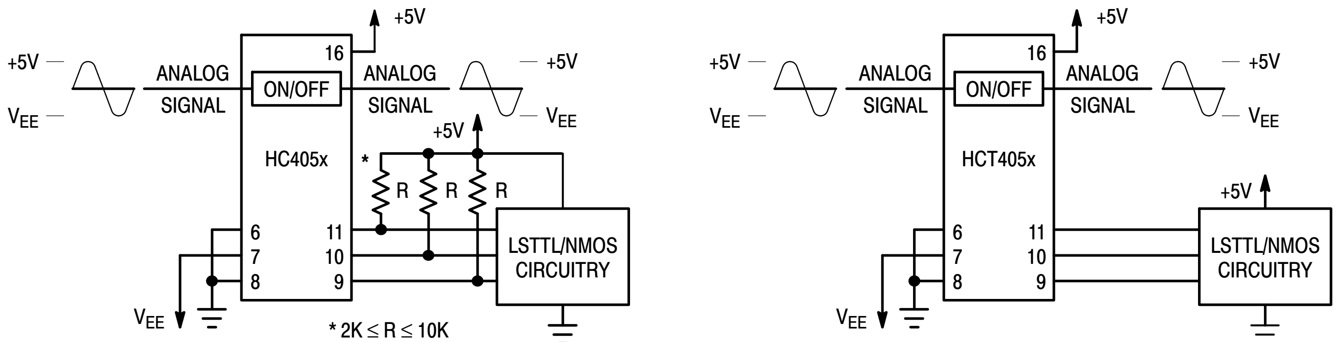


Figure 22. External Germanium or Schottky Clipping Diodes



a. Using Pull−Up Resistors with a HC Device

b. Using HCT Interface

Figure 23. Interfacing LSTTL/NMOS to CMOS Inputs

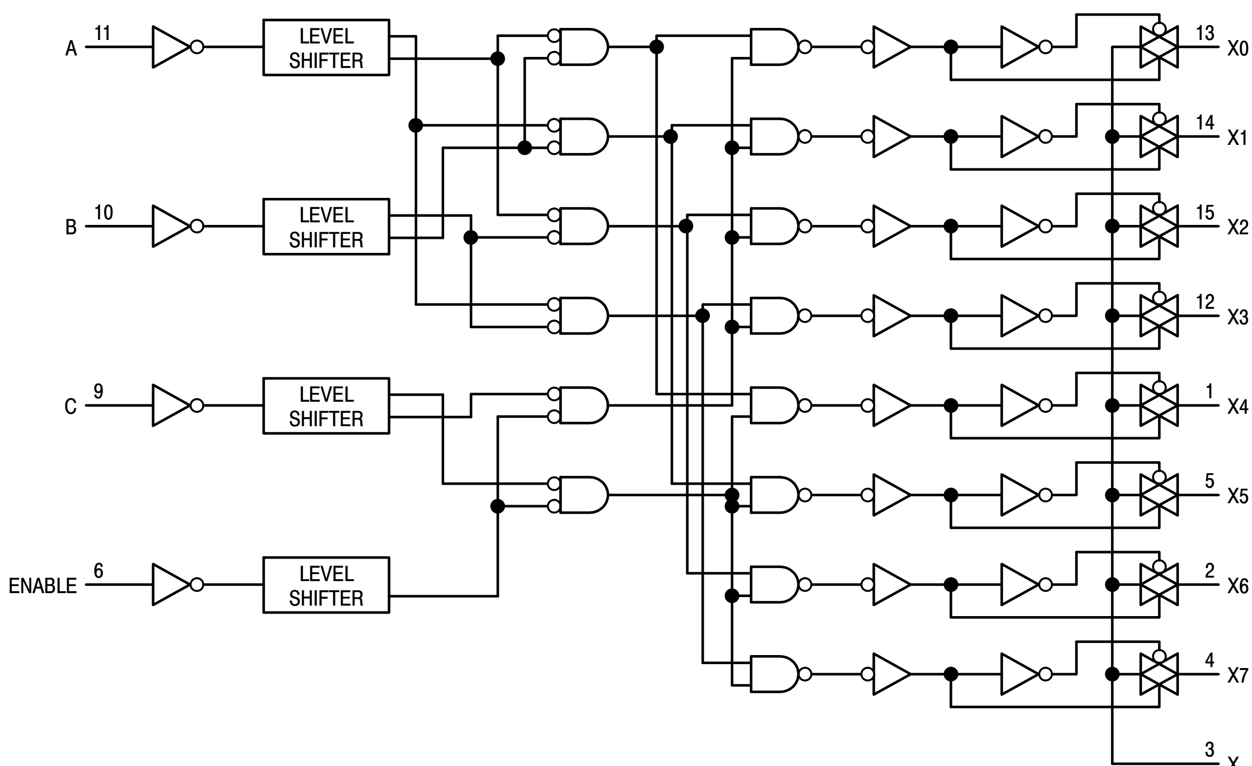


Figure 24. Function Diagram, HCT4051A

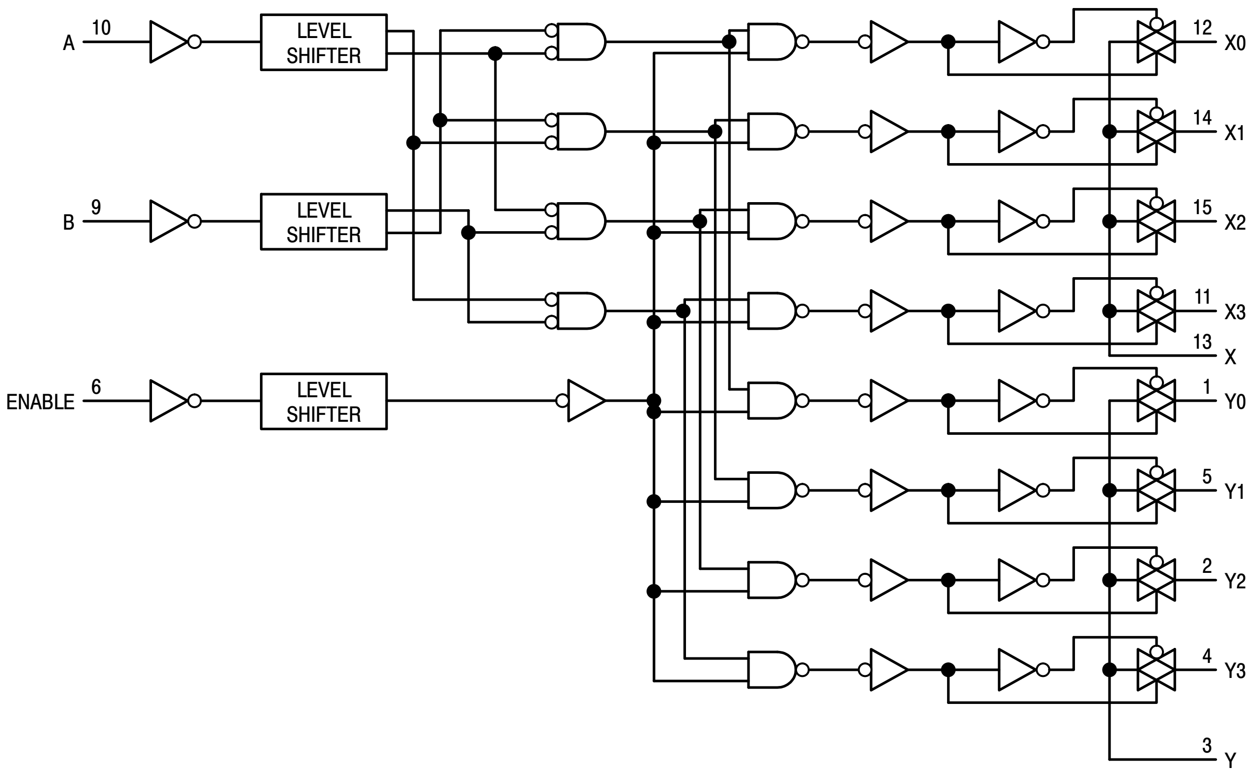


Figure 26. Function Diagram, HCT4052A

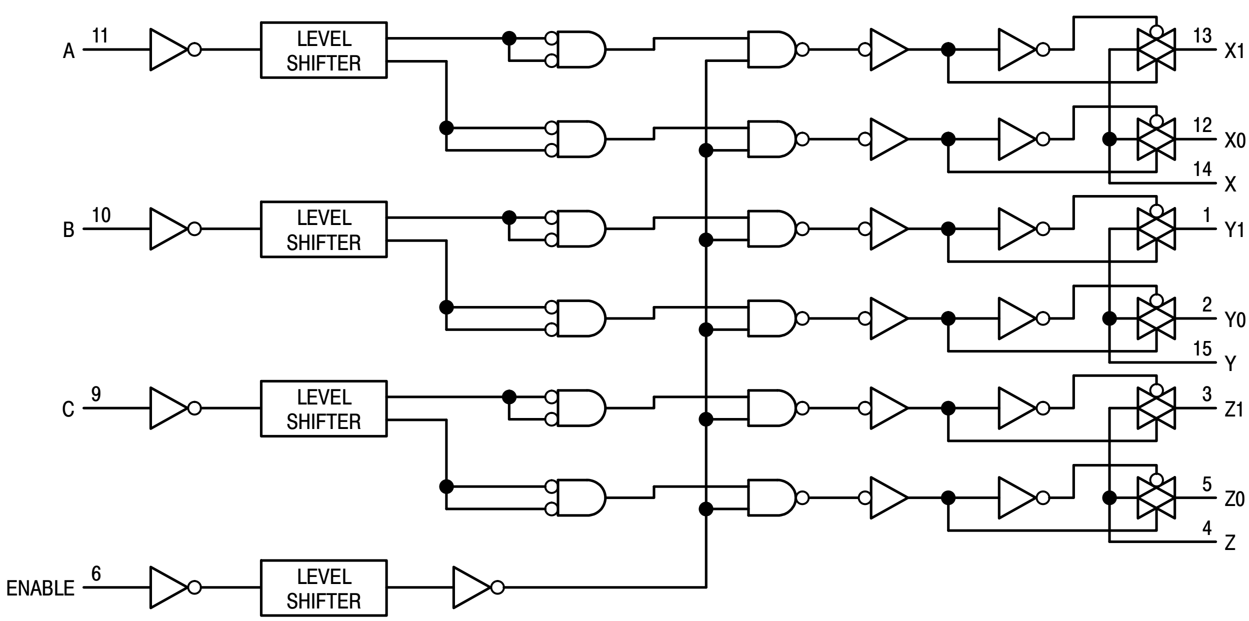


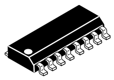
Figure 25. Function Diagram, HCT4053A

ORDERING INFORMATION

Device	Package	Shipping†
MC74HCT4051ADG	SOIC−16 (Pb−Free)	48 Units / Rail
MC74HCT4051ADR2G	SOIC−16 (Pb−Free)	2500 / Tape & Reel
MC74HCT4051ADTG	TSSOP−16 (Pb−Free)	96 Units / Rail
M74HCT4051ADTR2G	TSSOP−16 (Pb−Free)	2500 / Tape & Reel
NLV74HCT4051ADTR2G*	TSSOP−16 (Pb−Free)	2500 / Tape & Reel
MC74HCT4052ADR2G	SOIC−16 (Pb−Free)	2500 / Tape & Reel
M74HCT4052ADTR2G	TSSOP−16 (Pb−Free)	2500 / Tape & Reel
MC74HCT4053ADR2G	SOIC−16 (Pb−Free)	2500 / Tape & Reel
M74HCT4053ADTR2G	TSSOP−16 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

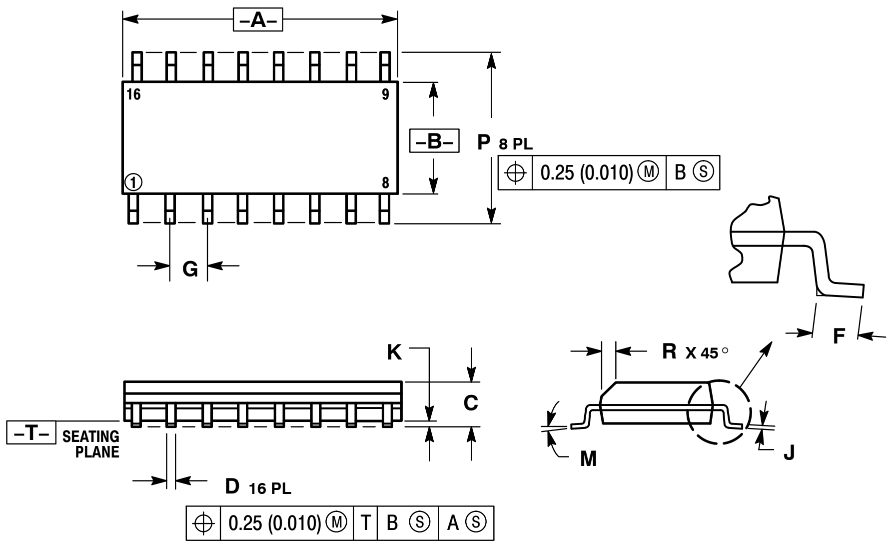
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.



SCALE 1:1

SOIC−16
CASE 751B−05
ISSUE K

DATE 29 DEC 2006



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR
15. EMITTER
16. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION
4. CATHODE
5. CATHODE
6. NO CONNECTION
7. ANODE
8. CATHODE
9. CATHODE
10. ANODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. NO CONNECTION
15. ANODE
16. CATHODE

STYLE 3:
PIN 1. COLLECTOR, DYE #1
2. BASE, #1
3. EMITTER, #1
4. COLLECTOR, #1
5. COLLECTOR, #2
6. BASE, #2
7. EMITTER, #2
8. COLLECTOR, #2
9. COLLECTOR, #3
10. BASE, #3
11. EMITTER, #3
12. COLLECTOR, #3
13. COLLECTOR, #4
14. BASE, #4
15. EMITTER, #4
16. COLLECTOR, #4

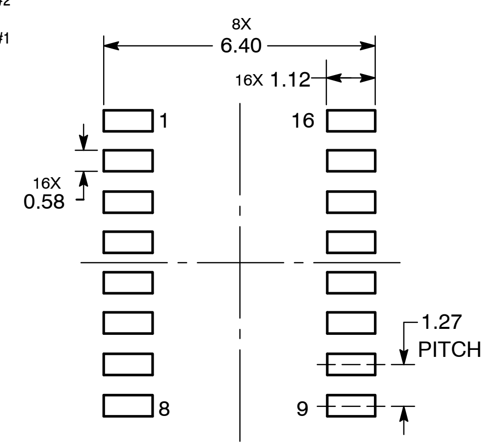
STYLE 4:
PIN 1. COLLECTOR, DYE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. EMITTER, #4
11. BASE, #3
12. EMITTER, #3
13. BASE, #2
14. EMITTER, #2
15. BASE, #1
16. EMITTER, #1

STYLE 5:
PIN 1. DRAIN, DYE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. DRAIN, #3
6. DRAIN, #3
7. DRAIN, #4
8. DRAIN, #4
9. GATE, #4
10. SOURCE, #4
11. GATE, #3
12. SOURCE, #3
13. GATE, #2
14. SOURCE, #2
15. GATE, #1
16. SOURCE, #1

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 7:
PIN 1. SOURCE N-CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE P-CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. SOURCE P-CH
9. SOURCE P-CH
10. COMMON DRAIN (OUTPUT)
11. COMMON DRAIN (OUTPUT)
12. COMMON DRAIN (OUTPUT)
13. GATE N-CH
14. COMMON DRAIN (OUTPUT)
15. COMMON DRAIN (OUTPUT)
16. SOURCE N-CH

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

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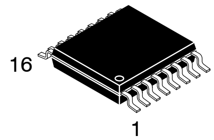
DESCRIPTION:	SOIC−16	PAGE 1 OF 1

MECHANICAL CASE OUTLINE

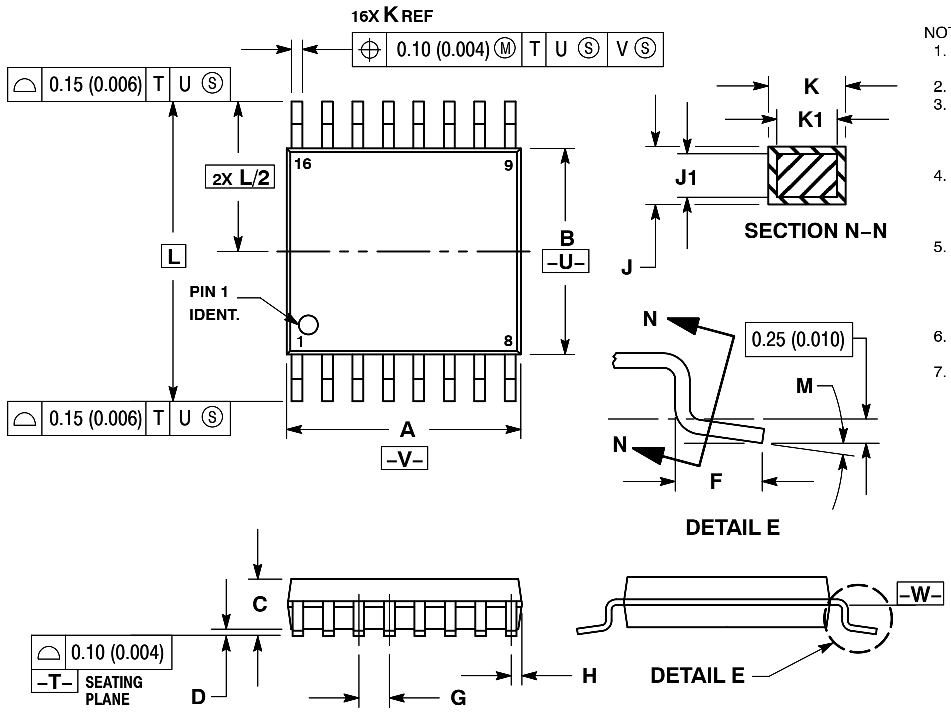
PACKAGE DIMENSIONS



SCALE 2:1

TSSOP−16
CASE 948F−01
ISSUE B

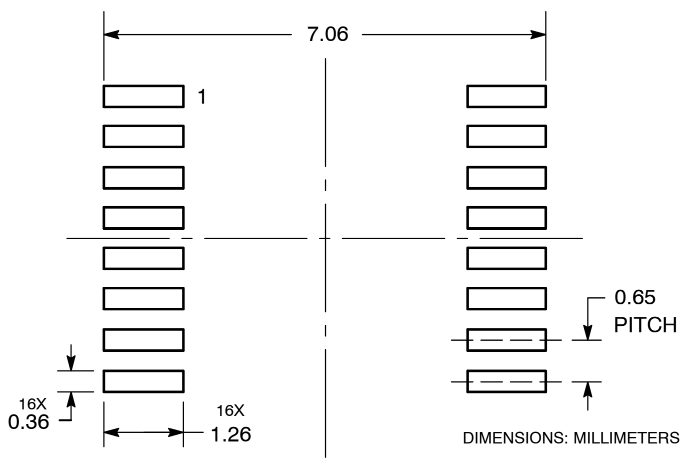
DATE 19 OCT 2006



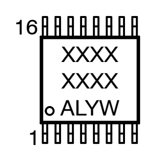
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT



GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
G or ▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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