SGM829
Low Quiescent Current, Programmable Delay Supervisory Circuit

GENERAL DESCRIPTION

The SGM829 family can monitor system voltages from 1.8V to 5V. When the V_{DD} voltage drops below a preset threshold (V_{IT}) or the manual reset (nMR) pin is driven low, the open-drain nRESET output is asserted. After the V_{DD} voltage and nMR voltage return above their respective thresholds, the nRESET output remains low within the user-adjustable delay time.

The SGM829 uses a precision reference to achieve 1% threshold accuracy. The reset timeout period can be set to 0.29ms by leaving the SRT pin open, or can be programmed from 1.25ms to 10s by connecting the SRT pin to an external capacitor. Low quiescent current makes SGM829 very suitable for battery-powered applications.

The SGM829 is available in a Green SOT-23-5 package.

FEATURES

- **Adjustable Reset Timeout Period: 1.25ms to 10s**
- **Low Quiescent Current: 0.6μA (TYP)**
- **High Threshold Accuracy: 1% (TYP)**
- **Factory-Set Detection Voltages from 1.8V to 5V**
- **Manual Reset (nMR) Input**
- **Open-Drain nRESET Output**
- **Available in a Green SOT-23-5 Package**

APPLICATIONS

Portable and Battery-Powered Products
FPGA and ASIC Applications
DSP or Microcontroller Applications
Notebook and Desktop Computers

TYPICAL APPLICATION

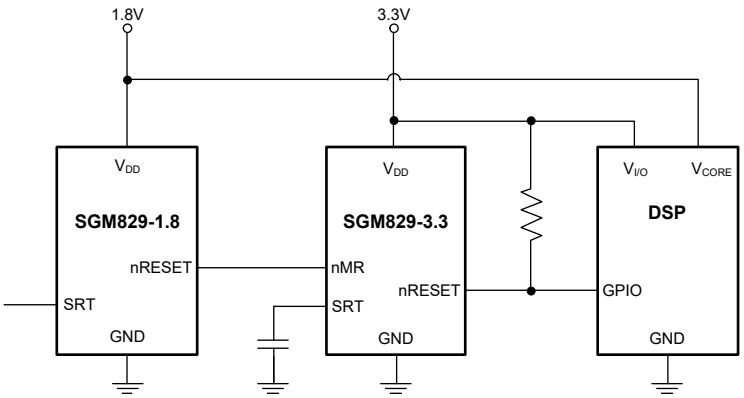


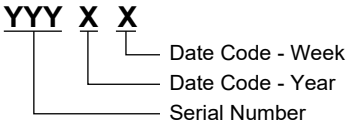
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	THRESHOLD VOLTAGE (V_{IT}) (V)	PACKAGE DESCRIPTION	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM829-1.8	1.67	SOT-23-5	SGM829-1.8XN5G/TR	R70XX	Tape and Reel, 3000
SGM829-1.9	1.77	SOT-23-5	SGM829-1.9XN5G/TR	R72XX	Tape and Reel, 3000
SGM829-2.5	2.33	SOT-23-5	SGM829-2.5XN5G/TR	R75XX	Tape and Reel, 3000
SGM829-2.7	2.52	SOT-23-5	SGM829-2.7XN5G/TR	R77XX	Tape and Reel, 3000
SGM829-2.9	2.7	SOT-23-5	SGM829-2.9XN5G/TR	R79XX	Tape and Reel, 3000
SGM829-3.0	2.79	SOT-23-5	SGM829-3.0XN5G/TR	R3CXX	Tape and Reel, 3000
SGM829-3.3	3.07	SOT-23-5	SGM829-3.3XN5G/TR	R7BXX	Tape and Reel, 3000
SGM829-3.7	3.45	SOT-23-5	SGM829-3.7XN5G/TR	R7DXX	Tape and Reel, 3000
SGM829-4.0	3.73	SOT-23-5	SGM829-4.0XN5G/TR	R7FXX	Tape and Reel, 3000
SGM829-4.5	4.2	SOT-23-5	SGM829-4.5XN5G/TR	R81XX	Tape and Reel, 3000
SGM829-5.0	4.65	SOT-23-5	SGM829-5.0XN5G/TR	R83XX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XX = Date Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ..... -0.3V to 7V
SRT to GND ..... -0.3V to V_{DD} + 0.3V
nRESET, nMR to GND ..... -0.3V to 7V
nRESET Pin Current ..... ±5mA
Package Thermal Resistance
SOT-23-5, θ_{JA} ..... 245℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 4000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Input Supply Voltage Range, V_{DD} ..... 1.65V to 6.5V
SRT Pin Voltage, V_{SRT} ..... V_{DD} (MAX)
nMR Pin Voltage, V_{nMR} ..... 0V to 6.5V
nRESET Pin Voltage, V_{nRESET} ..... 0V to 6.5V
nRESET Pin Current, I_{nRESET} ..... 0.0003mA to 5mA
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

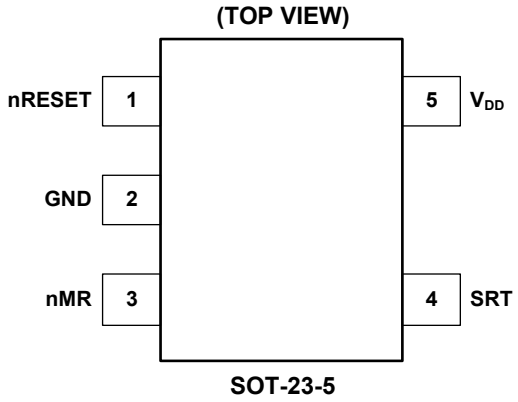
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	I/O	FUNCTION
1	nRESET	O	Active-Low Reset Output. When the V_{DD} input is lower than V_{IT} or the nMR pin is set to logic low, nRESET is asserted and driven to a low-impedance state. nRESET remains low (asserted) for the reset timeout period after both V_{DD} exceeds V_{IT} and nMR pin is driven high. A pull-up resistor from 10kΩ to 1MΩ should be used on this pin and allows the reset pin to attain voltages higher than V_{DD}.
2	GND	—	Ground.
3	nMR	I	Manual Reset Input Pin. Pulling this pin (nMR) low will assert nRESET. nMR is internally pulled up to V_{DD} by a 100kΩ resistor.
4	SRT	I	Set Reset Timeout Input. Connect a capacitor between SRT and ground to set the timeout period. The pin can be left open, but it cannot be connected to V_{DD}. Determine the period as follows: T_D (μs) = (2.8×10^6) × C_{SRT} (μF) + 290μs.
5	V_{DD}	I	Supply Voltage. It is recommended to place a 0.1μF ceramic capacitor close to this pin.

NOTE: I: input, O: output.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 1.65V to 6.5V, R_{LRESET} = 100kΩ (1), T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply Voltage Range	V_{DD}		1.65		6.5	V
Supply Current (Current into V_{DD} Pin)	I_{DD}	V_{DD} = 3.3V, nRESET not asserted, nMR, nRESET, SRT open		0.6	1.5	μA
		V_{DD} = 6.5V, nRESET not asserted, nMR, nRESET, SRT open		0.9	2	
Low-Level Output Voltage	V_{OL}	1.3V ≤ V_{DD} < 1.8V, I_{OL} = 0.4mA			0.2	V
		1.8V ≤ V_{DD} ≤ 6.5V, I_{OL} = 1mA			0.3	
Power-On Reset Voltage	V_{POR}	V_{OL_MAX} = 0.2V, I_{nRESET} = 15μA			0.8	V
Negative-Going Input Threshold Accuracy	V_{IT}	T_J = +25℃	-1.0		1.0	%
		T_J = -40℃ to +85℃	-1.3		1.3	
Hysteresis on V_{IT} (2)	V_{HYS}			50 × V_{IT}		mV
V_{DD} Drop to Reset Delay	t_{RP0}	Drop = V_{IT} - 250mV, T_J = -40℃ to +85℃		85		μs
nMR Internal Pull-Up Resistance	R_{nMR}	T_J = -40℃ to +85℃		100		kΩ
nMR Input	V_{IH}	Logic high	0.7 × V_{DD}			V
	V_{IL}	Logic low			0.3 × V_{DD}	
Input Capacitance, Any Pin	C_{IN}	SRT pin, V_{IN} = 0V to V_{DD}, T_J = -40℃ to +85℃		5		pF
		Other pins, V_{IN} = 0V to 6.5V, T_J = -40℃ to +85℃		5		
nMR Glitch Rejection		T_J = -40℃ to +85℃		100		ns
nMR to Reset Propagation Delay	t_{nMR}	T_J = -40℃ to +85℃		240		ns
Reset Timeout Period	t_D	SRT open	0.15	0.29	0.40	ms
		C_{SRT} = 1nF	1.5	2.8	4.0	
SRT Source Current	I_{RAMP}	T_J = -40℃ to +85℃		430		nA
SRT Source Threshold Voltage	$V_{TH-RAMP}$	T_J = -40℃ to +85℃		1.205		V

NOTES:

1. R_{LRESET} is the resistor connected to the nRESET pin.
2. Guaranteed by design and not tested in production.

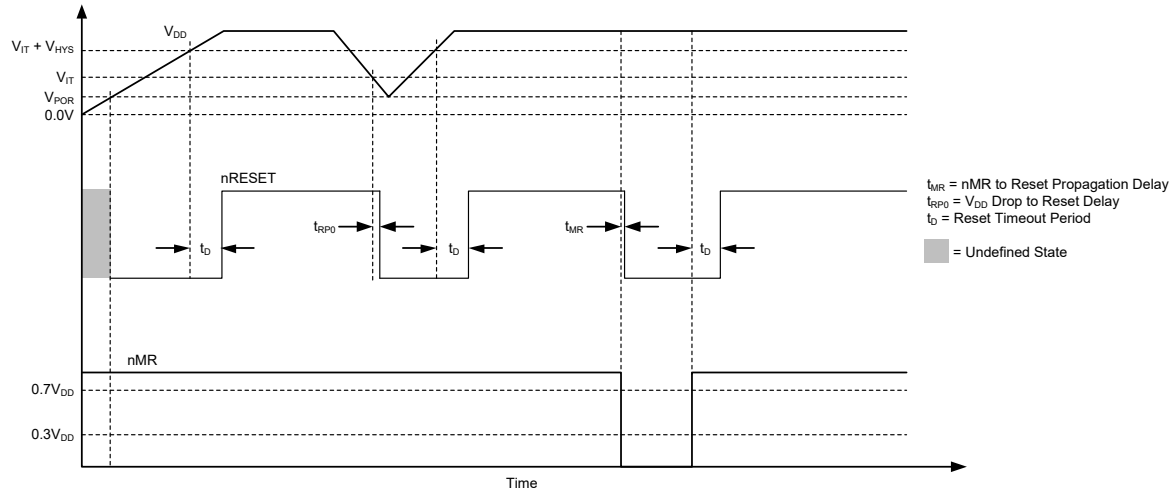
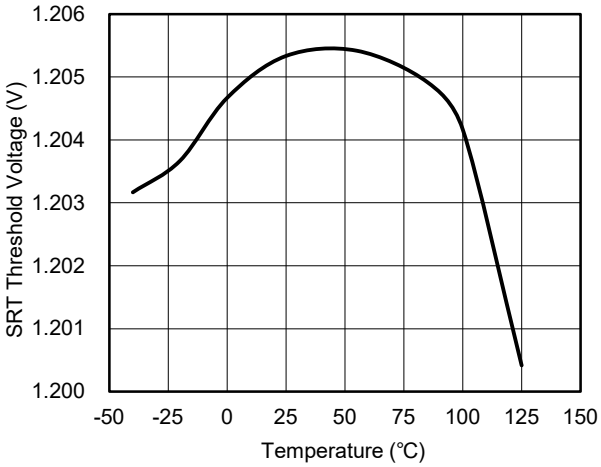


Figure 2. SGM829 Timing Diagram Showing nMR and V_{DD} Reset Timing

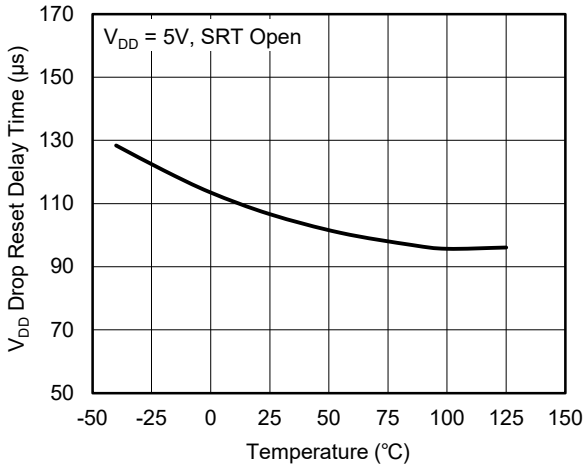
TYPICAL PERFORMANCE CHARACTERISTICS

Test for SGM829-3.0 only, T_J = +25℃, unless otherwise noted.

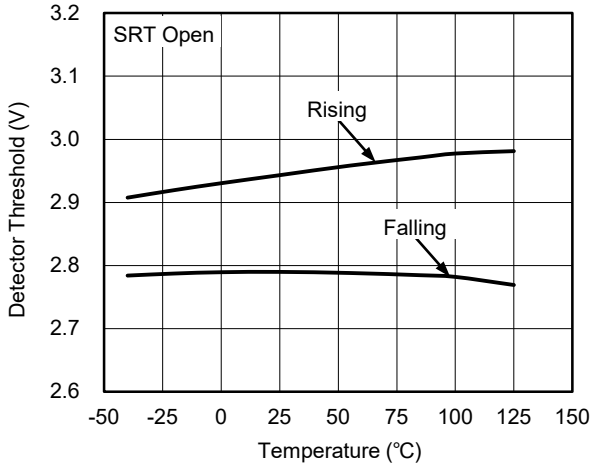
SRT Threshold Voltage vs. Temperature



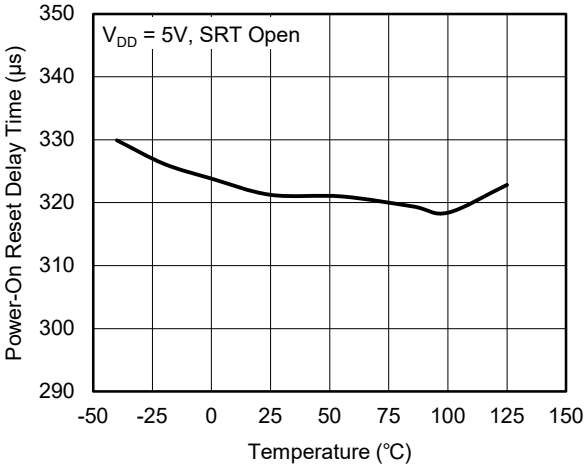
V_{DD} Drop Reset Delay Time vs. Temperature



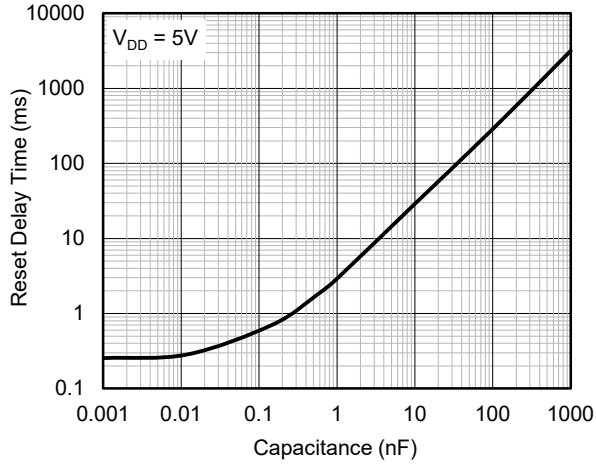
Detector Threshold vs. Temperature



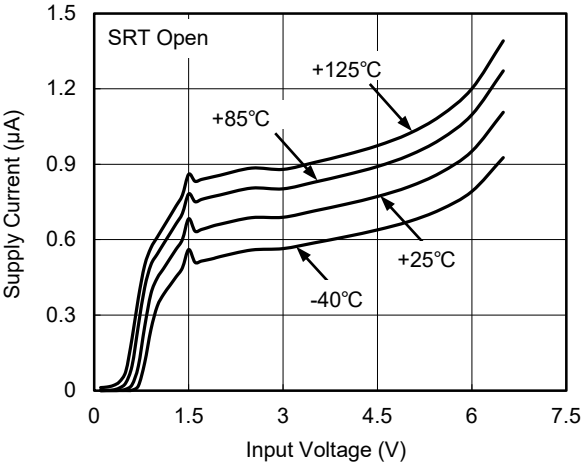
Power-On Reset Delay Time vs. Temperature



Reset Delay Time vs. Capacitance



Supply Current vs. Input Voltage



FUNCTIONAL BLOCK DIAGRAM

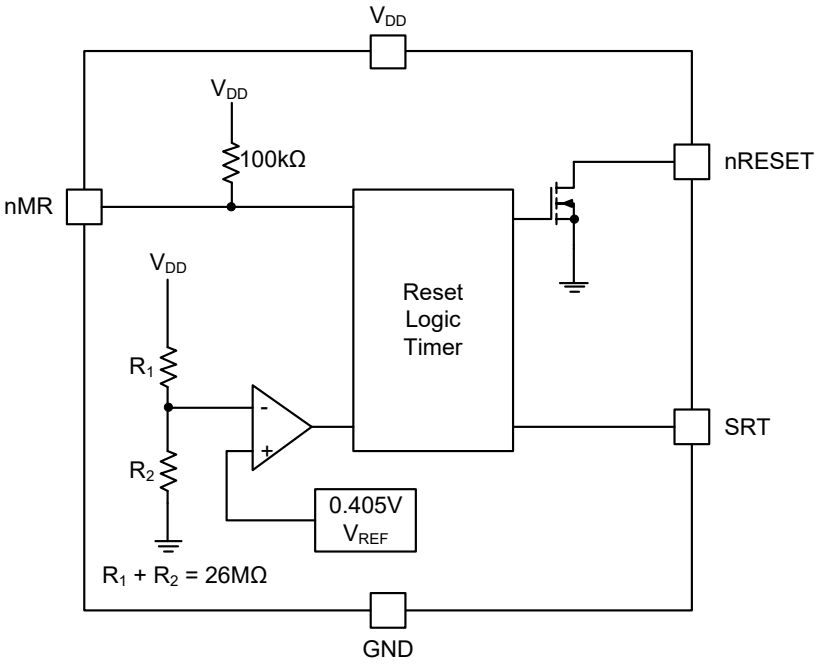


Figure 3. Functional Block Diagram

DETAILED DESCRIPTION

When the V_{DD} voltage drops below V_{IT} or the nMR pin is driven low, the open-drain nRESET output is asserted. After the V_{DD} voltage and nMR voltage return above their respective thresholds, the nRESET output remains low within the user-adjustable delay time.

Feature Description

The SGM829 device has a reset delay time adjustment function and a wide range of detection thresholds, so it can be widely used in a various applications. The detection threshold voltages are factory-set from 1.8V to 5V. In addition, connecting a capacitor between SRT pin and ground allows a programmable reset timeout period from 1.25ms to 10s.

Selecting the Reset Delay Time

When the V_{DD} voltage exceeds the V_{DD} threshold voltage, a current source will start to charge the SRT capacitor and the SRT voltage will rise. When the SRT voltage exceeds 1.205V, the nRESET voltage will change from low to high.

Therefore, there is a delay time between the point of V_{DD} reaching its threshold voltage and the nRESET active-high point. The delay time can be calculated according to the following equation:

$$T_D\,(\mu s) = (2.8 \times 10^6) \times C_{SRT}\,(\mu F) + 290\mu s \quad (1)$$

Manual Reset (nMR) Input

The nMR input allows a processor or other logic circuits to initiate a reset. When nMR is set to logic low ($0.3V_{DD}$), the nRESET is asserted. After nMR returns to logic high and V_{DD} exceeds its reset threshold, nRESET is deasserted after the user-defined reset delay expires. Note that nMR is internally connected to V_{DD} through a 100kΩ resistor, so if nMR is not used, this pin can be left open.

Figure 4 shows how to use nMR to monitor multiple system voltages. Note that if the logic signal does not drive nMR fully to V_{DD}, there will be some extra current drawn into V_{DD} due to an internal pull-up resistor on nMR. To minimize current draw, an external FET can be used as shown in Figure 5.

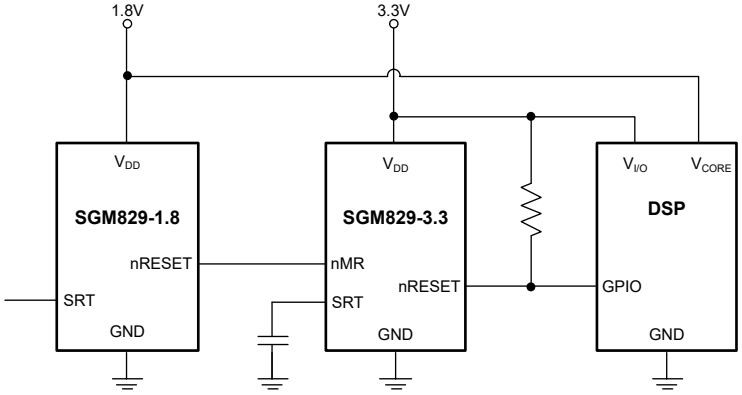


Figure 4. Using nMR to Monitor Multiple System Voltages

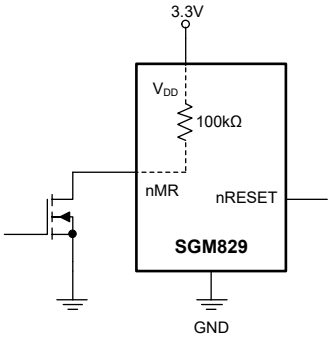


Figure 5. Using an External MOSFET to Minimize I_{DD} When nMR Signal Does not Go to V_{DD}

DETAILED DESCRIPTION (continued)

nRESET Output

As long as V_{DD} voltage exceeds V_{IT} and the nMR is logic high, nRESET remains high (deasserted). If either V_{DD} is lower than V_{IT} or nMR is driven low, nRESET is asserted, driving the nRESET pin to a low-impedance state.

Once the nMR is logic high again and V_{DD} voltage exceeds V_{IT} + V_{HYS}, a delay circuit is enabled, keeping nRESET low for a specified reset delay period. Once the reset delay has expired, the nRESET pin enters a high-impedance state. The pull-up resistor from the nRESET pin to the power supply can be used to reset the microprocessor signal to have a voltage above V_{DD} voltage. The pull-up resistor should be no smaller than 10kΩ due to the limited nRESET pull-down ability.

Device Functional Modes

Table 1. Truth Table

nMR	$V_{DD} > V_{IT}$	nRESET
L	0	L
L	1	L
H	0	L
H	1	H

Normal Operation ($V_{DD} > V_{DD\_MIN}$)

When the V_{DD} voltage is higher than V_{DD_MIN}, the logic state of nRESET is determined by V_{DD} and the logic state of nMR.

• nMR high: When V_{DD} voltage is higher than 1.65V for a selected time (t_D), the nRESET logic state corresponds to V_{DD} relative to V_{IT}.

• nMR low: In this mode, nRESET is held low regardless of V_{DD} voltage.

Above Power-On Reset but Lower than V_{DD_MIN} ($V_{POR} < V_{DD} < V_{DD\_MIN}$)

When the V_{DD} voltage is lower than V_{DD_MIN} and higher than the power-on reset voltage (V_{POR}), the nRESET is asserted and driven to a low-impedance state.

Below Power-On Reset ($V_{DD} < V_{POR}$)

When the V_{DD} voltage is lower than the required voltage (V_{POR}), the nRESET voltage is undefined. In the case of nRESET pulling up to V_{DD} through a 100kΩ resistor, nRESET voltage is equal to or lower than V_{DD} voltage.

APPLICATION INFORMATION

Figure 6 shows a typical application of the SGM829-2.5 used with a 2.5V processor. The nRESET output is typically connected to the nRESET input of a microprocessor. A pull-up resistor is necessary to keep the nRESET logic high when nRESET is not asserted.

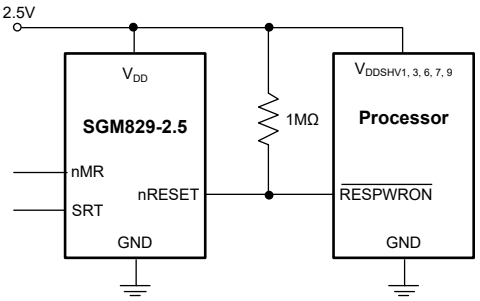


Figure 6. Typical Application of the SGM829 with a Processor

Design Requirements

The SGM829 is intended to drive the nRESET input of a microprocessor. The nRESET pin is pulled high with a 1MΩ resistor and the reset timeout period is programmed by SRT pin. Leaving SRT open will offer a typical reset timeout period of 0.29ms.

Detailed Design Procedure

The primary constraint for this application is the reset timeout period. In this case, because SRT is open, the reset timeout period is set to 0.29ms. A 0.1μF decoupling capacitor is connected to the V_{DD} pin and a 1MΩ resistor is used to pull the nRESET pin high.

Power Supply Recommendations

The device is designed to operate from an input supply with a voltage range from 1.65V to 6.5V.

Layout Guidelines

It is recommended to place a 0.1μF ceramic capacitor near the V_{DD} pin. If there is no capacitor connected to the SRT pin, parasitic capacitance on this pin should be minimized so the nRESET delay time is not significantly affected.

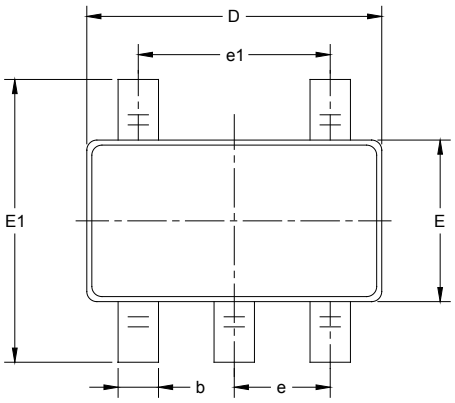
REVISION HISTORY

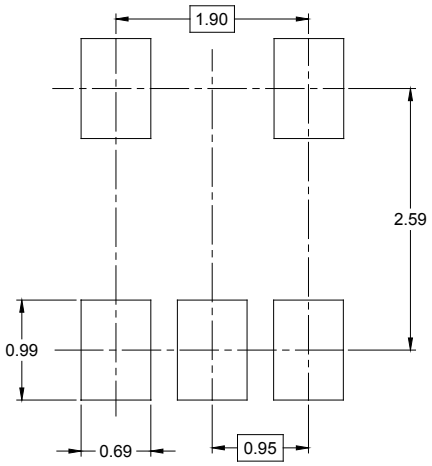
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (MAY 2021) to REV.A	Page
Changed from product preview to production data	All

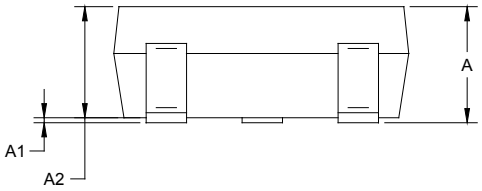
PACKAGE OUTLINE DIMENSIONS

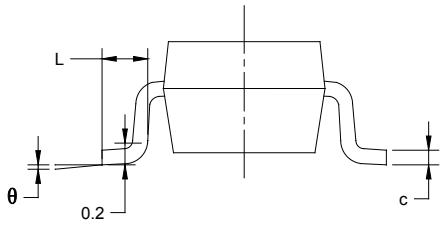
SOT-23-5





RECOMMENDED LAND PATTERN (Unit: mm)

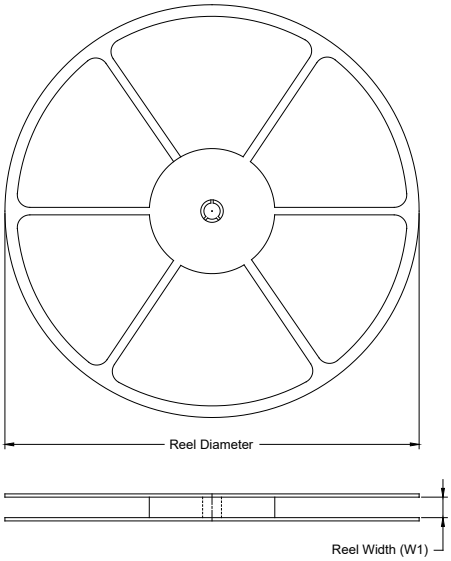




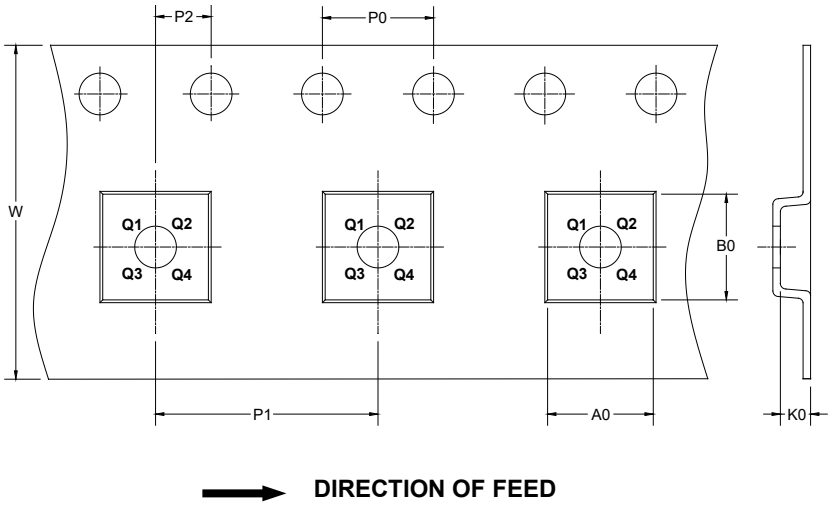
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950 BSC		0.037 BSC	
e1	1.900 BSC		0.075 BSC	
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



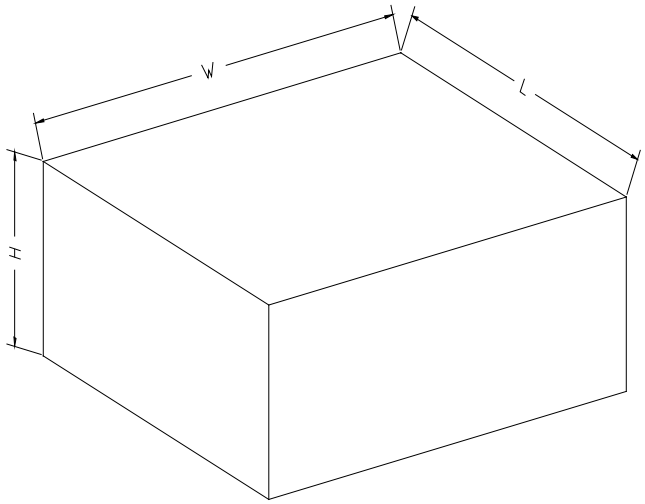
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT-23-5	7″	9.5	3.20	3.20	1.40	4.0	4.0	2.0	8.0	Q3

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002