SGM90516

High-Density, 12-Bit Analog Monitor and Control Solution with Multichannel ADC, Bipolar DACs, Temperature Sensor, and GPIO Ports

GENERAL DESCRIPTION

The SGM90516 is a high integrated analog front end, which includes 12-bit 16 channels digital-to-analog converters (DACs), a 12-bit 21 channels inputs successive approximation (SAR) analog-to-digital converter (ADC), a temperature sensor and an on-chip reference.

The chip also has 8 channels general purpose inputs and outputs (GPIOs). These pins are configurable for ADC inputs or GPIOs.

The chip is operated by a 4-wire SPI-compatible interface.

The SGM90516 is available in a Green TQFP-10×10-64L (Exposed Pad) package. It is specified from -40℃ to +125℃.

APPLICATIONS

Active Antenna System mMIMO
Distributed Antenna Systems
Macro Remote Radio Unit
Radar
Outdoor Backhaul Unit
Data Acquisition Systems

FEATURES

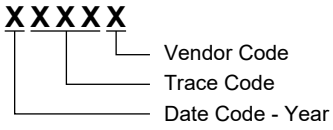
- **16 Monotonic 12-Bit DACs**
  - **Programmable Voltage Ranges: -10V to 0V, -5V to 0V, 0V to 5V, and 0V to 10V**
  - **High Current Drive Capability: up to ±15mA**
  - **Auto-Range Detector**
  - **Selectable Clamp Voltage**
- **12-Bit SAR ADC**
  - **21 External Analog Inputs**
    16 Bipolar Inputs: -12.5V to +12.5V
    5 High-Precision Inputs: 0V to 5V
  - **Programmable Out-of-Range Alarms**
- **Internal 2.5V Reference**
- **Internal Temperature Sensor**
  - **-40℃ to +125℃ Operation**
  - **±3℃ Accuracy**
- **Eight General-Purpose I/O Ports (GPIOs)**
  - **Low-Power SPI-Compatible Serial Interface**
- **4-Wire Mode, 1.8V to 5.25V Operation**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in a Green TQFP-10×10-64L (Exposed Pad) Package**

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM90516	TQFP-10×10-64L (Exposed Pad)	-40℃ to +125℃	SGM90516XTFF64G/TR	05Q XTFF64 XXXXX	Tape and Reel, 1000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltage Range
- AVDD to GND ..... -0.3V to 6V
- DVDD to GND ..... -0.3V to 6V
- IOVDD to GND ..... -0.3V to 6V
- AVCC to GND ..... -0.3V to 18V
- AVEE to GND ..... -13V to 0.3V
- AVSSB, AVSSC, AVSSD to AVEE ..... -0.3V to 13V
- AVCC to AVSSB, AVSSC, or AVSSD ..... -0.3V to 26V
- AVCC to AVEE ..... -0.3V to 26V
- DGND to AGND ..... -0.3V to 0.3V

ADC_[0-15] Analog Input Voltage to GND ..... -13V to 13V

LV_ADC[16-20] Analog Input Voltage to GND ..... -0.3V to V_{AVDD} + 0.3V

DAC_A[0-3] Outputs to GND ..... V_{AVEE} - 0.3V to V_{AVCC} + 0.3V

DAC_B[4-7] Outputs to GND ..... V_{AVSSB} - 0.3V to V_{AVCC} + 0.3V

DAC_C[8-11] Outputs to GND ..... V_{AVSSC} - 0.3V to V_{AVCC} + 0.3V

DAC_D[12-15] Outputs to GND ..... V_{AVSSD} - 0.3V to V_{AVCC} + 0.3V

REF_CMP to GND ..... -0.3V to V_{AVDD} + 0.3V

CS, SCLK, SDI and RESET to GND ..... -0.3V to V_{IOVDD} + 0.3V

SDO to GND ..... -0.3V to V_{IOVDD} + 0.3V

GPIO[0-7] to GND ..... -0.3V to V_{IOVDD} + 0.3V

ADC_[0:15] Analog Input Current ..... -10mA to 10mA

LV_ADC[16:20] Analog Input Current ..... -10mA to 10mA

GPIO[0:7] Sinking Current 5mA

Junction Temperature ..... +150℃

Storage Temperature Range ..... -65℃ to +150℃

Lead Temperature (Soldering, 10s) ..... +260℃

RECOMMENDED OPERATING CONDITIONS

V_{AVDD} ..... 4.7V to 5.5V

V_{DVDD} (1) ..... 4.7V to 5.5V

V_{IOVDD} (2) ..... 1.8V to 5.5V

V_{AVCC} ..... 4.7V to 12.5V

V_{AVEE} ..... -12.5V to 0V

V_{AVSSB}, V_{AVSSC}, V_{AVSSD} ..... V_{AVEE} to 0V

Specified Operating Temperature Range ..... -40℃ to +105℃

Operating Temperature Range ..... -40℃ to +125℃

NOTES:

1. The value of the DVDD pin must be equal to that of the AVDD pin.
2. The value of the IOVDD pin must be less than or equal to that of the DVDD pin.

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

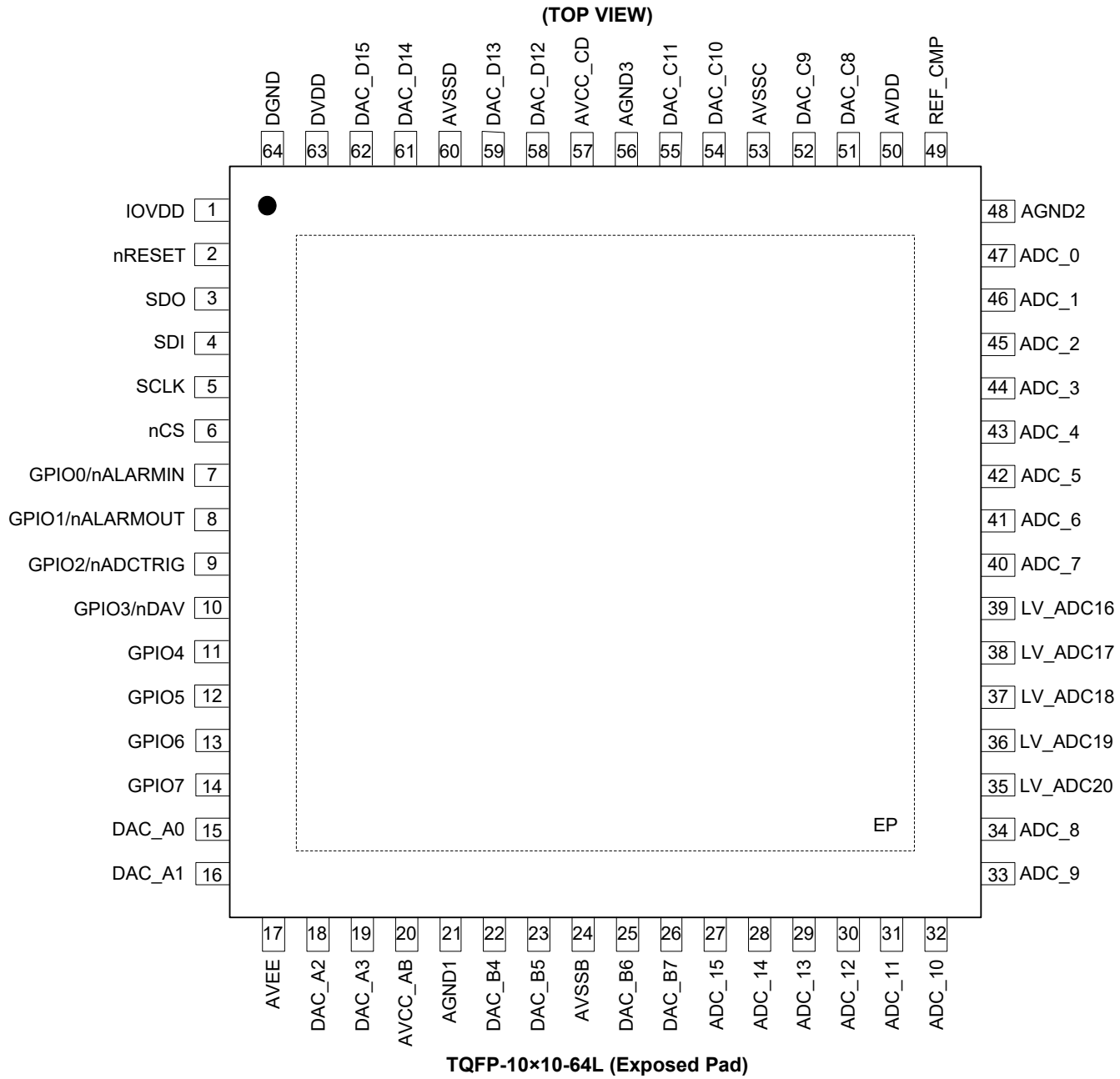
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



TQFP-10×10-64L (Exposed Pad)

PIN DESCRIPTION

PIN	NAME	I/O	FUNCTION
1	IOVDD	I	Digital Interface Input/Output Power Supply. It can be operated from 1.8V to 5.25V. The voltage on this pin must not be greater than the value of the DVDD pin.
2	nRESET	I	It's a hardware reset input pin. It's active low.
3	SDO	O	Serial Data Output pin. When CS pin is pulled high, SDO is in high impedance. When CS pin is low, the data is shifted out by this pin at each falling edge of the SCLK.
4	SDI	I	Serial Data Input pin. Data is shifted in at each rising edged of the SCLK.
5	SCLK	I	Serial Interface Clock.
6	nCS	I	It's chip select pin. This pin also works as the data frame synchronization signal. When it's pulled low, it enables the serial interface operation.
7	GPIO0/nALARMIN	I/O	General Purpose Digital Input/Output Pin0 (default). It's a bidirectional pin which has an internal 48kΩ resistor pulled up to IOVDD. This pin can be alternatively configured as nALARMIN input pin, which is an active low input signal. If it's not used, this pin can be floated.
8	GPIO1/nALARMOUT	I/O	General Purpose Digital Input/Output Pin1 (default). It's a bidirectional pin which has an internal 48kΩ resistor pulled up to IOVDD. This pin can be alternatively configured as nALARMOUT output pin, which is an open drain output. If there is an alarm event is generated, it outputs active low. If it's not used, this pin can be floated.
9	GPIO2/nADCTRIG	I/O	General Purpose Digital Input/Output Pin2 (default). It's a bidirectional pin which has an internal 48kΩ resistor pulled up to IOVDD. This pin can be alternatively configured as nADCTRIG input pin, which is an active low input signal. The falling edge of this pin begins the sampling and conversion of the ADC. If it's not used, this pin can be floated.
10	GPIO3/nDAV	I/O	General Purpose Digital Input/Output Pin3 (default). It's a bidirectional pin which has an internal 48kΩ resistor pulled up to IOVDD. This pin can be alternatively configured as nDAV output pin, which is an active low signal indicated data available. When in direct mode, the nDAV goes low if the conversion ends. When in auto mode, a 1us pulse will appear on this pin if a conversion cycle finished. When it is in deactivated, nDAV pin remains high. If it's not used, this pin can be floated.
11	GPIO4	I/O	General Purpose Digital Input/Output. These pins are bidirectional pins which have an internal 48kΩ resistor pulled up to IOVDD. If they are not used, these pins can be floated.
12	GPIO5	I/O	
13	GPIO6	I/O	
14	GPIO7	I/O	
15	DAC_A0	O	DAC Group A. These DAC channels share the same range and clamp voltage. If any of the other DAC groups is in a negative voltage range, DAC group A should be in a negative voltage range as well.
16	DAC_A1	O	
17	AVEE	I	Lowest Potential in the System. This pin is typically tied to a negative supply voltage but if all DACs are set in a positive output range, this pin can be connected to the analog ground. This pin also acts as the negative power supply for DAC group A. This pin sets the power-on-reset and clamp voltage values for the DAC group A.
18	DAC_A2	O	DAC Group A. These DAC channels share the same range and clamp voltage. If any of the other DAC groups is in a negative voltage range, DAC group A should be in a negative voltage range as well.
19	DAC_A3	O	
20	AVCC_AB	I	Positive Analog Power for DAC Groups A and B. The AVCC_AB and AVCC_CD pins must be connected to the same potential (AVCC).

PIN DESCRIPTION (continued)

PIN	NAME	I/O	FUNCTION
21	AGND1	I	Analog Ground. The pin is the ground reference point for all analog circuitry on the device. Connect the AGND1, AGND2, and AGND3 pins to the same potential (AGND). Ideally, the analog and digital grounds should be at the same potential (GND) and must not differ by more than ±0.3V.
22	DAC_B4	O	DAC Group B. These DAC channels share the same range and clamp voltage.
23	DAC_B5	O	
24	AVSSB	I	Negative Analog Supply for DAC Group B. This pin sets the power-on-reset and clamp voltage values for the DAC group B. This pin is typically tied to the AVEE pin for the negative output ranges or AGND for the positive output ranges.
25	DAC_B6	O	DAC Group B. These DAC channels share the same range and clamp voltage.
26	DAC_B7	O	
27	ADC_15	I	Bipolar Analog Inputs. These pins are typically used to monitor the DAC group-A outputs. The input range of these channels is -12.5V to 12.5V.
28	ADC_14	I	
29	ADC_13	I	
30	ADC_12	I	
31	ADC_11	I	Bipolar Analog Inputs. These pins are typically used to monitor the DAC group B outputs. The input range of these channels is -12.5V to 12.5V.
32	ADC_10	I	
33	ADC_9	I	
34	ADC_8	I	
35	LV_ADC20	I	General Purpose Analog Inputs. These channels are used for general monitoring. The input range of these pins is 0 to 2 × V_{REF}.
36	LV_ADC19	I	
37	LV_ADC18	I	
38	LV_ADC17	I	
39	LV_ADC16	I	
40	ADC_7	I	Bipolar Analog Inputs. These pins are typically used to monitor the DAC group D outputs. The input range of these channels is -12.5V to 12.5V.
41	ADC_6	I	
42	ADC_5	I	
43	ADC_4	I	
44	ADC_3	I	Bipolar Analog Inputs. These pins are typically used to monitor the DAC group C outputs. The input range of these channels is -12.5V to 12.5V.
45	ADC_2	I	
46	ADC_1	I	
47	ADC_0	I	

PIN DESCRIPTION (continued)

PIN	NAME	I/O	FUNCTION
48	AGND2	I	Analog Ground. The pin is the ground reference point for all analog circuitry on the device. Connect the AGND1, AGND2, and AGND3 pins to the same potential (AGND). Ideally, the analog and digital grounds should be at the same potential (GND) and must not differ by more than ±0.3V.
49	REF_CMP	O	Internal Reference Compensation Capacitor Connection. Connect a 4.7μF capacitor between this pin and the AGND2 pin.
50	AVDD	I	Analog Supply Voltage (4.7V to 5.5V). This pin must have the same value as the DVDD pin.
51	DAC_C8	O	DAC Group C. These DAC channels share the same range and clamp voltage.
52	DAC_C9	O	
53	AVSSC	I	Negative Analog Supply for DAC Group C. This pin sets the power on reset and clamp voltage values for the DAC group C. This pin is typically tied to the AVEE pin for the negative output ranges or AGND for the positive output ranges.
54	DAC_C10	O	DAC Group C. These DAC channels share the same range and clamp voltage.
55	DAC_C11	O	
56	AGND3	I	Analog Ground. The pin is the ground reference point for all analog circuitry on the device. Connect the AGND1, AGND2, and AGND3 pins to the same potential (AGND). Ideally, the analog and digital grounds should be at the same potential (GND) and must not differ by more than ±0.3V.
57	AVCC_CD	I	Positive analog power for DAC groups C and D. The AVCC_AB and AVCC_CD pins must be connected to the same potential (AVCC).
58	DAC_D12	O	DAC Group D. These DAC channels share the same range and clamp voltage.
59	DAC_D13	O	
60	AVSSD	I	Negative Analog Supply for DAC Group D. This pin sets the power on reset and clamp voltage values for the DAC group D. This pin is typically tied to the AVEE pin for the negative output ranges or AGND for the positive output ranges.
61	DAC_D14	O	DAC Group D. These DAC channels share the same range and clamp voltage.
62	DAC_D15	O	
63	DVDD	I	Digital Supply Voltage (4.7V to 5.5V). This pin must have the same value as the AVDD pin.
64	DGND	I	Digital Ground. This pin is the ground reference point for all digital circuitry on the device. Ideally, the analog and digital grounds should be at the same potential (GND) and must not differ by more than ±0.3V.
Thermal Pad	EP	I	The thermal pad is located on the bottom side of the device package. The thermal pad should be tied to the same potential as the AVEE pin or left disconnected.

ELECTRICAL CHARACTERISTICS

DAC

(The electrical ratings specified in this section apply to all specifications in this document, unless otherwise noted. These specifications are interpreted as conditions that do not degrade the device parametric or functional specifications for the life of the product containing it. V_{AVDD} = V_{DVDD} = 4.7V to 5.5V, V_{AVCC} = 12V, V_{IOVDD} = 1.8V to 5.25V, AGND = DGND = 0V, V_{AVEE} = V_{AVSSB} = V_{AVSSC} = V_{AVSSD} = -12V (for DAC groups in negative range) or 0 V (for DAC groups in positive ranges), DAC output range = 0V to 10V for all groups, no load on the DACs, T_A = -40℃ to +105℃)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DAC DC Accuracy						
Resolution			12			Bits
Relative Accuracy (INL)	Measured by line passing through codes 020h and FFFh. 0V to 10V and -10V to 0V ranges			±0.3		LSB
	Measured by line passing through codes 040h and FFFh. 0V to 5V and -5V to 0V ranges			±0.5		
Differential Nonlinearity (DNL)	Specified monotonic. Measured by line passing through codes 020h and FFFh. 0V to 10V and -10V to 0V ranges			±0.03		LSB
	Specified monotonic. Measured by line passing through codes 020h and FFFh. 0V to 5V and -5V to 0V ranges			±0.06		
Total Unadjusted Error (1) (TUE)	T_A = +25℃	0V to 10V range		±2.5		mV
		-10V to 0V range		±2.5		
		0V to 5V range		±1.5		
		-5V to 0V range		±1.5		
Offset Error		Measured by line passing through codes 020h and FFFh. 0V to 10V range		±0.25		mV
		Measured by line passing through codes 040h and FFFh. 0V to 5V range		±0.25		
Zero-Code Error	T_A = +25℃	Code 000h, -10V to 0V range		±1		mV
		Code 000h, -5V to 0V range		±1		
Gain Error (1)		Measured by line passing through codes 020h and FFFh, 0V to 10V range		±0.01		%FSR
		Measured by line passing through codes 020h and FFFh, -10V to 0V range		±0.01		
		Measured by line passing through codes 040h and FFFh, 0V to 5V range		±0.01		
		Measured by line passing through codes 040h and FFFh, -5V to 0V range		±0.01		
Offset Temperature Coefficient	0V to 10V range			±1		ppm/℃
	0V to 5V range			±1		
Zero-Code Temperature Coefficient	-10V to 0V range			±2		ppm/℃
	-5V to 0V range			±2		
Gain Temperature Coefficient (1)	0V to 10V range			±2.5		ppm/℃
	-10V to 0V range			±2.5		
	0V to 5V range			±2.5		
	-5V to 0V range			±2.5		

NOTE:

1. The internal reference contribution not included.

ELECTRICAL CHARACTERISTICS (continued)

DAC (continued)

(The electrical ratings specified in this section apply to all specifications in this document, unless otherwise noted. These specifications are interpreted as conditions that do not degrade the device parametric or functional specifications for the life of the product containing it. V_{AVDD} = V_{DVDD} = 4.7V to 5.5V, V_{AVCC} = 12V, V_{IOVDD} = 1.8V to 5.25V, AGND = DGND = 0V, V_{AVEE} = V_{AVSSB} = V_{AVSSC} = V_{AVSSD} = -12V (for DAC groups in negative range) or 0 V (for DAC groups in positive ranges), DAC output range = 0V to 10V for all groups, no load on the DACs, T_A = -40℃ to +105℃)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DAC Output Characteristics					
Full-Scale Output Voltage Range (2)	Set at power-up or reset through auto-range detection. The output range can be modified after power-up or reset through the DAC range registers (Address 0x1E through 0x1F). DAC-RANGE = 100b	-10		0	V
	The output range can be modified after power-up or reset through the DAC range registers (Address 0x1E through 0x1F). DAC-RANGE = 101b	-5		0	
	Set at power-up or reset through auto-range detection. The output range can be modified after power-up or reset through the DAC range registers (Address 0x1E through 0x1F). DAC-RANGE = 111b	0		5	
	The output range can be modified after power-up or reset through the DAC range registers (Address 0x1E through 0x1F). DAC-RANGE = 110b	0		10	
Output Voltage Settling Time	Transition: Code 400h to C00h to within ½ LSB, R_L = 2kΩ, C_L = 200pF. 0V to 10V and -10V to 0 V ranges		10		μs
	Transition: Code 400h to C00h to within ½ LSB, R_L = 2kΩ, C_L = 200pF. 0V to 5V and -5V to 0V ranges		10		
Slew Rate	Transition: Code 400h to C00h, 10% to 90%, R_L = 2kΩ, C_L = 200pF. 0V to 10V and -10V to 0V ranges		1.25		V/μs
	Transition: Code 400h to C00h, 10% to 90%, R C_L = 200pF. 0V to 5V and -5V to 0V ranges		1.25		
Short Circuit Current	Full-scale current shorted to the DAC group AVSS or AVCC voltage		±45		mA
Load Current (3)	Source or sink with 1V headroom from the DAC group AVCC or AVSS voltage, voltage drop < 25mV	±15			mA
	Source or sink with 300mV headroom from the DAC group AVCC or AVSS voltage, voltage drop < 25mV	±10			
Maximum Capacitive Load (4)	R_L = ∞, the capability of load of cap directly.	0		10	nF
DC Output Impedance	Code set to 800h, ±15mA		1		Ω
Power-On Overshoot	V_{AVEE} = V_{AVSSB} = V_{AVSSC} = V_{AVSSD} = AGND, V_{AVCC} = 0V to 12V, 2ms ramp		10		mV
Glitch Energy	Transition: Code 7FFh to 800h; 800h to 7FFh		1		nV-s
Output Noise	T_A = +25℃, 1kHz, code 800h, includes internal reference noise		520		$nV/\sqrt{Hz}$
	T_A = +25℃, integrated noise from 0.1Hz to 10Hz, code 800h, includes internal reference noise		20		μV_{PP}
Clamp Outputs					
Clamp Output Voltage (5)	DAC output range: 0V to 10V, V_{AVSS} = AGND		0		V
	DAC output range: 0V to 5V, V_{AVSS} = AGND		0		
	DAC output range: -10V to 0V, V_{AVSS} = -12V		V_{AVSS} + 2		
	DAC output range: -5V to 0V, V_{AVSS} = -6V		V_{AVSS} + 1		
Clamp Output Impedance			200		Ω

NOTES:

2. The output voltage of each DAC group must not be greater than that of the corresponding AVCC pin (AVCC_AB or AVCC_CD) or lower than that of the corresponding AVSS pin (AVEE, AVSSB, AVSSC or AVSSD). See the DAC Output Range and Clamp Configuration section for more details.
3. If all channels are simultaneously loaded, care must be taken to ensure the thermal conditions for the device are not exceeded.
4. To be sampled during initial release to ensure compliance; not subject to production testing.
5. No DAC load to the DAC group AVSS pin.

ELECTRICAL CHARACTERISTICS (continued)

ADC and Temperature Sensor

(The electrical ratings specified in this section apply to all specifications in this document, unless otherwise noted. These specifications are interpreted as conditions that do not degrade the device parametric or functional specifications for the life of the product containing it. V_{AVDD} = V_{DVDD} = 4.7V to 5.5V, V_{AVCC} = 12V, V_{IOVDD} = 1.8V to 5.25V, AGND = DGND = 0V, V_{AVEE} = V_{AVSSB} = V_{AVSSC} = V_{AVSSD} = -12V (for DAC groups in negative range) or 0 V (for DAC groups in positive ranges), DAC output range = 0V to 10V for all groups, no load on the DACs, T_A = -40℃ to +105℃)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution		12			Bits
Integral Nonlinearity	Unipolar input channels		±0.5		LSB
	Bipolar input channels		±0.5		
Differential Nonlinearity	Specified monotonic. All input channels		±0.5		LSB
Unipolar Analog Inputs: LV_ADC16 to LV_ADC20					
Absolute Input Voltage Range		AGND - 0.2		V_{AVDD} + 0.2	V
Full Scale Input Range	V_{REF} measured at REF_CMP pin	0		2 × V_{REF}	V
Input Capacitance			34		pF
DC Input Leakage Current	Unselected ADC input			±10	μA
Offset Error			±1		LSB
Offset Error Match			±0.5		LSB
Gain Error (1)			±0.5		LSB
Gain Error Match			±1		LSB
Update Time	Single unipolar input, temperature sensor disabled		11.5		μs
Bipolar Analog Inputs: ADC_0 to ADC_15					
Absolute Input Voltage Range		-13		13	V
Full Scale Input Range		-12.5		12.5	V
Input Resistance			175		kΩ
Offset Error			±0.25		LSB
Gain Error (1)			±0.5		LSB
Update Time	Single bipolar input, temperature sensor disabled		25		μs
Temperature Sensor					
Operating Range		-40		125	℃
Accuracy	T_A = -40℃ to +125℃, AVDD = 5V		±1.25		℃
Resolution	LSB size		0.25		℃
Update Time	All ADC input channels disabled		256		μs
ADC Update Time					
Internal Oscillator Frequency			4		MHz
ADC Update Time	All 21 ADC inputs enabled, temperature sensor disabled.		609.5		μs
	All 21 ADC inputs enabled, temperature sensor enabled.		865.5		μs
Internal Reference (Internal Reference Not Accessible)					
Initial Accuracy	T_A = +25℃		2.5		V
Reference Temperature Coefficient			12		ppm/℃

NOTE:

1. The internal reference contribution not included.

ELECTRICAL CHARACTERISTICS (continued)

General

(The electrical ratings specified in this section apply to all specifications in this document, unless otherwise noted. These specifications are interpreted as conditions that do not degrade the device parametric or functional specifications for the life of the product containing it. V_{AVDD} = V_{DVDD} = 4.7V to 5.5V, V_{AVCC} = 12V, V_{IOVDD} = 1.8V to 5.25V, AGND = DGND = 0V, V_{AVEE} = V_{AVSSB} = V_{AVSSC} = V_{AVSSD} = -12V (for DAC groups in negative range) or 0 V (for DAC groups in positive ranges), DAC output range = 0V to 10V for all groups, no load on the DACs, T_A = -40℃ to +105℃)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
AVSS Detector					
AVSS Threshold Detector (AV_{SSTH})		-3.5		-1.5	V
Digital Logic: GPIO					
High-Level Input Voltage	V_{IOVDD} = 1.8V to 5.5V	0.7 × V_{IOVDD}			V
Low-Level Input Voltage	V_{IOVDD} = 1.8V			0.45	V
	V_{IOVDD} = 2.7V to 5.5V			0.3 ×V_{IOVDD}	
Low-Level Output Voltage	V_{IOVDD} = 1.8V, I_{LOAD} = -2mA			0.4	V
	V_{IOVDD} = 5.5V, I_{LOAD} = -5mA			0.4	
Input Impedance	To IOVDD		48		kΩ
Digital Logic: All Except GPIO					
High-Level Input Voltage	V_{IOVDD} = 1.8V to 5.5V	0.7 ×V_{IOVDD}			V
Low-Level Input Voltage	V_{IOVDD} = 1.8V			0.45	V
	V_{IOVDD} = 2.7V to 5.5V			0.3 ×V_{IOVDD}	V
High-Level Output Voltage	I_{LOAD} = -1mA	V_{IOVDD} - 0.4			V
Low-Level Output Voltage	I_{LOAD} = 1mA			0.4	V
High Impedance Leakage				±5	μA
High Impedance Output Capacitance			10		pF
Power Requirements					
AVDD Supply Current (I_{AVDD})	No DAC load, all DACs at 800h code and ADC at the fastest auto conversion rate		6		mA
AVCC Supply Current (I_{AVCC})			7.5		
AVSS Supply Current (I_{AVSS})			-5		
AVEE Supply Current (I_{AVEE})			-1.75		
DVDD Supply Current (I_{DVDD})			1		
IOVDD Supply Current (I_{IODD})			1.5		μA
Power Consumption			215		mW
AVDD Supply Current (I_{AVDD})	Power-down mode		2.5		mA
AVCC Supply Current (I_{AVCC})			1		
AVSS Supply Current (I_{AVSS})			-3		
AVEE Supply Current (I_{AVEE})			-1.75		
DVDD Supply Current (I_{DVDD})			0.75		
IOVDD Supply Current (I_{IODD})			1.5		μA
Power Consumption			90		mW

TIMING REQUIREMENTS

(V_{AVDD} = V_{DVDD} = 4.7V to 5.5V, V_{AVCC} = 12V, V_{AVEE} = -12V, AGND = DGND = V_{AVSSB} = V_{AVSSC} = V_{AVSSD} = 0V, DAC output range = 0V to 10V for all groups, no load on the DACs, T_A = -40℃ to +105℃, unless otherwise noted)

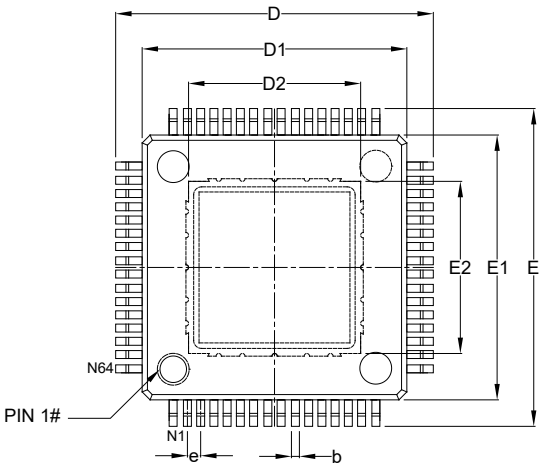
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Interface (1)					
SCLK Frequency (f_{SCLK})	V_{IOVDD} = 1.8V to 2.7V			15	MHz
	V_{IOVDD} = 2.7 to 5.25V			20	
SCLK Period (t_P)	V_{IOVDD} = 1.8V to 2.7V	66.67			ns
	V_{IOVDD} = 2.7 to 5.25V	50			
SCLK Pulse Width High (t_{PH})	V_{IOVDD} = 1.8V to 2.7V	30			ns
	V_{IOVDD} = 2.7 to 5.25V	23			
SCLK Pulse Width Low (t_{PL})	V_{IOVDD} = 1.8V to 2.7V	30			ns
	V_{IOVDD} = 2.7 to 5.25V	23			
SDI Setup (t_{SU})	V_{IOVDD} = 1.8V to 2.7V	10			ns
	V_{IOVDD} = 2.7 to 5.25V	10			
SDI Hold (t_H)	V_{IOVDD} = 1.8V to 2.7V	10			ns
	V_{IOVDD} = 2.7 to 5.25V	10			
SDO Driven To Tri- State (2) (t_{ODZ})	V_{IOVDD} = 1.8V to 2.7V	0		15	ns
	V_{IOVDD} = 2.7 to 5.25V	0		9	
SDO Tri-State To Driven (2) (t_{OZD})	V_{IOVDD} = 1.8V to 2.7V	0		23	ns
	V_{IOVDD} = 2.7 to 5.25V	0		15	
SDO Output Delay (2) (t_{OD})	V_{IOVDD} = 1.8V to 2.7V	0		23	ns
	V_{IOVDD} = 2.7 to 5.25V	0		15	
nCS Setup (t_{SU_nCS})	V_{IOVDD} = 1.8V to 2.7V	5			ns
	V_{IOVDD} = 2.7 to 5.25V	5			
nCS Hold (t_{H_nCS})	V_{IOVDD} = 1.8V to 2.7V	20			ns
	V_{IOVDD} = 2.7 to 5.25V	20			
Inter-Access Gap (t_{IAG})	V_{IOVDD} = 1.8V to 2.7V	10			ns
	V_{IOVDD} = 2.7 to 5.25V	10			
Digital Logic					
Reset Delay; Delay-to-Normal Operation from Reset			100		μs
Power-Down Recovery Time				70	μs
Clamp Shutdown Delay			100		μs
Convert Pulse Width		20			ns
Reset Pulse Width		20			ns
ADC WAIT State (3); the Wait Time from When the ADC Enters the IDLE State		2			μs

NOTES:

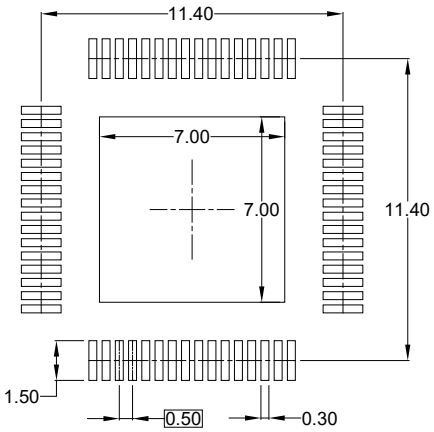
1. Specified by design and characterization. Not tested during production.
2. SDO loaded with 10 pF load capacitance for SDO timing specifications.
3. Specified by design; not subject to production testing. See the ADC Sequencing section for more details.

PACKAGE OUTLINE DIMENSIONS

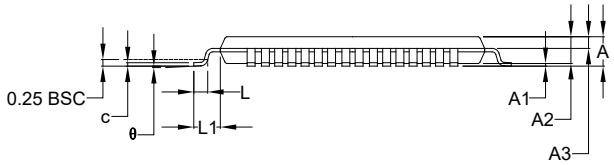
TQFP-10×10-64L (Exposed Pad)



TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	-	-	1.200
A1	0.050	-	0.150
A2	0.950	1.000	1.050
A3	0.390	0.440	0.490
b	0.170	-	0.270
c	0.090	0.130	0.180
D	11.800	12.000	12.200
D1	9.900	10.000	10.100
D2	5.900	-	6.800
E	11.800	12.000	12.200
E1	9.900	10.000	10.100
E2	5.900	-	6.800
e	0.400	0.500	0.600
L	0.450	-	0.750
L1	1.000 REF		
θ	0°	3.5°	7°

NOTES:

1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.