3. 8V-32V Vin, 2A Synchronous Step-down DCDC Converter with EMI Reduction

FEATURES

- Qualified for automotive application
- EMI Reduction with Switching Node Ringing-free
- Pulse Skipping Mode PSM with 22uA Quiescent Current in Light Load Condition
- 3.8V-32V Wide Input Voltage Range
- Up to 2A Continuous Output Load Current
- 0.8V ±1% Feedback Reference Voltage
- Fully Integrated 140mΩ R_{dson} High Side MOSFET and 70mΩ R_{dson} Low Side MOSFET
- 1uA Shut-down Current
- 80ns Minimum On-time
- Precision Enable Threshold for Programmable UVLO Threshold and Hysteresis
- 4ms Built-in Soft Start Time
- Output Over Voltage Protection
- Thermal Shutdown Protection at 160°C
- Available in QFN2X3-9L Package

APPLICATIONS

- Automotive
- White Goods, Home Appliance
- Surveillance, network systems
- Audio, WiFi Speaker
- Printer, Charging Station
- DTV, STB, Monitor/LCD Display

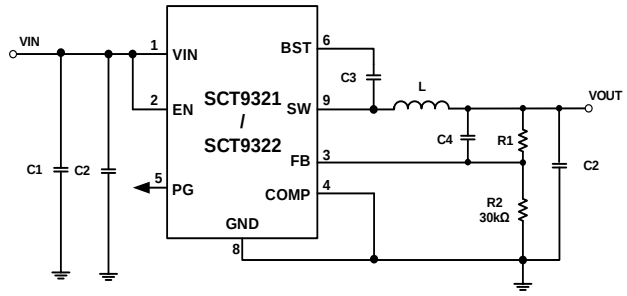
DESCRIPTION

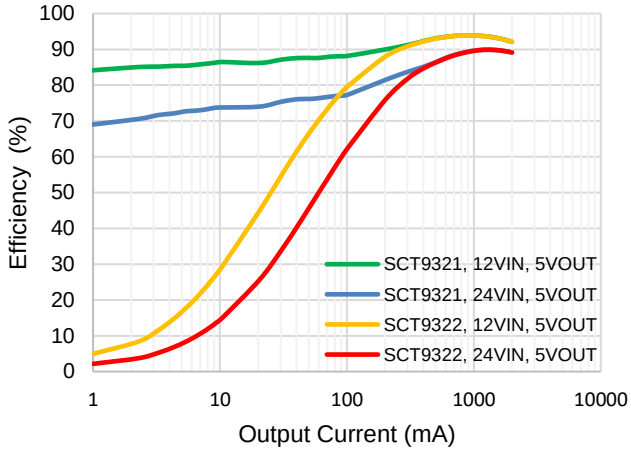
The SCT9321/SCT9322 is 2A synchronous buck converters with up to 32V wide input voltage range, which fully integrates an 140mΩ high-side MOSFET and a 70mΩ low-side MOSFET to provide high efficiency step-down DCDC conversion. The SCT9321/SCT9322 adopts peak current mode control. The SCT9321/SCT9322 supports the Pulse Skipping Modulation (PSM) with typical 22uA Ultra-Low Quiescent.

The SCT9321/SCT9322 is an Electromagnetic Interference (EMI) friendly buck converter with implementing optimized design for EMI reduction. The converter has proprietary designed gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off time, which further erases high frequency radiation EMI noise caused by the MOSFETs hard switching.

The SCT9321/SCT9322 offers output over-voltage protection, cycle-by-cycle peak current limit, and thermal shutdown protection. The device is available in a low-profile 3x2mm QFN2X3-9L package.

TYPICAL APPLICATION





Efficiency, fsw=500kHz

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Release to market

DEVICE ORDER INFORMATION

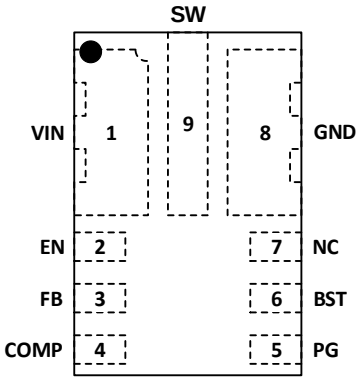
PART NUMBER	PACKAGE MARKING	PACKAGE DISCRIPTION
SCT9321/SCT9322FSA	9321/9322	QFN2X3-9L
1) For Tape & Reel, Add Suffix R (e.g. SCT9321/SCT9322FSAR)		

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
BST	-0.3	40	V
VIN, SW, EN	-0.3	34	V
VIN	-0.3	40 (400ms)	V
VS, FB, COMP	-0.3	5.5	V
Operating junction temperature(2)	-40	125	C
Storage temperature T_{STG}	-65	150	C

PIN CONFIGURATION



Top View: QFN-9, Plastic

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.
(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

PIN FUNCTIONS

NAME	NO.	PIN FUNCTION
VIN	1	Power supply input. Must be locally bypassed.
EN	2	Enable logic input. Floating the pin enables the device. This pin supports high voltage input up to VIN supply to be connected VIN directly to enable the device automatically. The device has precision enable thresholds 1.18V rising / 1.1V falling for programmable UVLO threshold and hysteresis.
FB	3	Buck converter output feedback sensing voltage. Connect a resistor divider from VOUT to FB to set up output voltage. The device regulates FB to the internal reference of 0.8V typical.
COMP	4	Compensation pin. Connect this pin to GND for internal compensation. Add an RC network to adjust the loop response externally. See Loop Response Design for more details.

PG	5	Open drain power-good output that is pulled to GND when the output voltage is out of its regulation limits or during soft-start. There is an internal 5MΩ pull-up resistor.
BST	6	Power supply for the high-side power MOSFET gate driver. Must connect a 0.1uF or greater ceramic capacitor between BST pin and SW node.
NC	7	NC
GND	8	Power ground. Must be soldered directly to ground plane.
SW	9	Switching node of the buck converter.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	3.8	32	V
T_J	Operating junction temperature	-40	125	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-2	+2	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014specification, all pins(1)	-0.5	+0.5	kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	QFN-9	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	70	°C/W
$R_{\theta JC}$	Junction to case thermal resistance(1)	15	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT9321/SCT9322 is mounted. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT9321/SCT9322. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

ELECTRICAL CHARACTERISTICS

V_{IN}=12V, T_J=-40°C~125°C, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		3.8		32	V
V_{IN_UVLO}	Input UVLO	V_{IN} rising	3.3	3.5	3.7	V
	Hysteresis			440		mV
I_{SD}	Shutdown current	EN=0, No load, VIN=12V		1	3	uA

SYMBOL	PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
I_Q	Quiescent current	SCT9321	EN=floating, No load, No switching. VIN=12V. BST-SW=5V		22		uA
		SCT9322	EN=floating, No load, No switching. VIN=12V. BST-SW=5V, COMP floating		206		uA
Enable, Soft Start and Working Modes							
V_{EN_H}	Enable high threshold			1.15	1.18	1.22	V
V_{EN_L}	Enable low threshold			1.05	1.1	1.15	V
I_{EN}	Enable pin input current		EN=1V	1	1.5	2	uA
I_{EN_HYS}	Enable pin hysteresis current		EN=1.5V		4		uA
Power MOSFETs							
R_{DSON_H}	High side FET on-resistance				140		mΩ
R_{DSON_L}	Low side FET on-resistance				70		mΩ
Feedback and Error Amplifier							
V_{FB}	Feedback Voltage			0.792	0.8	0.808	V
Current Limit							
I_{LIM_HSD}	HSD peak current limit			3.0	3.5	4.0	A
I_{LIM_LSD}	LSD valley current limit			2.5	3.0	3.5	A
Switching Frequency							
F_{SW}	Switching frequency		V_{IN}=12V, V_{OUT}=5V	300	450	500	kHz
t_{ON_MIN}	Minimum on-time				80	100	ns
Soft Start Time							
t_{SS}	Internal soft-start time				4		ms
Protection							
V_{OVP}	Output OVP threshold Hysteresis		V_{OUT} rising		110 5		% %
T_{HIC_W}	OCP hiccup wait time				512		Cycles
T_{HIC_R}	OCP hiccup restart time				8192		Cycles
T_{SD}	Thermal shutdown threshold Hysteresis		T_J rising		170 25		°C

TYPICAL CHARACTERISTICS

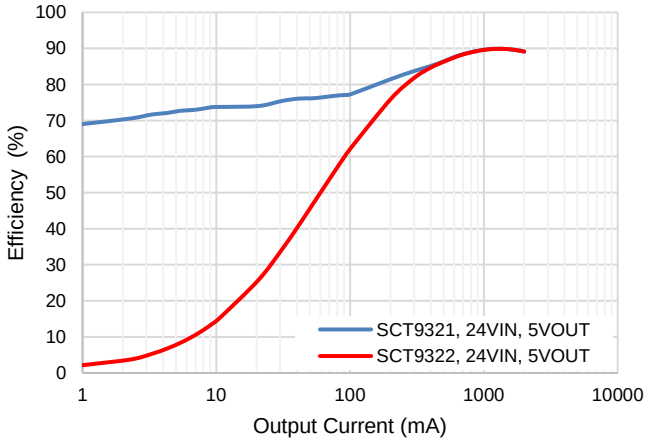


Figure 1. Efficiency vs Load Current, Vin=24V

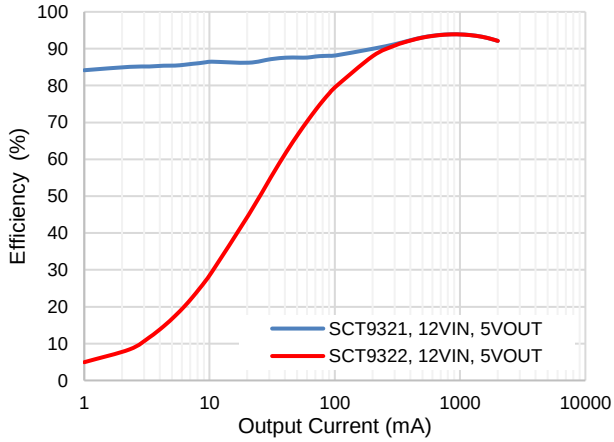


Figure 2. Efficiency vs Load Current, Vin=12V

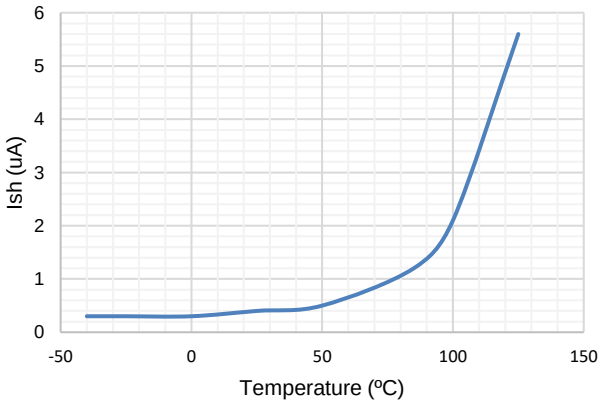


Figure 3. Shut-down Current vs Temperature

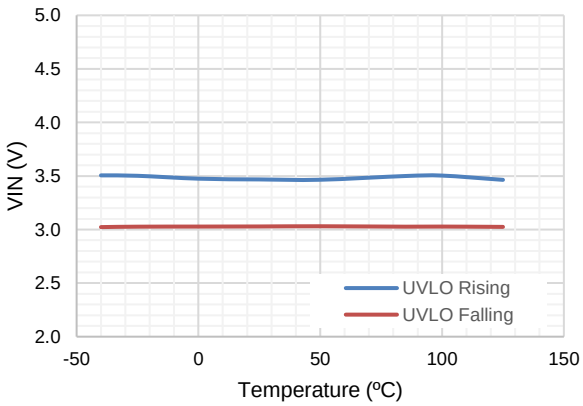


Figure 4. VIN UVLO vs Temperature

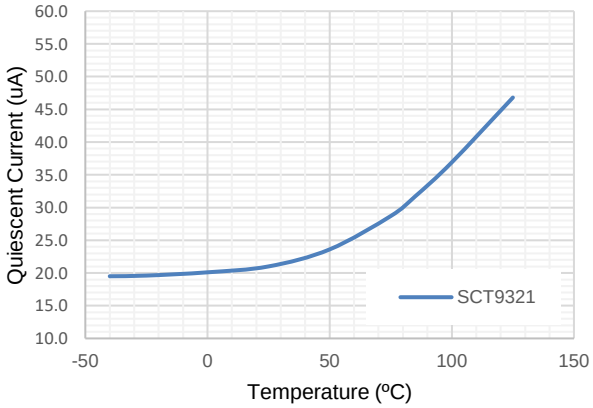


Figure 5. Quiescent Current vs Temperature

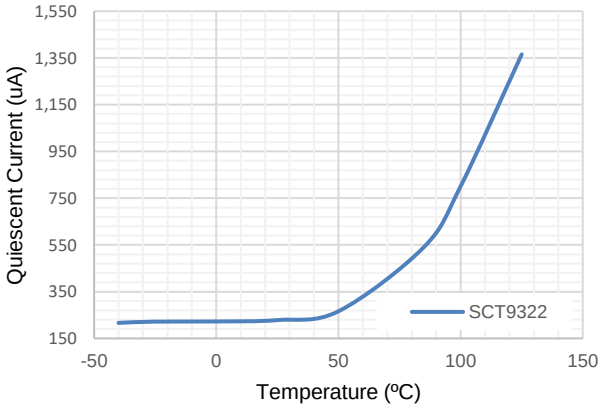


Figure 6. Quiescent Current vs Temperature

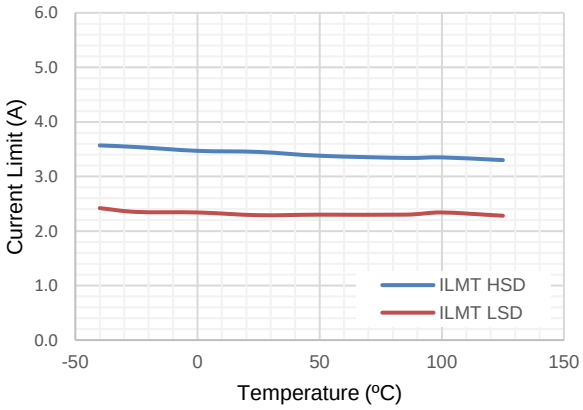


Figure 7. Peak Current Limit vs Temperature

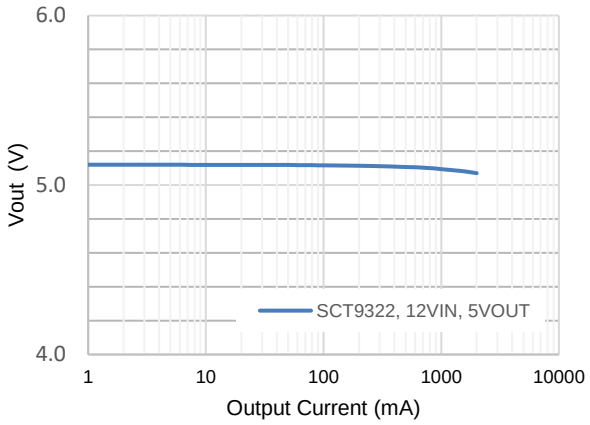


Figure 8. Load Regulation, SCT9322, Vout=5V

FUNCTIONAL BLOCK DIAGRAM

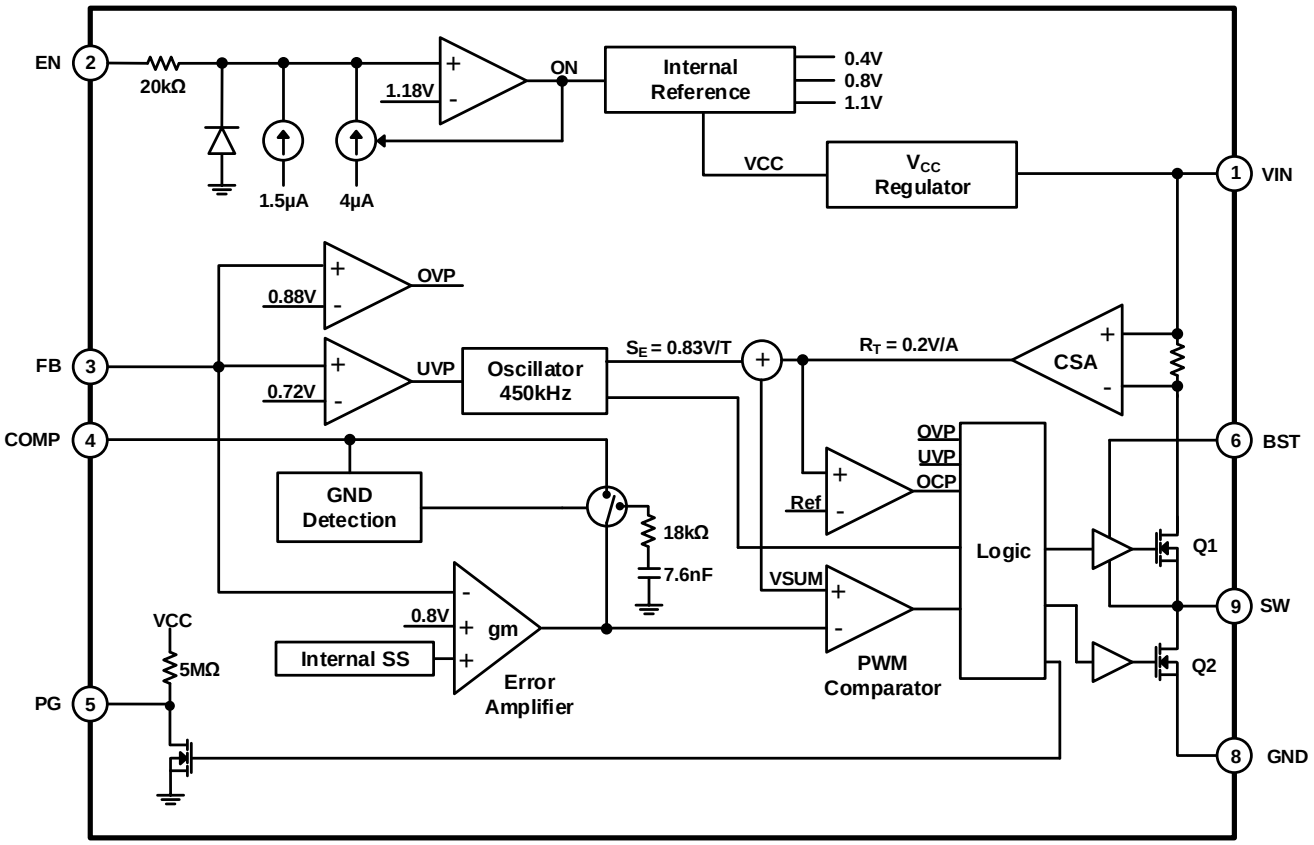


Figure 9. Functional Block Diagram

OPERATION

Overview

The SCT9321/SCT9322 device is 3.8V-32V input, 2A output, EMI friendly, fully integrated synchronous buck converters. The device employs fixed frequency peak current mode control. An internal clock with 450kHz frequency initiates turning on the integrated high-side power MOSFET Q1 in each cycle, then inductor current rises linearly and the converter charges output cap. When sensed voltage on high-side MOSFET peak current via the CSA block, rising above the voltage of internal COMP (see functional block diagram), the device turns off high-side MOSFET Q1 and turns on low-side MOSFET Q2. The inductor current decreases when MOSFET Q2 is ON. In the next rising edge of clock cycle, the low-side MOSFET Q2 turns off. This repeats on cycle-by-cycle based.

The SCT9321/9322 features peak current mode control together with built-in 4ms soft-start time. The device provides two loop compensation modes: internal loop compensation mode and external loop compensation mode, selected by different connecting-status of the COMP pin. The peak current mode control with the internal loop compensation network and the built-in 4ms soft-start simplify the SCT9321/SCT9322 footprints and minimize the off-chip component counts. The external loop compensation mode makes the device adapt wide-range application easily. The quiescent current of SCT9321 is 22uA typical under no-load condition and no switching. When disabling the device, the supply shut down current of SCT9321/SCT9322 is only 1μA. The SCT9321 works at Pulse Skipping Mode PSM to further increase the power efficiency in light load condition, hence the power efficiency can be achieved up to 88% at 5mA load condition.

The error amplifier serves the COMP node by comparing the voltage on the FB pin with an internal 0.8V reference voltage. When the load current increases, a reduction in the feedback voltage relative to the reference raises COMP voltage till the average inductor current matches the increased load current. This feedback loop well regulates the output voltage. The device also integrates an internal slope compensation circuitry to prevent sub-harmonic oscillation when duty cycle is greater than 50% for a fixed frequency peak current mode control. To provide the lower output ripple in light load condition, the SCT9322 works at the Force Pulse Width Modulation (FPWM) mode.

The hiccup mode minimizes power dissipation during prolonged output overcurrent or short conditions. The hiccup wait time is 512 cycles and the hiccup restart time is 8192 cycles. The SCT9321/SCT9322 device also features protections including cycle-by-cycle high-side MOSFET peak current limit, over-voltage protection, and over-temperature protection.

PSM Working Modes

In light load condition, the SCT9321 forces the device operating at forced Pulse Skipping Modulation (PSM) mode. When the load current decreasing, the internal COMP net voltage decreases as the inductor current down. With the load current further decreasing, the COMP net voltage decreases and be clamped at a voltage corresponding to the 600mA peak inductor current. When the load current approaches zero, the SCT9321 enter Pulse Skipping Mode (PSM) mode to increase the converter power efficiency at light load condition. When the inductor current decreases to zero, zero-cross detection circuitry on high-side MOSFET Q1 forces the Q1 off till the beginning of the next switching cycle. The buck converter does not sink current from the load when the output load is light and converter works in PSM mode.

FPWM Working Modes

To provide the lower output ripple in light load condition, the SCT9322 offers the fixed 450kHz switching frequency and works at the Force Pulse Width Modulation (FPWM) mode.

VIN Power

The SCT9321/SCT9322 is designed to operate from an input voltage supply range between 3.8V to 32V, at least 0.1uF decoupling ceramic cap is recommended to bypass the supply noise. If the input supply locates more than a few inches from the converter, an additional electrolytic or tantalum bulk capacitor or with recommended 22uF may be required in addition to the local ceramic bypass capacitors.

Under Voltage Lockout UVLO

The SCT9321/SCT9322 Under Voltage Lock Out (UVLO) default startup threshold is typical 3.5V with VIN rising and shutdown threshold is 3.1V with VIN falling. The more accurate UVLO threshold can be programmed through the precision enable threshold of EN pin.

Enable and Start up

When applying a voltage higher than the EN high threshold (typical 1.18V/rise), the SCT9321/SCT9322 enables all functions and the device starts soft-start phase. The SCT9321/SCT9322 has the built in 4ms soft-start time to prevent the output overshoot and inrush current. When EN pin is pulled low, the internal SS net will be discharged to ground. Buck operation is disabled when EN voltage falls below its lower threshold (typically 1.1V/fall).

An internal 1.5uA pull up current source connected from internal LDO power rail to EN pin guarantees that floating EN pin automatically enables the device. For the application requiring higher VIN UVLO voltage than the default setup, there is a 4uA hysteresis pull up current source on EN pin which configures the VIN UVLO voltage with an off-chip resistor divider R3 and R4, shown in Figure 10. The resistor divider R3 and R4 are calculated by equation (1) and (2).

EN pin is a high voltage pin and can be directly connected to VIN to automatically start up the device with VIN rising to its internal UVLO threshold.

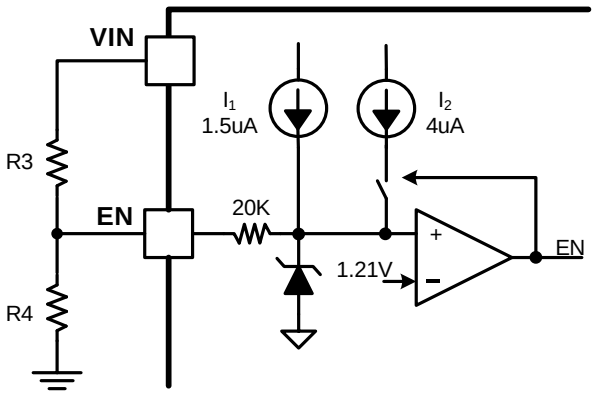


Figure 10. Adjustable VIN UVLO

$$R3 = \frac{V_{Start}\left(\frac{V_{ENF}}{V_{ENR}}\right) - V_{Stop}}{I_1\left(1 - \frac{V_{ENF}}{V_{ENR}}\right) + I_2} \quad (1)$$

$$R4 = \frac{R_3 \times V_{ENF}}{V_{Stop} - V_{ENF} + R_3(I_1 + I_2)} \quad (2)$$

Where:

Vstart: Vin rise threshold to enable the device
Vstop: Vin fall threshold to disable the device
I_1=1.5uA
I_2=4uA
V_{ENR}=1.18V

V_{EMF}=1.1V

Power-GOOD (PG) Indicator

The SCT9321/SCT9322 has an open-drain output that is actively held low during soft start period until the output voltage reaches 80% of the target output. When the output voltage is outside of its regulation by -20%, the PG will pull low until the output returns to set value. The PG low to high transition is delayed by 1.5ms while the falling edge PG is delayed by 200μs to prevent false triggering.

Peak Current Limit and Hiccup Mode

The SCT9321/9322 have cycle-by-cycle peak current limit with sensing the internal high side MOSFET Q1 current during overcurrent condition. While the Q1 turns on, its conduction current is monitored by the internal sensing circuitry. Once the high-side MOSFET Q1 current exceeds the limit, it turns off immediately. If the Q1 over current time exceeds 512 switching cycles (hiccup waiting time), the buck converter enters hiccup mode and shuts down. After 8192 cycles off, the buck converter restarts to power up. The hiccup modes reduce the power dissipation in over current condition.

Over Voltage Protection and Minimum On-time

Both SCT9321/SCT9322 features buck converter output over voltage protection (OVP). If the output feedback pin voltage exceeds 110% of feedback reference voltage (0.8V), the converter stops switching immediately. When the output feedback pin voltage drops below 105% of feedback reference voltage, the converter resumes to switching. The OVP function prevents the connected output circuitry damaged from un-predictive overvoltage. Featured feedback overvoltage protection also prevents dynamic voltage spike to damage the circuitry at load during fast loading transient.

The high-side MOSFET Q1 has minimum on-time 80ns typical limitation. While the device operates at minimum on-time, further increasing VIN results in pushing output voltage beyond regulation point. With output feedback over voltage protection, the converter skips pulse by turning off high-side MOSFET Q1 and prevents output running away higher to damage the load.

Bootstrap Voltage Regulator

An external bootstrap capacitor between BST and SW pin powers floating high-side power MOSFET gate driver. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on.

The floating supply (BST to SW) UVLO threshold is 2.7V rising and hysteresis of 350mV. When the converter operates with high duty cycle or prolongs in sleep mode for certain long time, the required time interval to recharging bootstrap capacitor is too long to keep the voltage at bootstrap capacitor sufficient. When the voltage across bootstrap capacitor drops below 2.35V, BST UVLO occurs. The SCT9321/SCT9322 intervenes to turn on low side MOSFET periodically to refresh the voltage of bootstrap capacitor to guarantee operation over a wide duty range.

Low Drop-out Regulation

To support the application of small voltage-difference between Vout and Vin, the Low Drop Out (LDO) Operation is implemented by the SCT9321/SCT9322. The Low Drop Out Operation is triggered automatic when the off time of the high-side power MOSFET exceeds the minimum off time limitation.

In low drop out operation, high-side MOSFET remains ON as long as the BST pin to SW pin voltage is higher than BST UVLO threshold. When the voltage from BST to SW drops below 2.35V, the high-side MOSFET turns off and low-side MOSFET turns on to recharge bootstrap capacitor periodically in the following several switching cycles. Only 100ns of low side MOSFET turning on in each refresh cycle minimizes the output voltage ripple. Low-side MOSFET may turn on for several times till bootstrap voltage is charged to higher than 2.7V for high-side

MOSFET working normally. Then high-side MOSFET turns on and remains on until bootstrap voltage drops to trigger bootstrap UVLO again. Thus, the effective duty cycle of the switching regulator during Low Drop-out LDO operation can be very high even approaching 100%.

During ultra-low voltage difference of input and output voltages, i.e. the input voltage ramping down to power down, the output can track input closely thanks to LDO operation mode.

EMI Reduction with Switching Node Ringing-free

In buck converter, the switching node ringing amplitude and cycles are critical especially related to the high frequency radiation EMI noise. The SCT9321/SCT9322 implements the multi-level gate driver speed technique to achieve the switching node ringing-free without scarifying the switching node rise/fall slew rate and power efficiency of the converter. The switching node ringing amplitude and cycles are damped by the built-in MOSFETs gate driving technique (SCT Patented Proprietary Design). The switching node zoomed in wave form is shown in Figure 14.

Thermal Shutdown

Once the junction temperature in the SCT9321/SCT9322 exceeds 170°C, the thermal sensing circuit stops converter switching and restarts with the junction temperature falling below 125°C. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

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APPLICATION INFORMATION

Typical Application

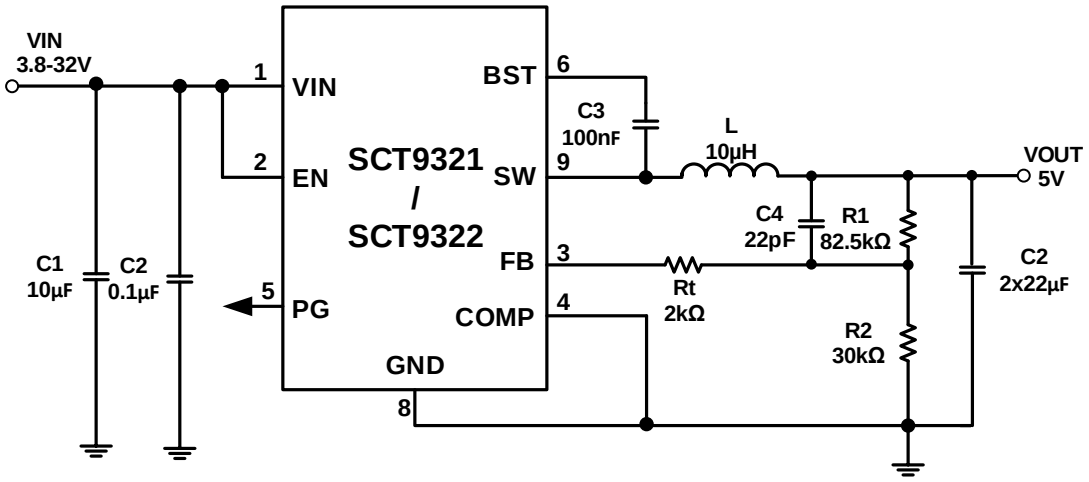


Figure 11. 24V Input, 5V/2A Output

Design Parameters

Design Parameters	Example Value
Input Voltage	12V
Output Voltage	3.3V
Output Current	2A
Output voltage ripple (peak to peak)	±0.03V
Switching Frequency	450kHz

Input Capacitor Selection

For good input voltage filtering, choose low-ESR ceramic capacitors. A ceramic capacitor 10μF is recommended for the decoupling capacitor anda0.1μF ceramic bypass capacitor is recommended to be placed as close as possible to the VIN pin of the SCT9321/SCT9322.

Use Equation (3) to calculate the input voltage ripple:

$$\Delta V_{IN} = \frac{I_{OUT}}{C_{IN} \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (3)$$

Where:

- C_{IN} is the input capacitor value
- f_{sw} is the converter switching frequency
- I_{OUT} is the maximum load current

Due to the inductor current ripple, the input voltage changes if there is parasitic inductance and resistance between the power supply and the VIN pin. It is recommended to have enough input capacitance to make the input voltage ripple less than 100mV. Generally, a 35V/10uF input ceramic capacitor is recommended for most of applications. Choose the right capacitor value carefully with considering high-capacitance ceramic capacitors DC bias effect, which has a strong influence on the final effective capacitance.

Inductor Selection

The performance of inductor affects the power supply's steady state operation, transient behavior, loop stability, and buck converter efficiency. The inductor value, DC resistance (DCR), and saturation current influences both efficiency and the magnitude of the output voltage ripple. Larger inductance value reduces inductor current ripple and therefore leads to lower output voltage ripple. For a fixed DCR, a larger value inductor yields higher efficiency via reduced RMS and core losses. However, a larger inductor within a given inductor family will generally have a greater series resistance, thereby counteracting this efficiency advantage.

Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value at 0-A current depending on how the inductor vendor defines saturation. When selecting an inductor, choose its rated current especially the saturation current larger than its peak current during the operation.

To calculate the current in the worst case, use the maximum input voltage, minimum output voltage, maxim load current and minimum switching frequency of the application, while considering the inductance with -30% tolerance and low-power conversion efficiency.

For a buck converter, calculate the inductor minimum value as shown in equation (4).

$$L_{INDMIN} = \frac{V_{OUT} \times (V_{INMAX} - V_{OUT})}{V_{INMAX} \times K_{IND} \times I_{OUT} \times f_{SW}} \quad (4)$$

Where:

- K_{IND} is the coefficient of inductor ripple current relative to the maximum output current.

Therefore, the peak switching current of inductor, I_{LPEAK}, is calculated as in equation (5).

$$I_{LPEAK} = I_{OUT} + K_{IND} \times \frac{I_{OUT}}{2} \quad (5)$$

Set the current limit of the SCT9321/SCT9322 higher than the peak current I_{LPEAK} and select the inductor with the saturation current higher than the current limit. The inductor's DC resistance (DCR) and the core loss significantly affect the efficiency of power conversion. Core loss is related to the core material and different inductors have

different core loss. For a certain inductor, larger current ripple generates higher DCR and ESR conduction losses and higher core loss.

Output Capacitor Selection

For buck converter, the output capacitor value determines the regulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the most stringent of these three criteria.

For small output voltage ripple, choose a low-ESR output capacitor like a ceramic capacitor, for example, X5R and X7R family. Typically, 1～2x 22μF ceramic output capacitors work for most applications. Higher capacitor values can be used to improve the load transient response. Due to a capacitor's de-rating under DC bias, the bias can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance.

From the required output voltage ripple, use the equation (6) to calculate the minimum required effective capacitance, C_{OUT}.

$$C_{OUT} = \frac{\Delta I_{LPP}}{8 \times V_{OUTRipple} \times f_{SW}} \quad (6)$$

Where

- $V_{OUTRipple}$ is output voltage ripple caused by charging and discharging of the output capacitor.
- ΔI_{LPP} is the inductor peak to peak ripple current, equal to $k_{IND} * I_{OUT}$.
- f_{SW} is the converter switching frequency.

The allowed maximum ESR of the output capacitor is calculated by the equation (7).

$$R_{ESR} = \frac{V_{OUTRipple}}{\Delta I_{LPP}} \quad (7)$$

The output capacitor affects the crossover frequency f_C. Considering the loop stability and effect of the internal loop compensation parameters, choose the crossover frequency less than 55 kHz ($\frac{1}{10} \times f_{SW}$) without considering the feed-forward capacitor. A simple estimation for the crossover frequency without feed forward capacitor is shown in equation (8), assuming C_{OUT} has small ESR.

$$C_{OUT} > \frac{18k \times G_M \times G_{MP} \times 0.8V}{2\pi \times V_{OUT} \times f_C} \quad (8)$$

Where

- G_M is the transfer conductance of the error amplifier (300uS).
- G_{MP} is the gain from internal COMP to inductor current, which is 5A/V.
- f_C is the cross over frequency.

Additional capacitance de-rating for aging, temperature and DC bias should be factored in which increases this minimum value. Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. The capacitor data sheets specify the RMS (Root Mean Square) value of the maximum ripple current. Equation (9) can be used to calculate the RMS ripple current the output capacitor needs to support.

$$I_{COUTRMS} = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{\sqrt{12} \cdot V_{IN} \cdot L_{IND} \cdot f_{SW}} \quad (9)$$

Output Feed-Forward Capacitor Selection

The SCT9321/SCT9322 has the internal integrated loop compensation as shown in the function block diagram. The compensation network includes a 18k resistor and a 7.6nF capacitor. Usually, the type II compensation network has a phase margin between 60 and 90 degree. However, if the output capacitor has ultra-low ESR, the converter results in low phase margin. To increase the converter phase margin, a feed-forward cap C_{ff} is used to boost the phase margin at the converter cross-over frequency f_c. Equation (10) is used to calculate the feed-forward capacitor.

$$C_{ff} = \frac{1}{2\pi \cdot f_C \times R_1} \tag{10}$$

Output Feedback Resistor Divider Selection

The SCT9321/SCT9322 features external programmable output voltage by using a resistor divider network R1 and R2 as shown in the typical application circuit Figure11. Use equation (11) to calculate the resistor divider values.

$$R_1 = \frac{(V_{OUT} - V_{ref}) \times R_2}{V_{ref}} \tag{11}$$

Set the resistor R2 value to be approximately 30k. Slightly increasing or decreasing R1 can result in closer output voltage matching when using standard value resistors.

Table 1. Recommended External Components

Vout	L1	COUT	R1	R2	R3	Cf
3.3V	6.5uH	3*22uF	93.5k	30k	2k	22p
5V	10uH	3*22uF	158k	30k	2k	100p
12V	22uH	3*22uF	422k	30k	2k	330p

External Compensation network Design

The SCT9321/2 employs peak current mode control for easy compensation and fast transient response.

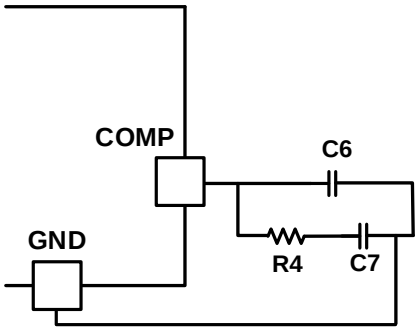


Figure 12. External Compensation Circuit

An external network comprising resister R4, ceramic capacitors C7 and optional C6 connected to the COMP pin is used for the loop compensation. The equation12 shows the close-loop small signal transfer function.

$$H(S) = \left[A_{EA} * \frac{1 + \frac{S}{2\pi * f_{Z1}}}{\left(1 + \frac{S}{2\pi * f_{P1}}\right) * \left(1 + \frac{S}{2\pi * f_{P3}}\right)}\right] * \left[G_{ISNS} * \frac{V_{OUT}}{I_{OUT}} * \frac{1 + \frac{S}{2\pi * f_{Z2}}}{1 + \frac{S}{2\pi * f_{P2}}}\right] * \frac{V_{FB}}{V_{OUT}} \tag{12}$$

where

- A_{EA} is error amplifier voltage gain
- G_{ISNS} is COMP to SW current trans-conductance, 5A/V typically

The DC voltage gain of the loop is given by equation 13.

$$A_{VDC} = A_{EA} * G_{ISNS} * \frac{V_{FB}}{I_{OUT}} \quad (13)$$

The system has two noteworthy poles: one is due to the compensation capacitor C7 and the error amplifier output resistor. The other is caused by the output capacitor and the load resistor. These poles as located at:

$$f_{P1} = \frac{1}{2\pi * R_{OEA} * C_7} = \frac{G_{EA}}{2\pi * A_{EA} * C_7} \quad (14)$$

$$f_{P2} = \frac{1}{2\pi * R_{LOAD} * C_{OUT}} = \frac{I_{OUT}}{2\pi * V_{OUT} * C_{OUT}} \quad (15)$$

where

- R_{OEA} is error amplifier output resistor
- G_{EA} is Error amplifier trans-conductance, 300uS typically
- R_{LOAD} is equivalent load resistor

The system has one zero of importance from R4 and C7. fz1 is used to counteract the fp2, and fz1 located at:

$$f_{Z1} = \frac{1}{2\pi * C_7 * R_4} \quad (16)$$

The system may have another important zero if the output capacitor has a large capacitance or a high ESR value. The zero, due to the ESR and the capacitance of the output capacitor is calculated by Equation 17.

$$f_{Z2} = \frac{1}{2\pi * C_{OUT} * ESR} \quad (17)$$

In this case, a third pole set by the optional compensation capacitor C6 and the compensation resistor R4 is used to compensates the effect of the ESR zero. This pole is calculated by Equation 18.

$$f_{P3} = \frac{1}{2\pi * C_6 * R_4} \quad (18)$$

The crossover frequency of converter is shown in Equation 19.

$$f_C = \frac{V_{FB}}{V_{OUT}} * \frac{G_{EA} * G_{ISNS} * R_4}{2\pi * C_{OUT}} \quad (19)$$

The system crossover frequency, where the feedback loop has unity gain, is important. A lower crossover frequency results in slower line and load transient response. A higher crossover frequency could cause the system unstable. A recommended rule of thumb is to set the crossover frequency to be approximately 1/10 of switching frequency.

The following steps can be followed to calculate the external compensation components. Calculate the compensation resistor R4 with Equation 20 once crossover frequency is selected.

$$R_4 = \frac{V_{OUT}}{V_{FB}} * \frac{2\pi * C_{OUT} * f_C}{G_{EA} * G_{ISNS}} \quad (20)$$

Then calculate C7 by placing a compensation zero at or before the output stage pole.

$$C_7 = \frac{R_{LOAD} * C_{OUT}}{R4} \quad (21)$$

Determine if the optional compensation capacitor C6 is required. Generally, it is required if the ESR zero f_{Z2} is located less than half of the switching frequency. Then fp3 can be used to cancel fz2. C6 can be calculated with Equation 22.

$$C_6 = \frac{C_{OUT} \times ESR}{R_4} \quad (22)$$

Table 2 lists typical values of compensation components for some standard output voltages with various output ceramic capacitors and inductors. The values of the compensation components have been optimized for fast transient responses and good stability. For the conditions not list in Table 2, customers can use Equation 20-Equation 22 to optimize the compensation components.

Table 2: Compensation Values for Typical Output Voltage/Capacitor Combinations

Vout	L1	COUT	R4	C7	C6
3.3V	10uH	2*22uF	25K	3.3nF	-
5V	10uH	2*22uF	30K	3.3nF	-
12V	22uH	2*22uF	50K	3.3nF	-

Application Waveforms

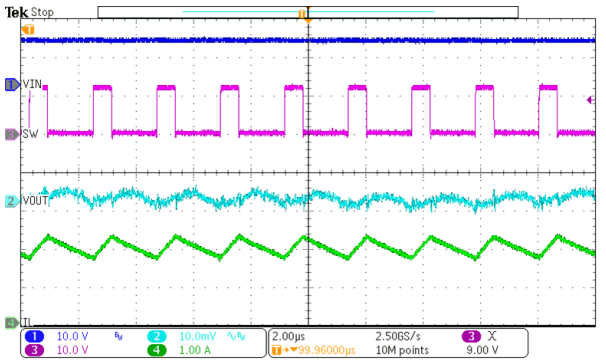


Figure 13. SW node waveform and Output Ripple
VIN=12V, IOUT=2A

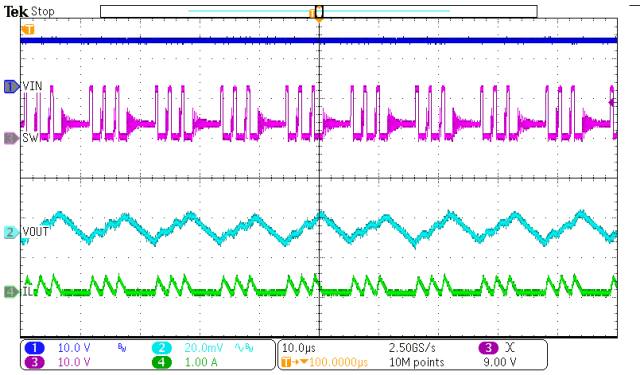


Figure 14. SW node Waveform and Output Ripple
VIN=12V, IOUT=100mA

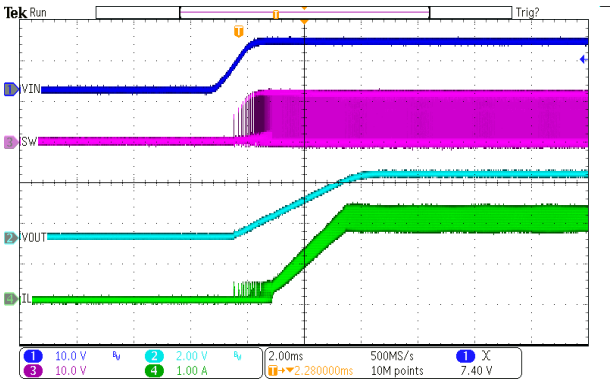


Figure 15. Power Up
VIN=12V, VOUT=3.3V, IOUT=2A

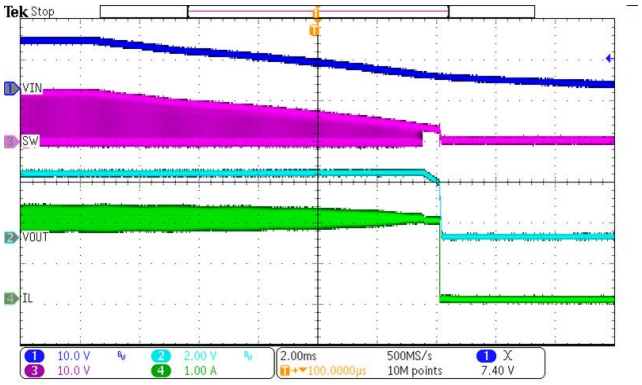


Figure 16. Power Down
VIN=12V, VOUT=3.3V, IOUT=2A

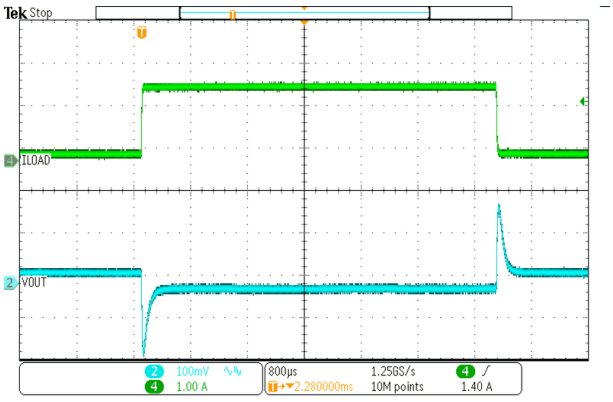


Figure 17. Load Transient
VOUT=3.3V, IOUT=0.2A to 1.8A, SR=250mA/us

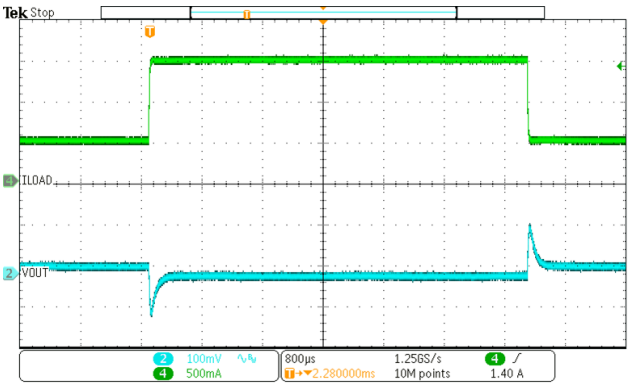


Figure 18. Load Transient
VOUT=3.3V, IOUT=0.5A to 1.5 A, SR=250mA/us

Layout Guideline

The regulator could suffer from instability and noise problems without carefully layout of PCB. Radiation of high-frequency noise induces EMI, so proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize coupling. The input capacitor needs to be very close to the VIN pin and GND pin to reduce the input supply ripple. Place the capacitor as close to VIN pin as possible to reduce high frequency ringing voltage on SW pin as well. Figure 20 is the recommended PCB layout of SCT9321/SCT9322.

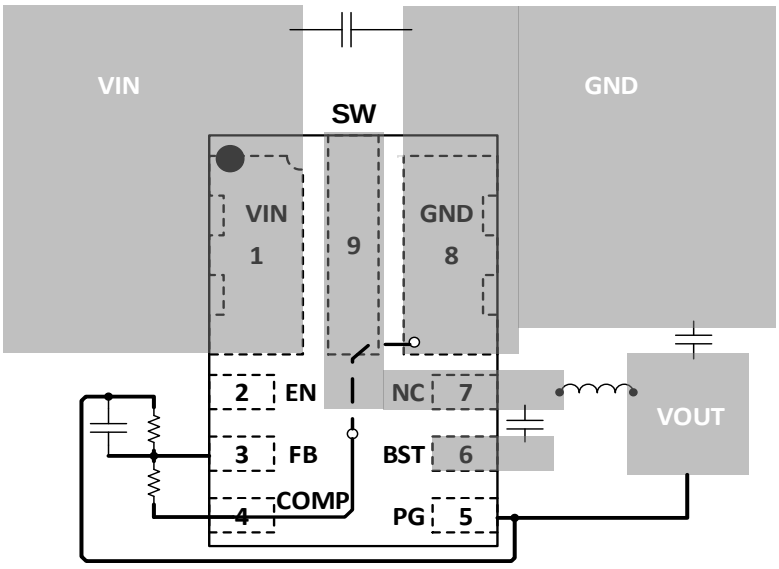


Figure 19. PCB Layout Example for application with internal compensation

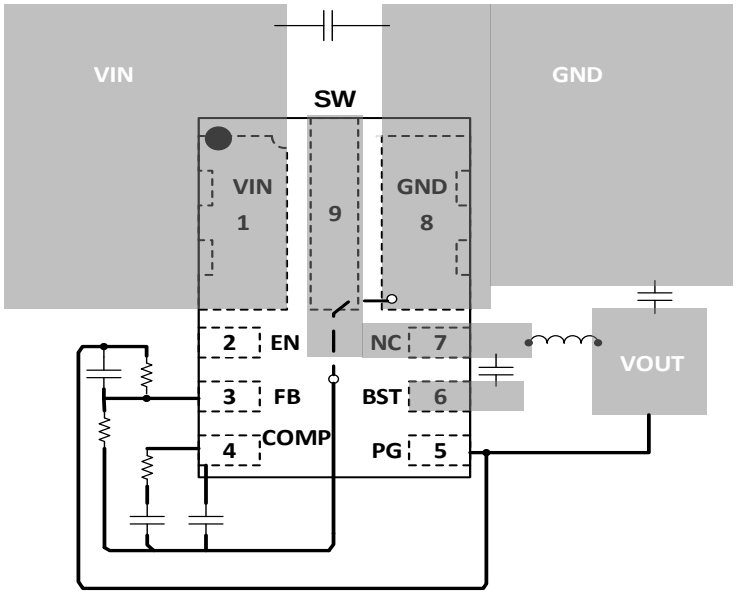


Figure 20. PCB Layout Example for application with external compensation

The layout needs be done with well consideration of the thermal. A large top layer ground plate using multiple thermal vias is used to improve the thermal dissipation. The bottom layer is a large ground plane connected to the top layer ground by vias.

Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using Equation (12).

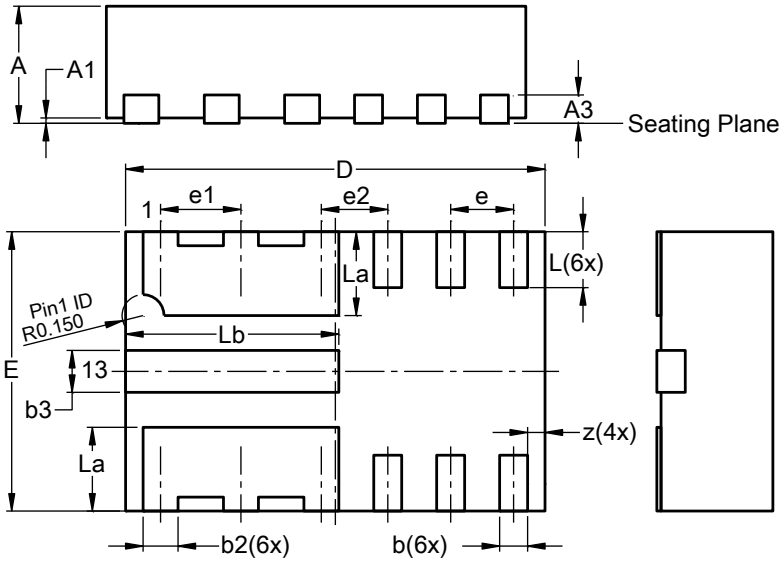
$$P_{D(MAX)} = \frac{125 - T_A}{R_{\theta JA}} \quad (12)$$

where

- T_A is the maximum ambient temperature for the application.
- $R_{\theta JA}$ is the junction-to-ambient thermal resistance given in the Thermal Information table.

The real junction-to-ambient thermal resistance $R_{\theta JA}$ of the package greatly depends on the PCB type, layout, thermal pad connection and environmental factor. Using thick PCB copper and soldering the GND to a large ground plate enhance the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also enhance the thermal capability.

PACKAGE INFORMATION



NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

SYMBOL	Unit: Millimeter		
	MIN	TYP	MAX
A	0.75	0.85	0.80
A1	0.00	0.05	0.02
A3	-	-	0.203
b	0.15	0.25	0.20
b2	0.20	0.30	0.25
b3	0.25	0.35	0.30
D	2.95	3.05	3.00
E	1.95	2.05	2.00
e	0.45 (BSC)		
e1	0.575 (BSC)		
e2	0.475 (BSC)		
L	0.35	0.45	0.40
La	0.55	0.65	0.60
Lb	1.475	1.575	1.525
z	-	-	0.125

