TS321 低功耗单路运算放大器

1 特性

- 宽电源范围
  - 3V 至 30V 的单电源供电范围
  - ±1.5 V 至 ±15 V 的双电源供电范围
- 从 0V 至 3.5V（最低值）(V_{CC} = 5 V) 的大输出电压摆幅
- 低电源电流：500μA（典型值）
- 低输入偏置电流：20nA（典型值）
- 与高容式负载一起工作时保持稳定

2 应用

- 台式计算机
- HVAC：采暖、通风和空调
- 便携式媒体播放器
- 冰箱
- 洗衣机：高端和低端

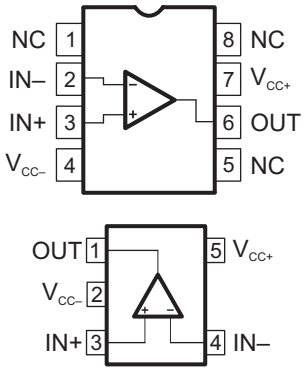
3 说明

TS321 是一种双极运算放大器，适用于注重节省空间的成本敏感型 应用 。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TS321	SOIC (8)	4.90mm × 3.90mm
	SOT-23 (5)	2.90mm × 1.60mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



目录

4 修订历史记录

Changes from Revision C (April 2015) to Revision D **Page**

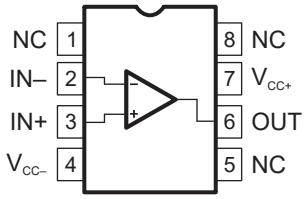
- 在*器件信息* 表中将 SOIC 封装引脚数量从“SOIC (14)”更正为“SOIC (8)” 1

Changes from Revision B (December 2013) to Revision C **Page**

- 已添加 *引脚配置和功能* 部分、*ESD 额定值* 表、*特性* *说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 1

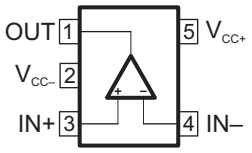
5 Pin Configuration and Functions

D Package
8-Pin SOIC
(Top View)



NC - no internal connection

DBV Package
5-Pin SOT-23
(Top View)



Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOIC	SOT-23		
IN–	2	4	I	Negative input
IN+	3	3	I	Positive input
NC	1	—	—	Do not connect
	5			
	8			
OUT	6	1	O	Output
V_{CC-}	4	2	—	Negative supply
V_{CC+}	7	5	—	Positive supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
	Supply voltage, V_{CC}	Single supply		32	V
		Dual supplies		±16	
	Differential input voltage(2), V_{ID}			±32	V
	Input voltage range (3), V_I		–0.3	32	V
	Input current, I_{IK}			50	mA
	Duration of output short circuit to ground, t_{short}			Unlimited	
	Operating virtual junction temperature, T_J			150	°C
	Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Differential voltages are at IN+ with respect to IN–.
(3) Input voltages are at IN with respect to $V_{CC–}$.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Single supply	3	30	V
		Dual supply	±1.5	±15	
T_A	Operating free-air temperature		–40	125	°C

6.4 Thermal Information: TS321

THERMAL METRIC(1) (2)(3)		TS321		UNIT
		D (SOIC)	DBV (SOT-23)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97	206	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Maximum power dissipation is a function of TJ(max), qJA, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is PD = [TJ(max) – TA] / qJA. Selecting the maximum of 150°C can effect reliability.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

6.5 Electrical Characteristics

V_{CC+} = 5 V, V_{CC-} = GND, V_O = 1.4 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	R_S = 0, 5 V < V_{CC+} < 30 V 0 < V_{IC} < (V_{CC+} – 1.5 V)	T_A = 25°C		0.5	4	mV
			T_A = Full range			5	
I_{IO}	Input offset current	T_A = 25°C			2	30	nA
		T_A = Full range				50	
I_{IB}	Input bias current(1)	T_A = 25°C			20	150	nA
		T_A = Full range				200	
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, R_L = 2 kΩ V_O = 1.4 V to 11.4 V	T_A = 25°C	50	100		V/mV
			T_A = Full range	25			
V_{ICR}	Common-mode input voltage(2)	V_{CC} = 30 V	T_A = 25°C	0		V_{CC+} – 1.5	V
			T_A = Full range	0		V_{CC+} – 2	
V_{OH}	High-level output voltage	V_{CC} = 30 V R_L = 2 kΩ	T_A = 25°C	26	27		V
			T_A = Full range	25.5			
		V_{CC} = 30 V R_L = 10 kΩ	T_A = 25°C	27	28		
			T_A = Full range	26.5			
		V_{CC} = 5 V R_L = 2 kΩ	T_A = 25°C	3.5			
			T_A = Full range	3			
V_{OL}	Low-level output voltage	R_L = 10 kΩ	T_A = 25°C		5	15	mV
			T_A = Full range			20	
GBP	Gain bandwidth product	V_{CC} = 30 V, V_I = 10 mV, R_L = 2 kΩ f = 100 kHz, C_L = 100 pF T_A = 25°C			0.8		MHz
SR	Slew rate	V_{CC} = 15 V, V_I = 0.5 V to 3 V, R_L = 2 kΩ, C_L = 100 pF, unity gain, T_A = 25°C			0.4		V/µs
φ_m	Phase margin	T_A = 25°C			60		°
CMRR	Common-mode rejection ratio	R_S ≤ 10 kΩ T_A = 25°C		65	85		dB
I_{SOURCE}	Output source current	V_{CC} = 15 V, V_O = 2 V, V_{ID} = 1 V T_A = 25°C		20	40		mA
I_{SINK}	Output sink current	V_{CC} = 15 V, V_{ID} = 1 V V_O = 2 V T_A = 25°C		10	20		mA
		V_{CC} = 15 V, V_{ID} = 1 V V_O = 0.2 V T_A = 25°C		12	50		µA
I_O	Short-circuit to GND	V_{CC} = 15 V, T_A = 25°C			40	60	mA
SVR	Supply-voltage rejection ratio	V_{CC} = 5 V to 30 V, T_A = 25°C		65	110		dB
I_{CC}	Total supply current	V_{CC} = 5 V T_A = 25°C, no load			500	800	µA
		V_{CC} = 30 V T_A = 25°C, no load			600	900	
		V_{CC} = 5 V T_A = full range, no load			600	900	
		V_{CC} = 30 V T_A = full range, no load				1000	
THD	Total harmonic distortion	V_{CC} = 30 V, V_O = 2 V_{pp}, A_V = 20 dB R_L = 2 k, f = 1 kHz, C_L = 100 pF, T_A = 25°C			0.015%		

(1) The direction of the input current is out of the device. This current essentially is constant, independent of the state of the output, so no loading change exists on the input lines.
(2) The input common-mode voltage of either input signal should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V_{CC+} – 1.5 V, but either or both inputs can go to 32 V without damage.

Electrical Characteristics (continued)

V_{CC+} = 5 V, $V_{CC–}$ = GND, V_O = 1.4 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
e_N	Equivalent input noise voltage	V_{CC} = 30 V, f = 1 kHz, R_S = 100 Ω T_A = 25°C		50		

6.6 Typical Characteristics

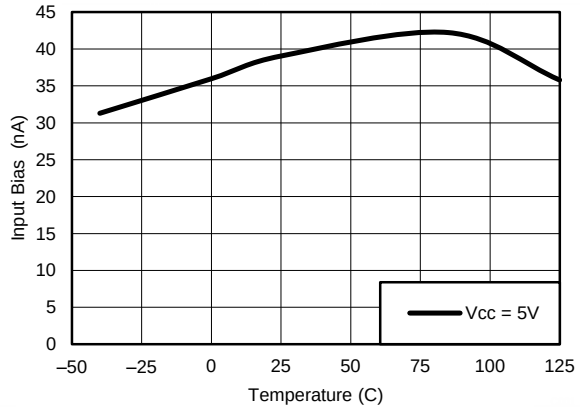


图 1. Input Current vs Temperature

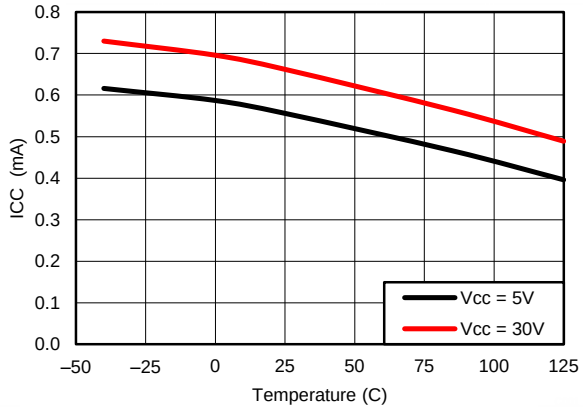


图 2. Supply Current vs Temperature

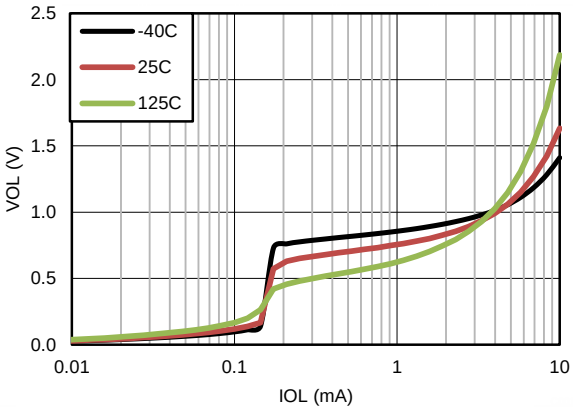


图 3. Output Sinking Characteristics

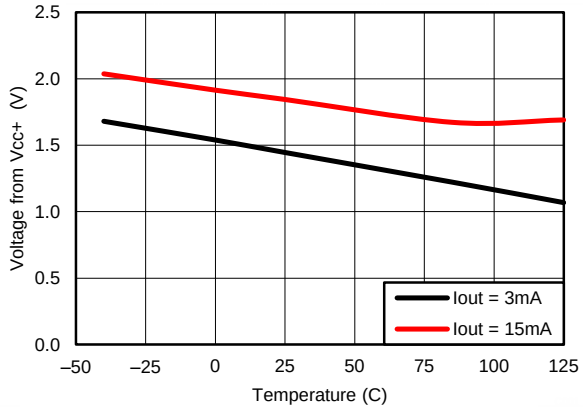


图 4. Output Sourcing Characteristics

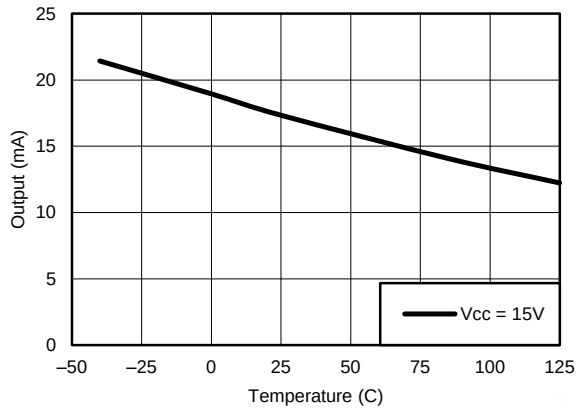


图 5. Short-Circuit Current to Supply (1)

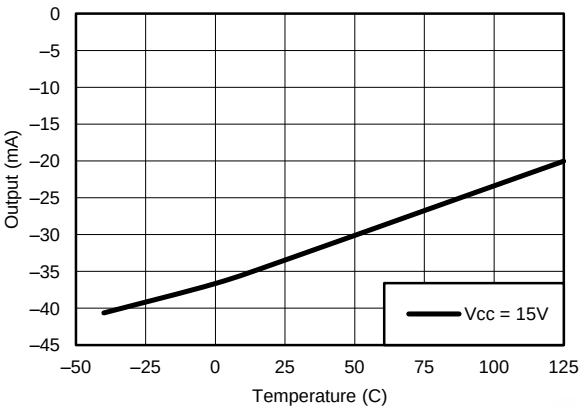


图 6. Short-Circuit Current to Ground

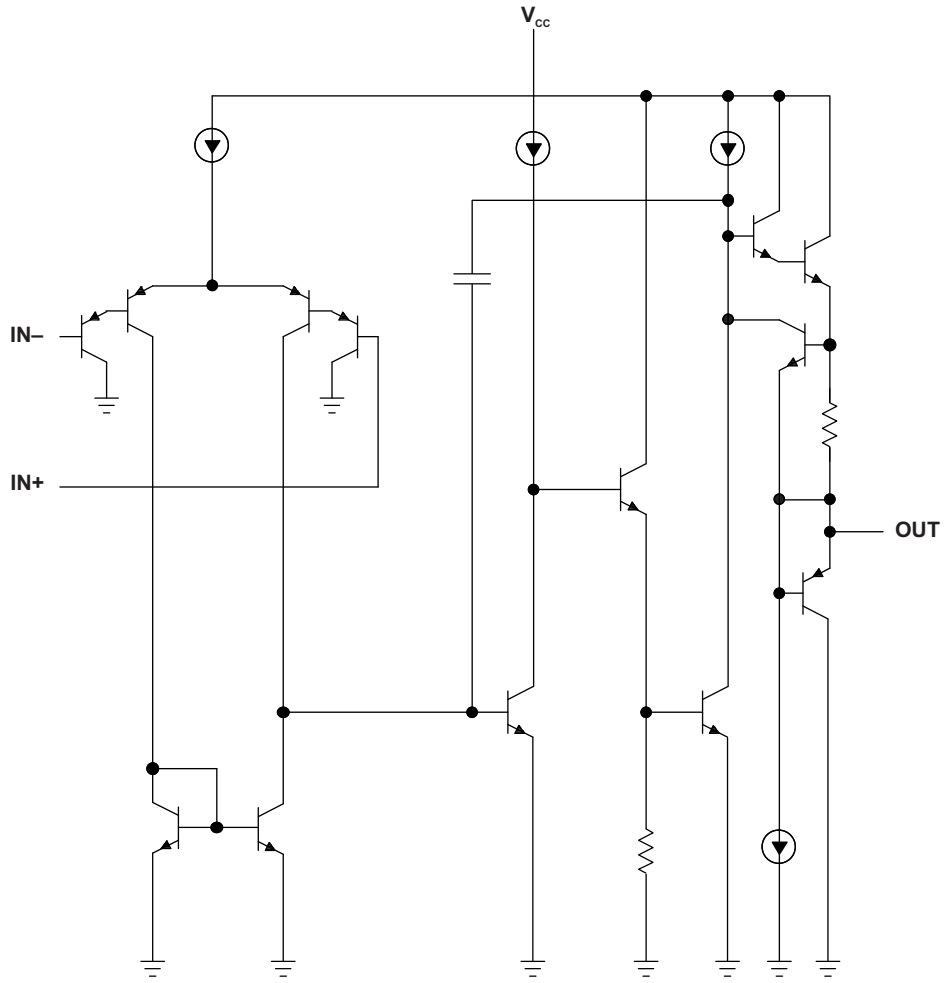
(1) Short circuits from outputs to VCC can cause excessive heating and eventual destruction.

7 Detailed Description

7.1 Overview

The TS321 is a single-channel operational amplifier. The device can handle a single supply between 3 V and 30 V or a dual-supply between ±1.5 V and ±15 V. Available in the small SOT-23 package, the TS321 is great for saving space in any application.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Voltage

The TS321 can be powered from a single supply between 3 V and 30 V or a dual-supply between ±1.5 V and ±15 V.

7.3.2 Gain Bandwidth Product

Gain bandwidth product is found by multiplying a measured bandwidth of the amplifier by the gain at which that bandwidth was measured. The TS321 has a gain bandwidth of 0.8 MHz.

7.3.3 Slew Rate

The slew rate is the rate at which an operational amplifier can change the output when there is a change on the input. The TS321 has a 0.4-V/μs slew rate.

Feature Description (接下页)

7.3.4 Input Common-Mode Range

The valid common-mode range is from device ground pin to VCC – 1.5 V (VCC – 2 V across temperature). Inputs may exceed VCC up to the maximum VCC without device damage. At least one input must be in the valid input common-mode range for output to be correct phase. If both inputs exceed valid range then output phase is undefined. If either input is less than –0.3 V then input current must be limited to 1 mA and output phase is undefined.

7.3.5 Stability With High Capacitive Loads

Operational amplifiers have reduced phase margin when there is a direct capacitance on the output. The stability is affected most when the amplifier is set to unity gain. Small signal response to a step input of 100 mV reveals the loop stability with a range of capacitors. See SLVA381 to correlate response waveform to phase margin. The responses at 1 nF or less indicate acceptable phase margin. The responses at 1 uF and above indicate good phase margin.

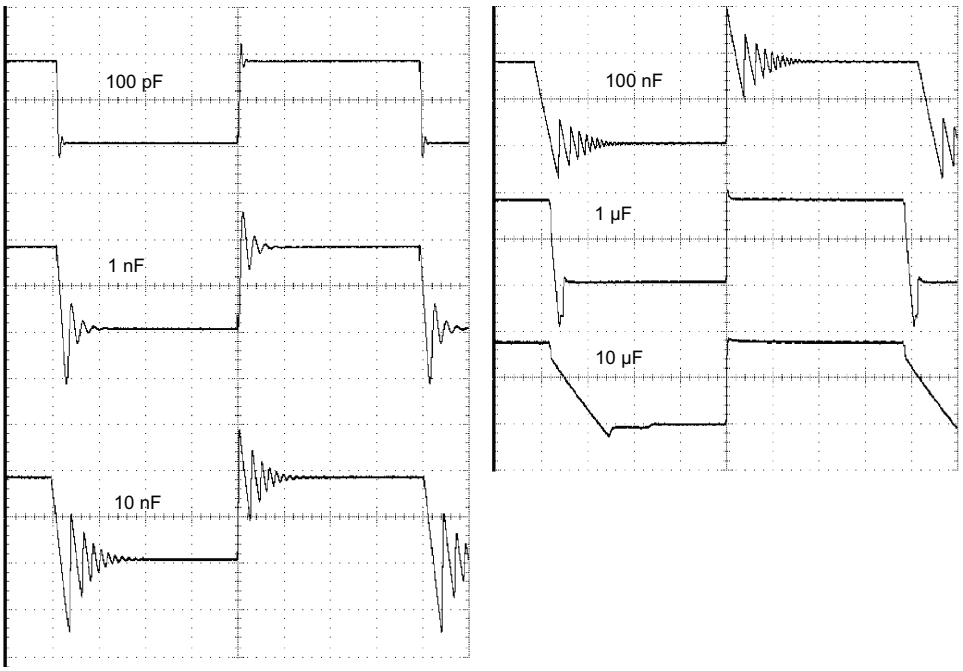


图 7. Small-Signal Response

7.4 Device Functional Modes

The TS321 is powered on when the supply is connected. This device can operate as a single-supply operational amplifier or dual-supply amplifier depending on the application.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TS321 operational amplifier is useful in a wide range of signal conditioning applications. Inputs can be powered before VCC for flexibility in multiple supply circuits.

8.2 Typical Application

A typical application for an operational amplifier in an inverting amplifier. This amplifier takes a positive voltage on the input, and makes the voltage a negative voltage of the same magnitude. In the same manner, the amplifier makes negative voltages positive.

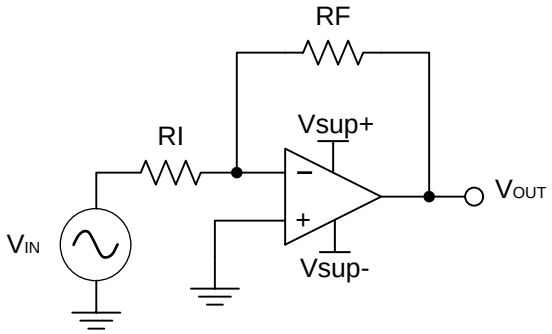


图 8. Typical Application Schematic

8.2.1 Design Requirements

The supply voltage must be selected such that the supply voltage is larger than the input voltage range and output range. For instance, this application scales a signal of ±0.5 V to ±1.8 V. Setting the supply at ±12 V is sufficient to accommodate this application.

8.2.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier:

$$A_V \quad \frac{VOUT}{VIN} \tag{1}$$

$$A_V \quad \frac{1.8}{-0.5} \quad -3.6 \tag{2}$$

Once the desired gain is determined, select a value for RI or RF. Selecting a value in the kilohm range is desirable because the amplifier circuit uses currents in the milliamp range. This ensures the part does not draw too much current. This example selects 10 kΩ for RI which means 36 kΩ is be used for RF. This is determined by 公式 3.

$$A_V \quad -\frac{RF}{RI} \tag{3}$$

Typical Application (接下页)

8.2.3 Application Curve

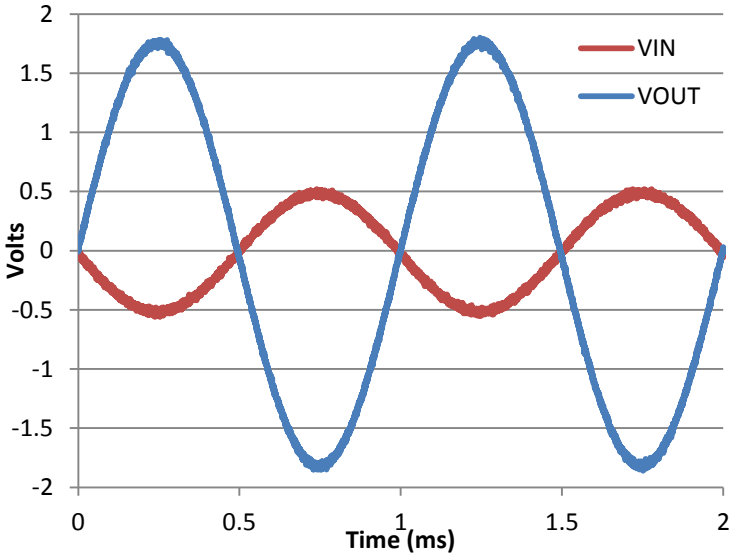


图 9. Input and Output Voltages of the Inverting Amplifier

9 Power Supply Recommendations

The TS321 is specified to operate between 3 V and 30 V or a dual supply between ±1.5 V and ±15 V.

CAUTION

Supply voltages larger than 32 V for a single supply, or outside the range of ±16 V for a dual supply can permanently damage the device (see the *Absolute Maximum Ratings*).

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout* section.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see SLOA089.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in *Layout Example*.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

10.2 Layout Example

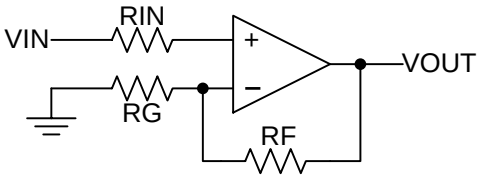


图 10. Operational Amplifier Schematic for Noninverting Configuration

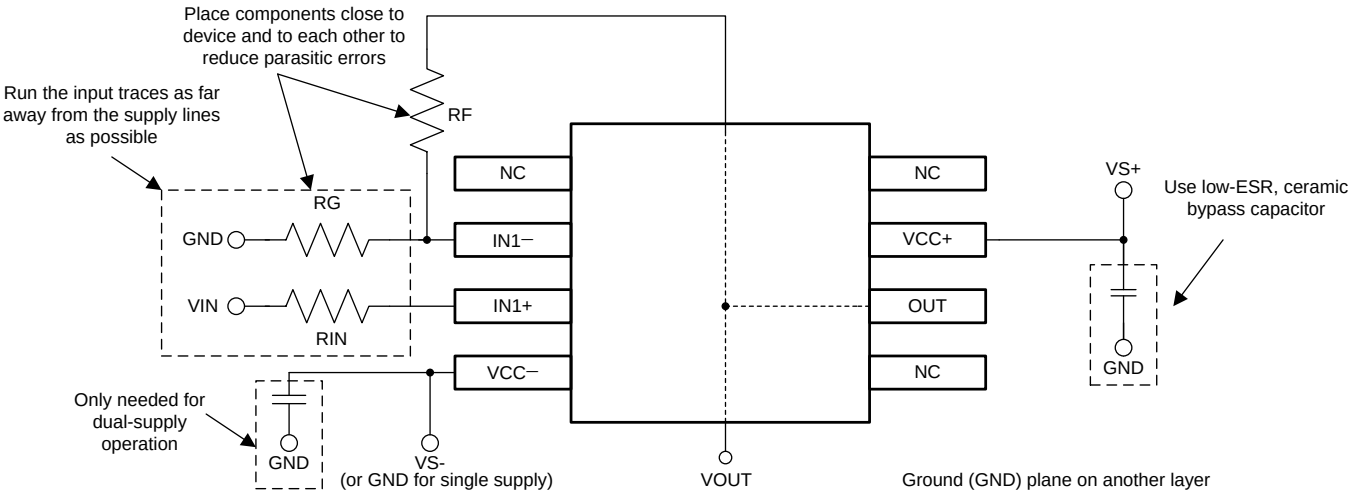


图 11. Operational Amplifier Board Layout for Noninverting Configuration

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

有关详细信息，请参阅以下内容：

- *简化稳定性检查*
- *《电路板布局布线技巧》*

11.2 商标

All trademarks are the property of their respective owners.

11.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.4 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

PACKAGE OPTION ADDENDUM

10-Dec-2020

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS321ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SR321I	Samples
TS321IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(9C1G, 9C1S)	Samples
TS321IDBVRE4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	9C1G	Samples
TS321IDBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	9C1G	Samples
TS321IDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(9C1G, 9C1S)	Samples
TS321IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SR321I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OPTION ADDENDUM

10-Dec-2020

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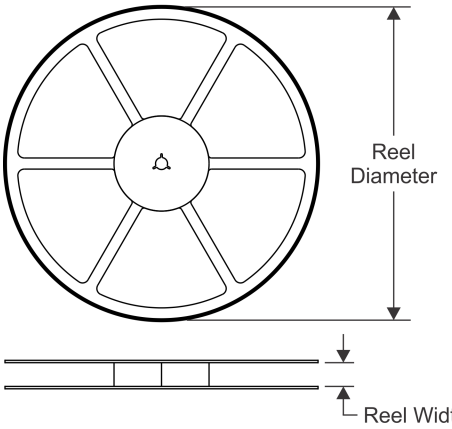
PACKAGE MATERIALS INFORMATION

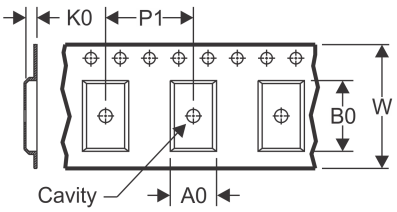
23-Jul-2021

TAPE AND REEL INFORMATION

REEL DIMENSIONS

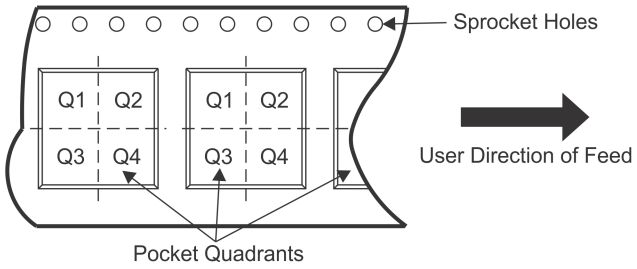


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



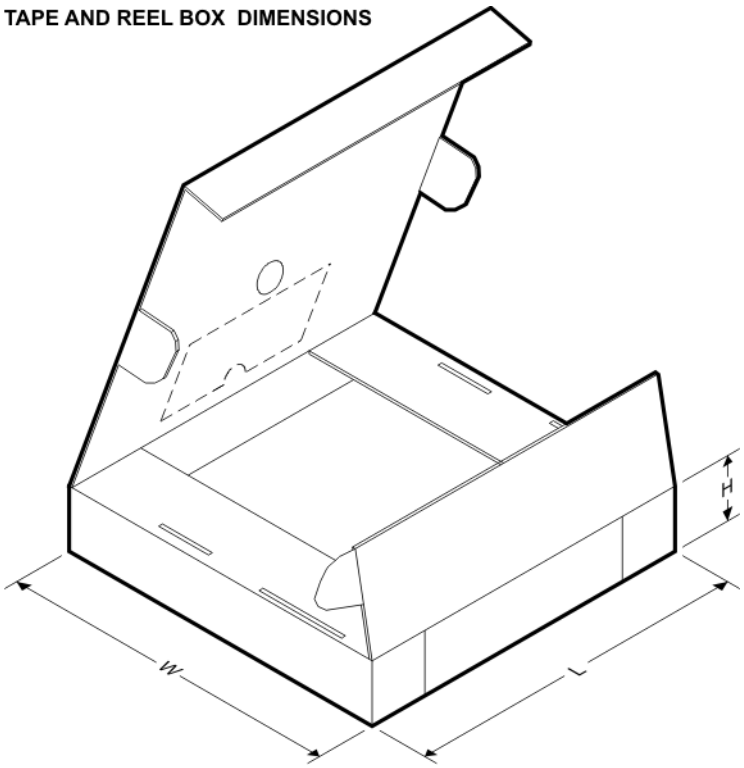
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS321IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TS321IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TS321IDBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TS321IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TS321IDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TS321IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

23-Jul-2021

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

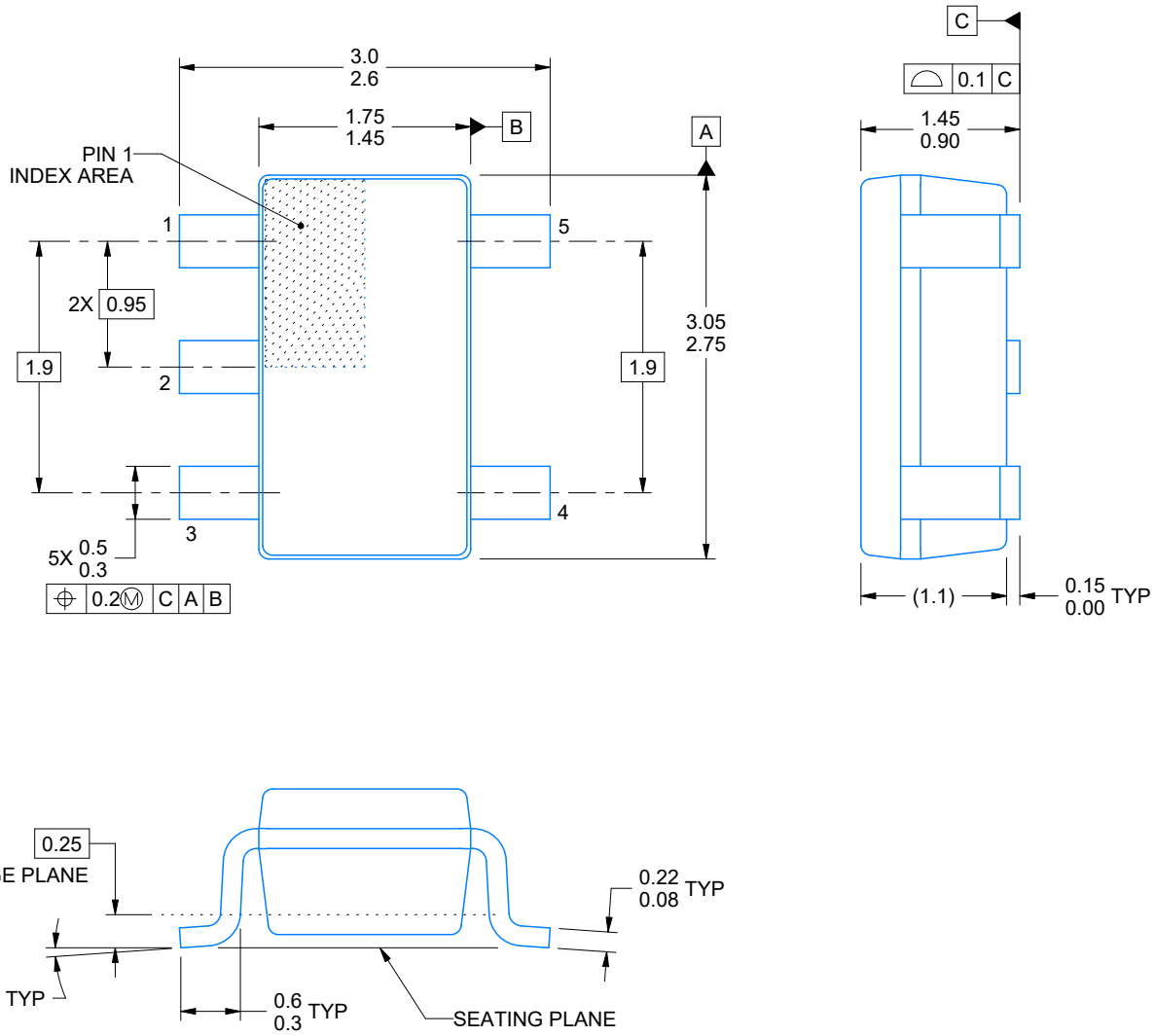
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS321IDBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
TS321IDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TS321IDBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
TS321IDBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
TS321IDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TS321IDR	SOIC	D	8	2500	340.5	336.1	25.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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NOTES:

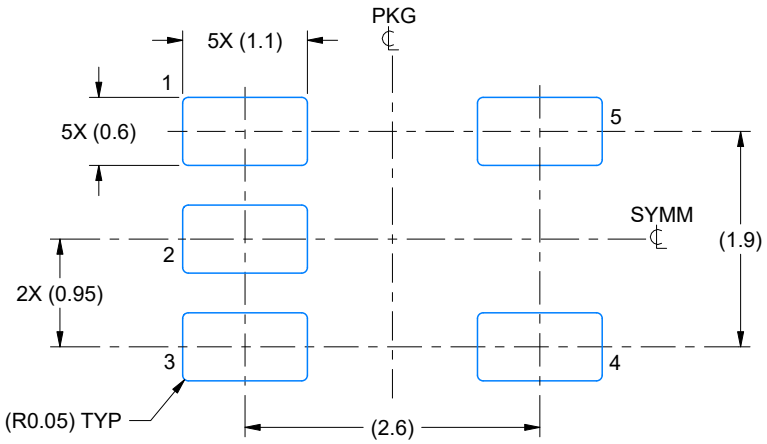
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.

EXAMPLE BOARD LAYOUT

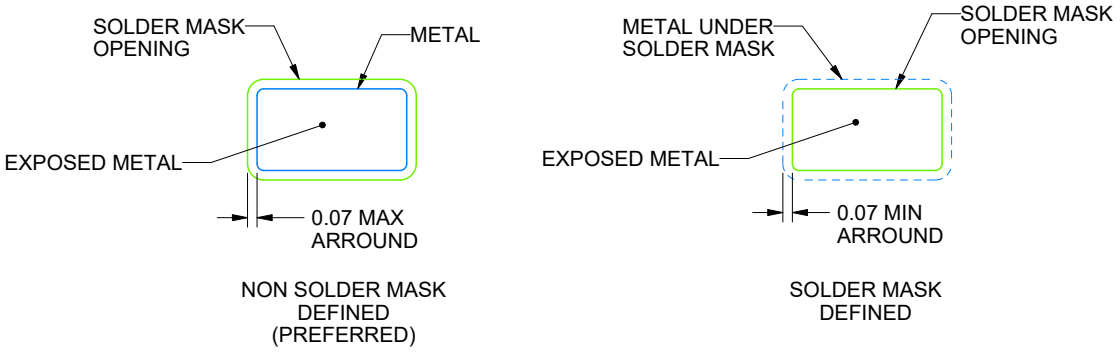
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

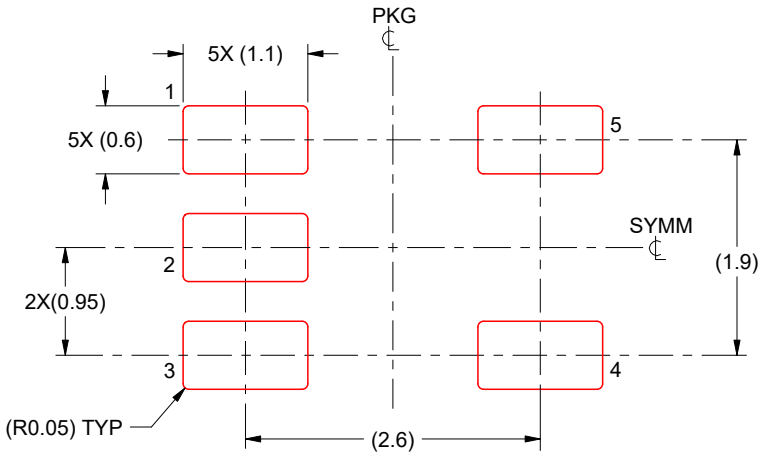
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

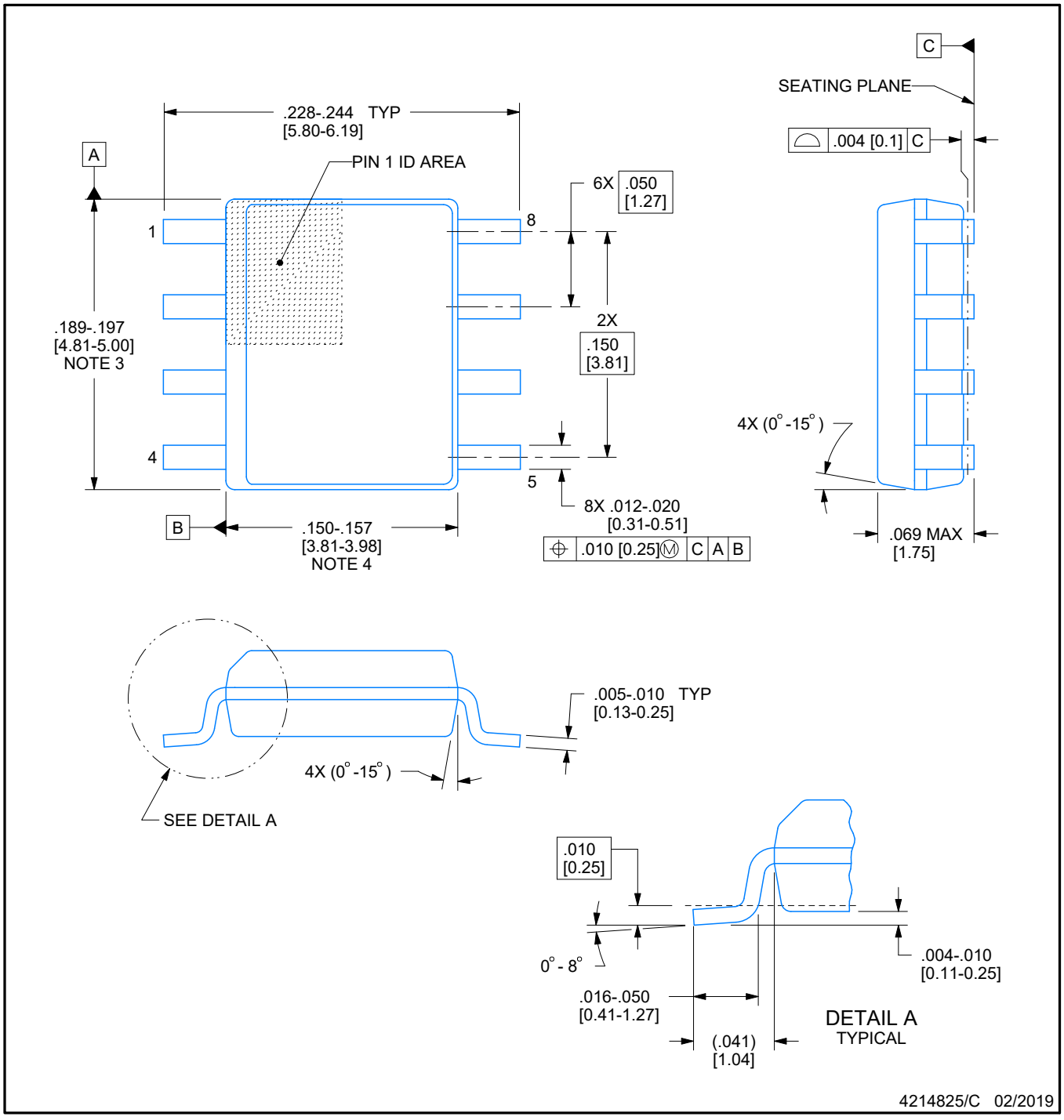
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

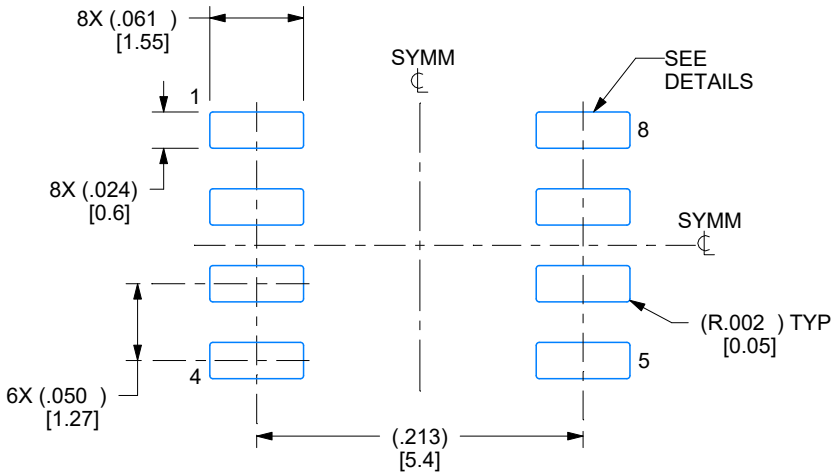
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

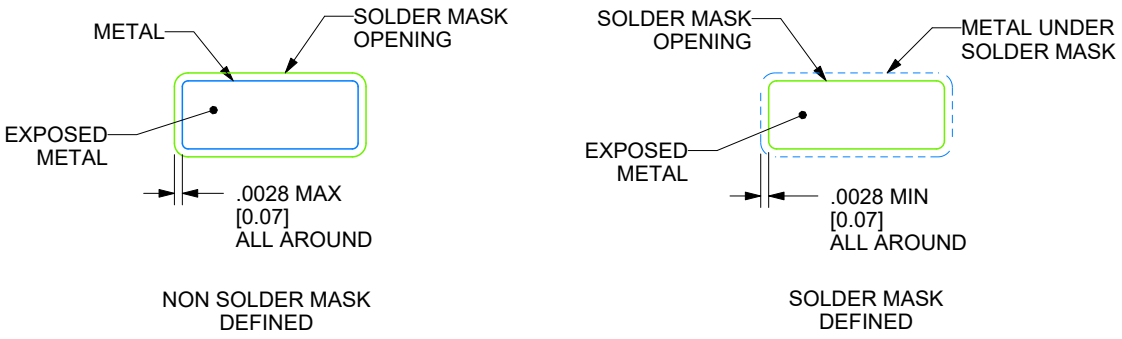
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

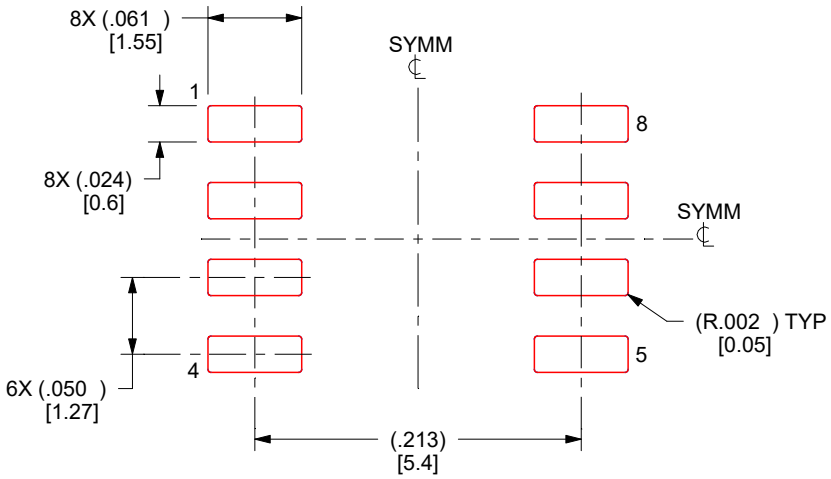
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.