SGM61720
High Efficiency, 2.5A, 60V Input Synchronous Step-Down Converter

GENERAL DESCRIPTION

The SGM61720 is a constant on-time control (COT) synchronous step-down converter with a wide input voltage range from 6V to 60V. The output voltage is adjustable up to 24V using the internal reference voltage. This device has 2.5A output current capability and operates at an almost fixed quasi-constant frequency (depending on V_{OUT} setting). With light load, the inductor current reaches zero in each cycle (DCM operation) and the device shifts into power-save mode in which frequency drops and becomes load dependent to maintain high efficiency.

The SGM61720 offers a broad set of features including input under-voltage lockout, internal soft-start, short-circuit protection, current limiting and thermal shutdown.

Using COT architecture, the device is capable of high step-down conversion ratios while offering excellent transient response with no need for loop compensation.

The SGM61720 is available in a Green SOIC-8 (Exposed Pad) package. It operates over an operating junction temperature range of -40℃ to +125℃.

FEATURES

- **Integrated 100mΩ/75mΩ Power MOSFETs**
- **Wide 6V to 60V Input Voltage Range**
- **2.5A/5V Output Current Capability**
- **Constant On-Time (COT) Control**
- **Power-Save Mode and PWM Mode**
- **1ms Internal Soft-Start for Inrush Current Limit**
- **Up to 24V Adjustable Output Voltage**
- **Pre-biased Startup**
- **-40℃ to +125℃ Operating Junction Temperature Range**
- **Available in a Green SOIC-8 (Exposed Pad) Package**

APPLICATIONS

Non-Isolated Telecommunication Buck Regulators
Secondary High Voltage Post-Regulators
Automotive Systems
Mobile Base Stations
48V Industrial Systems

TYPICAL APPLICATION

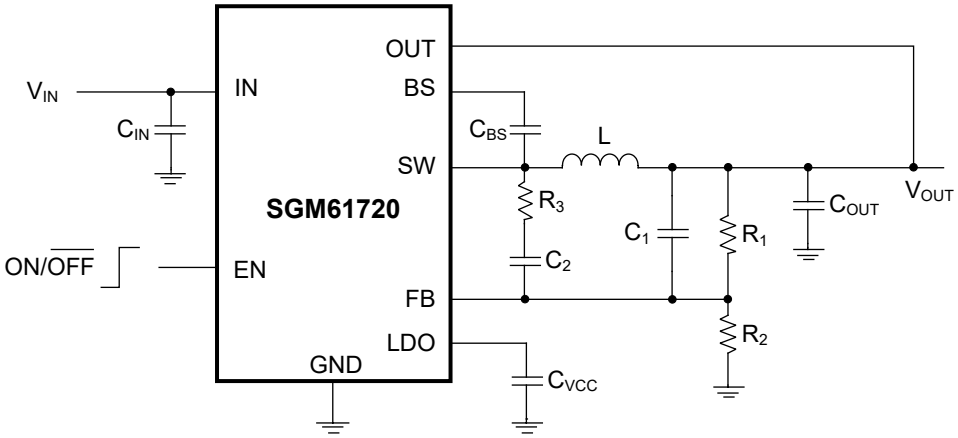


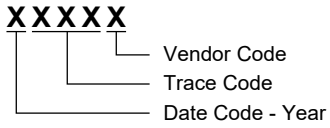
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61720	SOIC-8 (Exposed Pad)	SGM61720YPS8G/TR	SGM 61720YPS8 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Voltage 65V
OUT Voltage 30V
EN, SW Voltages ..... V_{IN} + 0.3V
BS Voltage ..... SW + 6V
FB Voltage 6V
Package Thermal Resistance
SOIC-8 (Exposed Pad), θ_{JA} ..... 39℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 2000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Supply Input Voltage Range ..... 6V to 60V
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

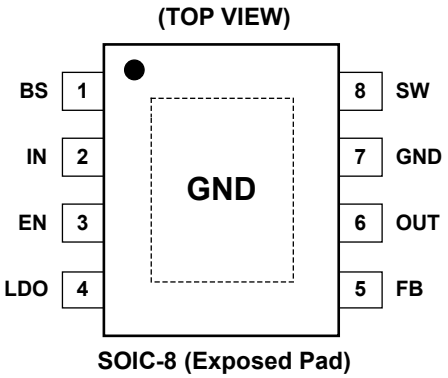
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	FUNCTION
1	BS	Bootstrap Pin. Connect a 0.1μF ceramic capacitor between BS pin to SW pin. This capacitor provides power supply to the integrated high-side MOSFET gate driver.
2	IN	Input Supply Voltage Pin. Decouple this pin to GND with a low ESR ceramic capacitor.
3	EN	Enable Pin. The device is enabled if the voltage on this pin exceeds the 1.5V rising threshold. It can be used to program the UVLO with a resistor divider on the IN pin. Do not leave this pin floating.
4	LDO	Internal LDO Voltage Output. Connect a 4.7μF ceramic capacitor from this pin to ground.
5	FB	Feedback (Sense) Input Pin for Output Voltage and Ripple. Connect to the center point of the resistor divider to program the output voltage and the ripple injection network.
6	OUT	Power Supply for Device from Output. OUT is a power source pin coming from the output. Note that V_{IN} can be as high as 60V that is not suitable to power the device internal circuit. Should not exceed 30V.
7	GND	Device Ground.
8	SW	Switching Node. Connect this pin to the switching node of the output inductor.
GND	Exposed Pad	Power Ground Exposed Pad. Must be connected to GND plane.

ELECTRICAL CHARACTERISTICS

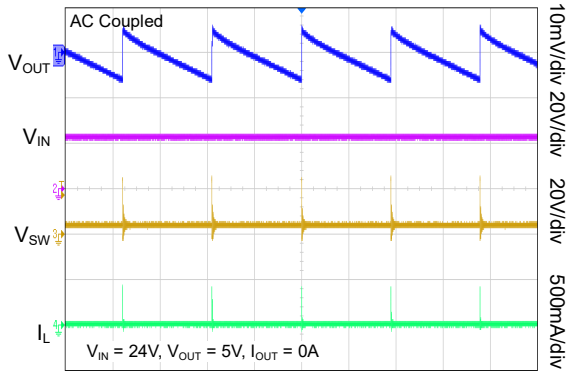
(T_J = +25℃, V_{IN} = 48V, V_{OUT} = 5V, I_{OUT} = 1A, L = 22μH and C_{OUT} = 47μF, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}		6		60	V
Quiescent Current	I_Q	I_{OUT} = 0, V_{FB} = V_{REF} × 105%		90	110	μA
Shutdown Supply Current	I_{SD}	EN = GND		3	4	μA
SW Leakage Current	I_{SW}	V_{SW} = 60V		0.1	1	μA
EN Rising Input Threshold	V_{IH}	V_{IN} = 6V to 60V, T_J = -40℃ to +125℃	1.5			V
EN Falling Input Threshold	V_{IL}	V_{IN} = 6V to 60V, T_J = -40℃ to +125℃			1.1	V
Feedback						
Feedback Reference Voltage	V_{REF}	T_J = +25℃	0.561	0.575	0.589	V
		T_J = -40℃ to +125℃	0.558	0.575	0.592	
FB Input Current	I_{FB}	V_{FB} = 3.3V	-50		50	nA
Power Stage						
High-side MOSFET On-Resistance	R_{DSON_HS}	I_{SW} = 200mA		100		mΩ
Low-side MOSFET On-Resistance	R_{DSON_LS}	I_{SW} = 200mA		75		mΩ
Current Limit						
High-side Current Limit	I_{LIM_HS}	Maximum inductor peak current		4.5		A
Low-side Current Limit	I_{LIM_LS}	Maximum inductor valley current		1.5		A
Input Under-Voltage Lockout						
Input UVLO Rising Threshold	V_{UVLO}	V_{IN} rising	4.5	5	5.4	V
Input UVLO Hysteresis	V_{UVLO_HYS}			0.7		V
Oscillator						
Switching Frequency	f_S	V_{IN} = 24V, V_{OUT} = 5V		300		kHz
Timing Requirements						
Minimum On-Time	t_{ON}			120		ns
Minimum Off-Time	t_{OFF}			200		ns
Soft-Start Time	t_{SS}			1		ms
Over-Temperature Protection						
Thermal Shutdown	T_{SD}	Junction temperature rising		160		℃
Thermal Shutdown Hysteresis	T_{HYS}	Junction temperature falling		30		℃

TYPICAL PERFORMANCE CHARACTERISTICS

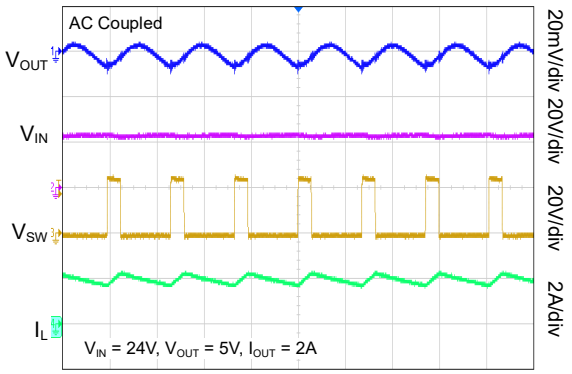
T_A = +25℃, V_{IN} = 24V, L = 22μH and C_{OUT} = 2×47μF, unless otherwise noted.

Output Voltage Ripple



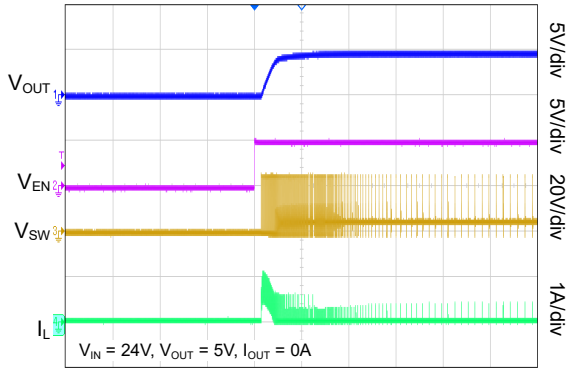
Time (200μs/div)

Output Voltage Ripple



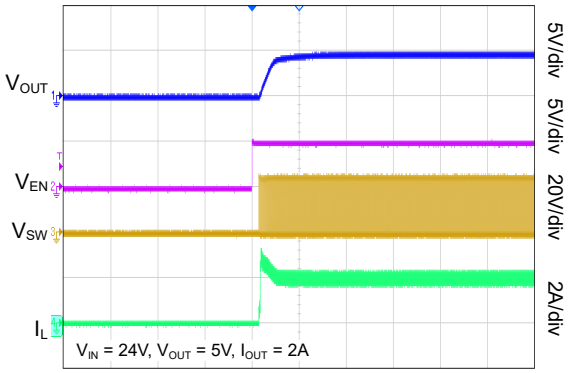
Time (2μs/div)

Startup through Enable



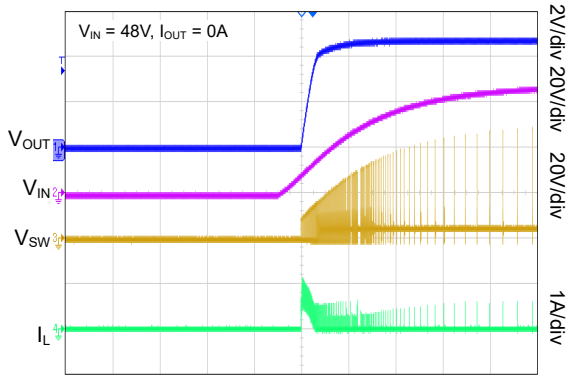
Time (2ms/div)

Startup through Enable



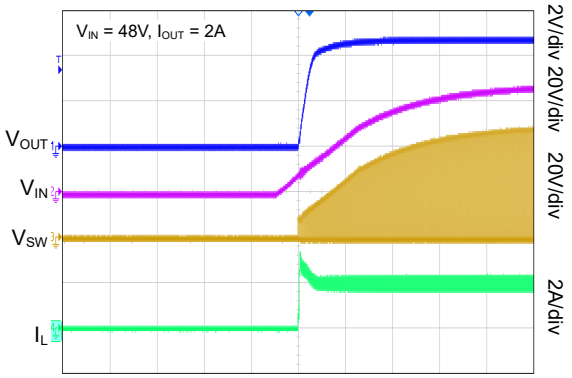
Time (2ms/div)

Startup through V_{IN}



Time (2ms/div)

Startup through V_{IN}

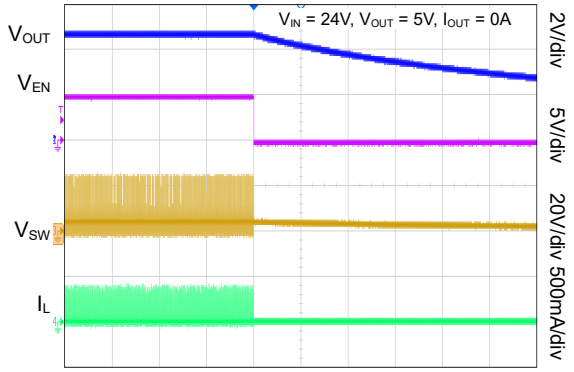


Time (2ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

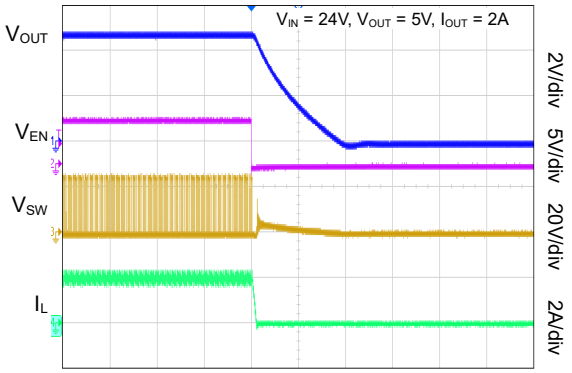
T_A = +25℃, V_{IN} = 24V, L = 22μH and C_{OUT} = 2×47μF, unless otherwise noted.

Shutdown through Enable



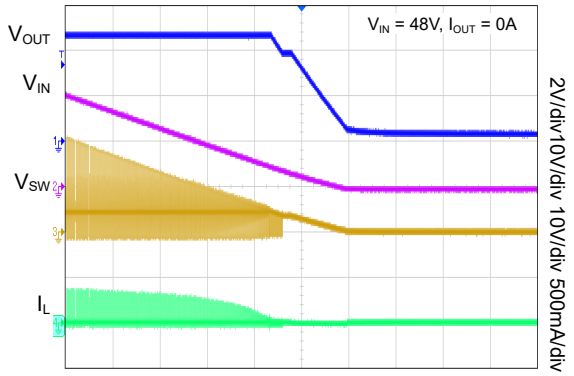
Time (500ms/div)

Shutdown through Enable



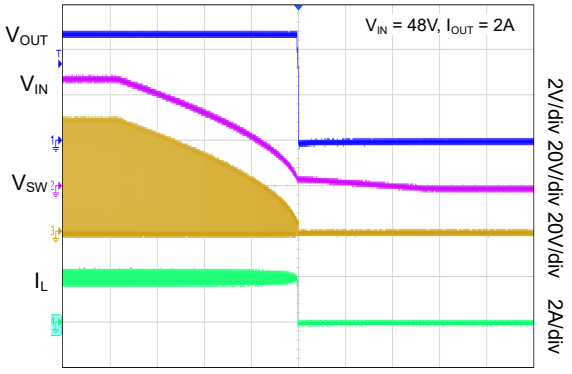
Time (100μs/div)

Shutdown through V_{IN}



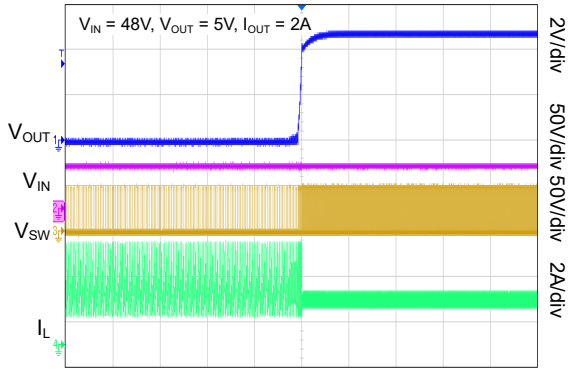
Time (20ms/div)

Shutdown through V_{IN}



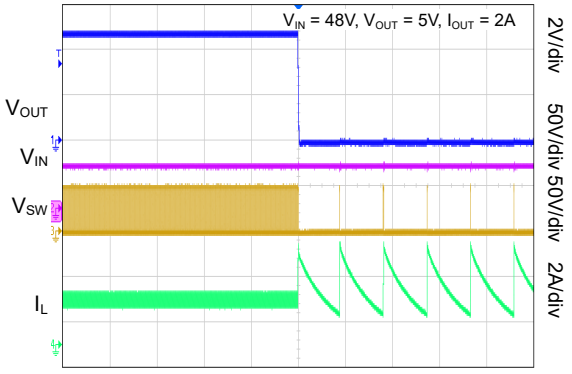
Time (10ms/div)

Short-Circuit Recovery



Time (5ms/div)

Short-Circuit Entry

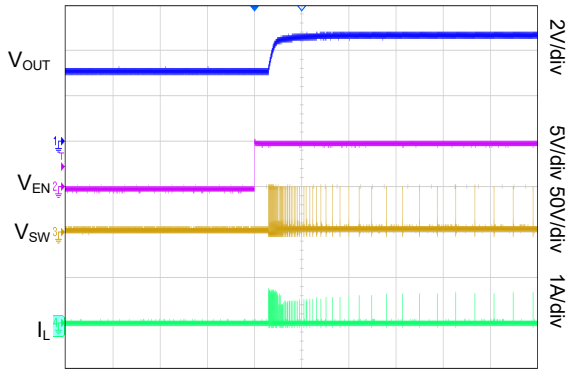


Time (100μs/div)

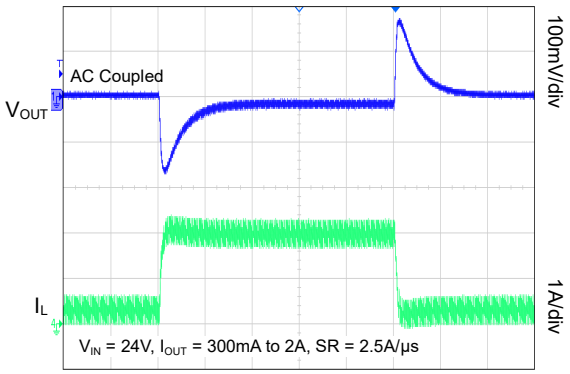
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 24V, L = 22μH and C_{OUT} = 2×47μF, unless otherwise noted.

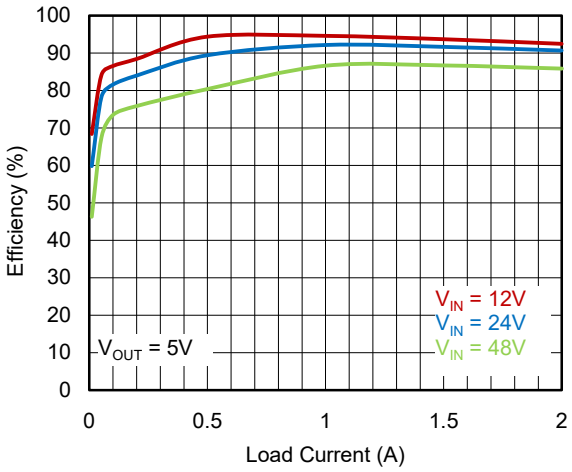
Pre-biased Startup



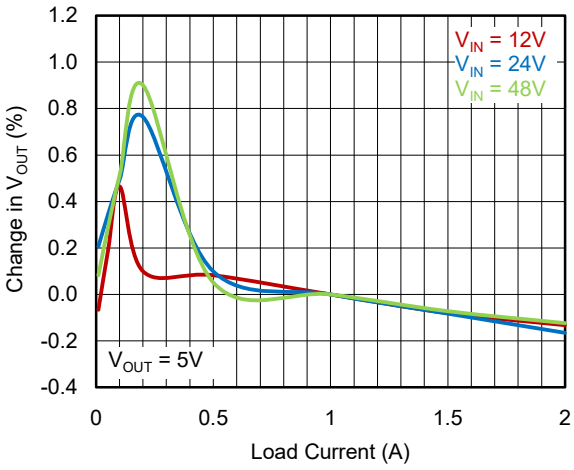
Load Transient Response



Efficiency vs. Load Current



Load Regulation



FUNCTIONAL BLOCK DIAGRAM

Figure 2 shows the block diagram of the SGM61720 synchronous step-down converter with the integrated low R_{DSON} N-channel MOSFET switches.

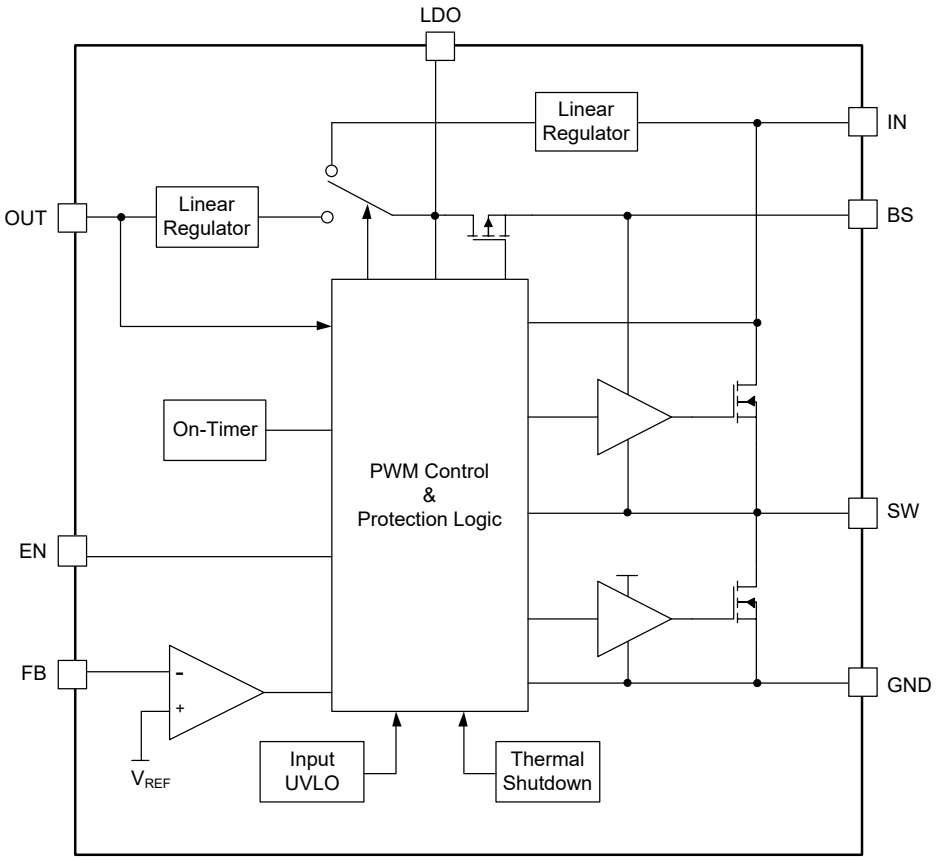


Figure 2. Block Diagram

NOTE: The OUT is a power input pin that is connected to V_{OUT}.

DETAILED DESCRIPTION

Overview

The SGM61720 is a high input voltage synchronous buck regulator with constant on-time control (COT) of high step-down conversion ratios. This device provides superior line and load regulations, cycle-by-cycle current limit, fast transient response and pre-biased startup capability, all with a simple passive compensation network. An internal precision reference voltage and a fixed soft-start timer are included. Several protection features such as input under-voltage lockout, output over-voltage protection, short-circuit, cycle-by- cycle over-current protection, and thermal shutdown are integrated to ensure safe operation.

Constant On-Time Control

In conventional voltage mode control (VMC) or current mode control (CMC) converters, a fixed frequency clock timing signal generates a sawtooth ramp that is compared with the compensation network output to adjust the PWM duty cycle (on-time) as control variable and regulate the output voltage. The compensator uses the voltage and/or current feedback(s) to govern the control variable and keep the output regulated with fast reaction to load or V_{IN} variations. The existence of the compensator in VMC or CMC converter inherently introduces some delay in the loop response. Unlike VMC or CMC, the constant on-time (COT) control is a hysteretic mode control without any clock signal or compensation amplifier. Each switching cycle is started

DETAILED DESCRIPTION (continued)

with a constant on-time pulse when an internal comparator senses that the output voltage is fallen below the desired output voltage. Output voltage is sensed by the feedback (FB) pin through an output resistor divider and is compared to the internal reference voltage (V_{REF}) with a low gain error amplifier. The amplifier output is sent to a comparator and when the feedback voltage (V_{FB}) falls below V_{REF}, the comparator triggers the on-time control logic that turns on the high-side switch. The on-time (t_{ON}) is determined by V_{IN} as approximated by Equation 1:

$$t_{ON}\ (\mu s) = 96 \times \frac{0.158\ (M\Omega)}{V_{IN} - 0.4} + t_{DELAY} \quad (1)$$

where t_{DELAY} is almost 50ns (0.05μs). For higher V_{IN} values, the -0.4V term can be ignored.

At the end of the on-time, the high-side MOSFET is turned off and after a very short dead-time the low-side MOSFET is turned on. The dead-time is implemented in the drivers to prevent shoot-through. The off-time continues until the V_{FB} falls below V_{REF} threshold again and ripple comparator triggers a new on-time pulse. Each cycle starts when the V_{FB} falls below V_{REF}. The controller does not allow the off-time to be shorter than 200ns (MIN) to ensure enough charge is received by the bootstrap capacitor for powering the high-side driver and also to provide sufficient time for the current sensing circuit in the low-side switch to measure current. The short blanking time is required to avoid switching transition noise that may interfere with the current measurement.

Figure 3 shows the basic timings of the COT converter when it is operating in continuous conduction mode (CCM) in which the inductor current stays above zero during the whole switching cycle. With light load, the inductor current reaches zero that will be discussed later. During the on-time, the inductor current has a rising slope and during the off-time it will be decreasing. The next on-time pulse starts when the V_{FB} falls below V_{REF} threshold. The required V_{FB} ripple (peak-to-peak) range for proper detection by ripple amplifier and comparator for stable PWM operation is roughly between 30mV to 200mV. Note that based on the operating principle of the COT converter, the ripple has to be in phase with the inductor ripple for stable operation, that is, when the inductor current is at its valley and the on-time needs to be started, the V_{FB} voltage should also be at the lowest to trigger the comparator and start the on-pulse in the right time. If there is a considerable phase delay in the ripple, the on-pulses start at the wrong times and COT pulse timing will not be stable (unstable frequency). With low ESR capacitors, lack of proper ripple phase or magnitude may occur, and cause stability issues as will be discussed later.

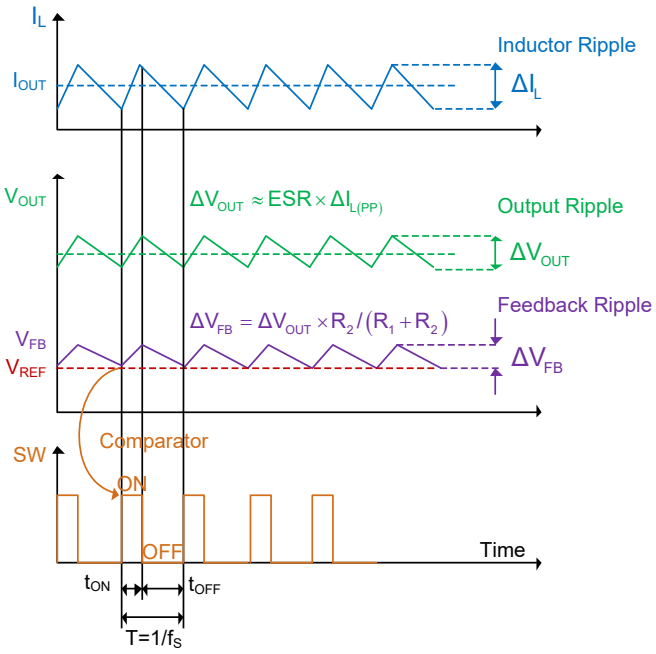


Figure 3. Basic Constant On-Time Control (The V_{OUT} capacitive ripple ($\Delta I_L/8f_SC$) is ignored.)

DETAILED DESCRIPTION (continued)

A Deeper Look into the Ripple

In COT control, the sensed ripple valleys determine the switching cycle timing, therefore the ripple must be clean from high frequency noise and appear with proper magnitude and phase on the FB pin (with respect to inductor current ripple) for stable operation. A real output capacitor has a parasitic ESR (equivalent series resistance) that results in two main components in the output voltage ripple (ΔV_{OUT}). Almost all inductor current ripple (AC component or ΔI_L) passes through the output capacitor while the DC current (I_L) goes to the load. The AC current multiplied by the ESR of the capacitor produces the ESR component of the voltage ripple (V_{rr} = ESR × ΔI_L) that is clearly in phase with the inductor ripple. However, the capacitive ripple component is due to the AC voltage variation of the capacitor which is caused by the charge and discharge with the inductor AC current. For the component (harmonic) of the inductor current, the capacitive ripple is almost ($V_{cr} \approx \Delta I_L/8f_SC$) which is 90° lag compared to the resistive ripple (V_{rr}) component.

The actual ripple includes higher order switching harmonics, but the main harmonic (at f_S) is usually the dominant component and by ignoring the higher order components, the overall phase lag of the output voltage ripple is estimated by the relative magnitudes of resistive (ESR) and capacitive ripple components (ESR and $|Z_C| = 1/2\pi f_S C$). The phase lag is given by $\tan^{-1}((2\pi f_S C \times ESR)^{-1})$. All lags and delays caused by the feedback network, parasitic elements of the FB path and the amplifier/comparator delays, should be considered for the evaluation of the actual feedback phase lag that affect the stability.

As an example, for a 100μF ceramic capacitor with ESR = 2mΩ and operating at f_S = 500kHz, the phase lag will be around 57° that is significant. However, for a 300μF capacitor with ESR = 10mΩ operating at 1MHz, the lag will be only 3°. Higher switching frequency may improve stability; however, significant phase lag may be introduced by the low gain amplifier and comparator at higher frequencies. Moreover, minimum on-time will limit the step-down ratio at higher frequencies, so a compromised frequency should to be considered. Higher output capacitance is usually implemented by paralleling more capacitors that inherently reduces the total effective ESR of the output capacitor due to parallel operation. While high ESR is not normally desired for better efficiency and higher RMS current handling (less heating) in the capacitors, it is generally preferred for stable COT operation. Therefore, a compromise is always needed for proper design of output capacitor to satisfy design requirements.

As ceramic capacitors are now commonly used for most applications, some ripple injection techniques are presented for stable operation of COT converters with low ESR capacitors as will be explained later.

Power Supply Select

The power for internal circuit is taken from V_{IN} when V_{OUT} is less than 5V, during power-up or when V_{OUT} setting is less than 5V. When V_{OUT} > 5V, the internal power supply will switch to the V_{OUT} to reduce losses.

Power-Save Mode

Considering power usage, the SGM61720 has three main operating modes: PWM mode, power-save mode and sleep mode. When the SGM61720 operates in continuous conduction mode (CCM) with heavy load, the device operates in PWM mode with an almost constant frequency. When it operates in discontinuous conduction mode (DCM) with light load, the SGM61720 goes into the power-save mode in which internal power dissipation is significantly reduced. Moreover, the operating frequency starts to drop depending on the load. At very light load and when the off-time exceeds 10μs, device goes to the sleep mode to lower internal dissipation.

The details are explained in Figure 4 that shows the timings of the COT control in DCM. Inductor current (I_L) is monitored with a zero-crossing detector and when I_L crosses the zero and goes slightly negative, both high-side and low-side MOSFETs are turned off (if V_{FB} > 0.575V). They will not turn on again until the V_{FB} falls below V_{REF} and triggers a new on-time pulse. During this off-time period, all non-essential circuits are shut down to minimize losses and the load is supplied by the output capacitor stored energy. The control circuitry wakes up when the new on-pulse is triggered. When the time between successive high-side pulses (t_1) is longer than 10μs, the device goes into sleep mode in which the system current dissipation is only about 90μA.

DETAILED DESCRIPTION (continued)

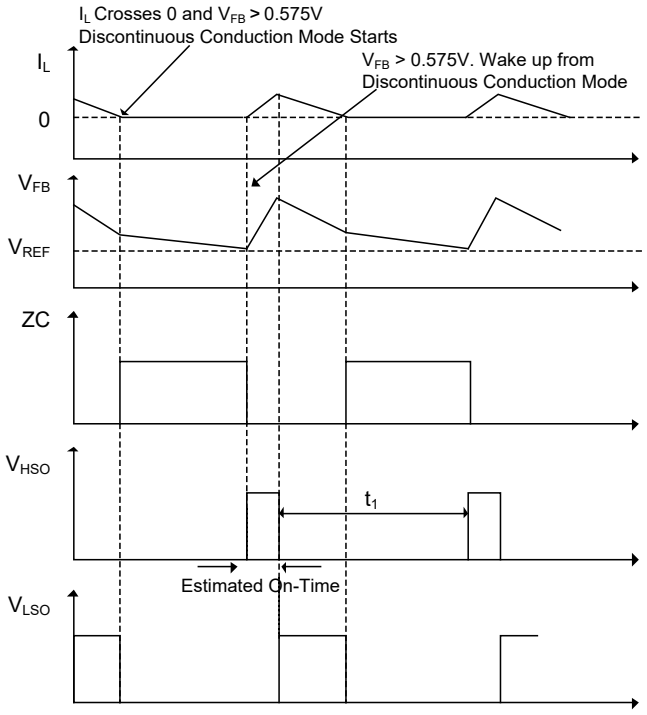


Figure 4. Power-Save Mode (DCM)

Reference Voltage

With the 0.575V internal precision reference voltage, it is possible to set the output voltage down to 0.575V. The accuracy of the internal reference is ±2.5% at +25℃ and ±3% across -40℃ to +125℃ junction temperature. A resistor divider between the output voltage, V_{OUT} (connected to the OUT input pin) and the FB pin, programs the output voltage as given in the Equation 2:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) \quad (2)$$

where R_1 and R_2 are the upper and lower resistors of the voltage divider between OUT and GND pins.

Current limit

When an over-current occurs on the output, it will be reflected on the SW node current. If the current in the high-side switch exceeds its limit (almost 4.5A), the high-side switch will automatically be turned off and after a short dead-time, the low-side switch will be turned on to take over the current in the inductor. If the low-side switch current falls below 1.5A the current will be considered normal and high-side switch will be turned on again.

Output Over-Voltage Protection (OVP)

If the sensed voltage on the FB pin exceeds 110% of the nominal value, it is considered an over-voltage event on the output (V_{OUT_OV}) and the device goes into the over-voltage protection status.

Upon occurrence of an OVP, switching stops and both high-side and low-side switches remain off. Due to the excellent sink and source capability of the synchronous output stage, in most cases, the error amplifier will be able to maintain output in regulation and bring voltage back to normal. Note that if the FB pin is disconnected or when the output is shorted to the V_{IN}, the error amplifier is not effective. However, if the FB pin is disconnected, a small internal current source will pull up the FB pin voltage and force the V_{OUT} to go down and disable the regulator, preventing catastrophic over voltage on the load. If a higher external voltage is accidently shorted to the converter output, an OVP event is triggered to protect the low-side switch. In any case, the regulator will automatically recover if the OVP fault is cleared.

Thermal Shutdown (TSD)

The SGM61720 monitors junction temperature and will stop PWM switching if it becomes too hot. If the junction temperature exceeds +160℃ (TYP), the device is forced to stop switching. It will recover automatically when T_J the junction temperature decreases by approximately 30℃.

Ripple Injection

The SGM61720 is a COT control device in which the PWM timing is based on the output voltage ripple feedback to the FB pin. As explained before, every time the V_{FB} voltage falls below V_{REF} threshold, the high-side switch is turned on and the inductor current starts to rise. High-side switch is kept on for a constant on-time which is determined by V_{IN} as explained in Equation 1. At the end of on-time, the high-side switch is turned off and after a very short dead-time, the low-side switch is turned on (off-time) and current in the inductor starts to decrease. The next on-time and current rise in the inductor start when the V_{FB} falls below V_{REF} threshold again. Therefore, in COT control the ripple initiates each cycle and there is no clock signal for switching.

DETAILED DESCRIPTION (continued)

The required V_{FB} peak-to-peak ripple range for stable PWM operation is between 30mV to 200mV. At high output voltage applications (typically V_{OUT} > 5V), the natural output ripple is usually large enough for proper PWM operation because the output filter is usually designed such that the output ripple magnitude is roughly 1% to 2% of the output voltage. However, in some design conditions like low output voltage applications, such as a 1V, the output voltage ripple is usually low (e.g. 10mV) and it will not be possible to get enough in phase ripple on the FB pin without a new strategy.

In fact, the ripple feedback is even lower than output ripple due to the voltage divider. If the FB ripple is small, the internal amplifier and comparator are not able to sense that and the control will be lost. In such condition, the output voltage is either not regulated or has large ripple due to missing or wrong multiple pulses. With the low ESR output capacitors such as ceramic ones, the ripple is also small. Therefore ripple injection methods are proposed for low output ripple applications to avoid instability.

Remember that naturally, the output ripple (ΔV_{OUT}) has two main components. One is in phase with inductor ripple and is produced by the inductor AC current going through the output capacitors (V_{rr} = ESR × ΔI_L), and the other one that has a lag phase is due to the charge and discharge of capacitor by ΔI_L current in each cycle (estimated by $V_{cr} \approx \Delta I_L/8f_sC$). The output capacitor C is usually designed large enough to filter switching ripples such that ΔV_{OUT} and output peak transients in response to load changes, remain within the acceptable range in the application. Too large output capacitor may result in startup issues.

Three main cases can be classified based on the amount of peak-to-peak feedback ripple (ΔV_{FB}) and the ripple injection technique used for COT converters.

Case1: If the output capacitor has large ESR, the output ripple at the FB pin is mainly due to the ESR that carries the inductor current ripple (see Figure 5). If the output voltage is small (R_2 is large compared to R_1) the ripples seen by FB pin are large enough and with proper phase. In this case converter has a stable operation without any ripple injection. The stability criterion is:

$$t_{ON} < 2 \times ESR \times C_{OUT} \quad (3)$$

The feedback voltage ripple is given by Equation 4:

$$\Delta V_{FB} \approx \frac{R_2}{R_1 + R_2} \times ESR \times \Delta I_L \quad (4)$$

where:

ΔI_L = peak-to-peak value of the inductor current ripple.

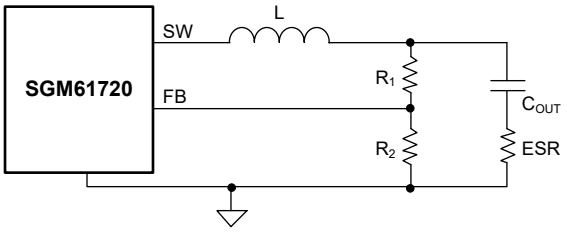


Figure 5. Feedback Circuit when Enough Ripple at FB Pin

Case 2: In this case, the in-phase ripple of the output is large enough, but it is weakened by the resistor divider (R_2 is large compared to R_1). As shown in Figure 6, a small feed-forward capacitor (C_{FF}), across the upper resistor (R_1) bypasses the resistor divider at the ripple frequency (f_S) and the ripple seen on the FB pin is essentially the same as the output voltage ripple (not weakened by the divider). The other advantage of using C_{FF} is the improvement of the converter transient response, because feeding back the actual over/under-voltage transients of the output with no weakening helps a quicker reaction and faster response to transients. In fact, it is sometimes used for applications like Case 1 for better transient response. However, the drawback of C_{FF} is that it may worsen the regulation of the converter output. Typically, the C_{FF} value is chosen between 1nF and 100nF (the impedance is typically a few ohms to a few hundred ohms).

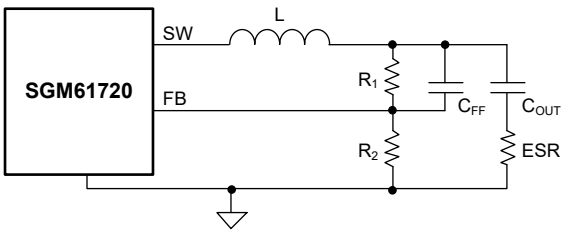


Figure 6. Use of Feed-Forward Capacitor when Inadequate Ripple at FB Pin

DETAILED DESCRIPTION (continued)

With the feed-forward capacitor, the feedback voltage ripple is very close to the output voltage ripple.

$$\Delta V_{FB} \approx ESR \times \Delta I_L \quad (5)$$

It is generally recommended to choose smaller values for R_1 and R_2. Also, the time constant seen by C_{FF} should be much longer than switching period, that is $((R_1||R_2) \times C_{FF} \gg \frac{1}{f_S})$.

Case 3: In modern designs, ceramic capacitors are extensively used due to their small size and good stability. Due to very low ESR of the output capacitors, there is virtually no ripple at the FB pin. This is usually more critical at low output voltage in which lower output ripple is required (typically less than 20mV). Therefore, additional ripple (in phase with inductor current) needs to be injected artificially into the FB pin to keep stable switching. The additional ripple can be injected from the switching SW node by a series resistor (R_{INJ}) and capacitor (C_{INJ}), as shown in Figure 7.

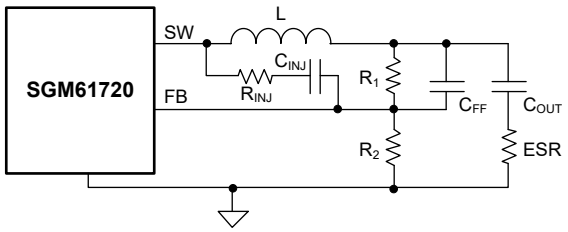


Figure 7. Ripple Injection from SW Pin

Note that if too much ripple is injected, the transient response will get worse, because the impact of the actual output variations on the feedback signal is reduced. The key point is that the ripple should be kept as small as possible without losing the stability. It is recommended to keep ΔV_{FB} between 30mV to 200mV.

The process of sizing the ripple injection resistor and capacitors in Figure 7 is as follows:

• Select C_{FF} to feed all output ripples into the feedback pin. The impedance of C_{FF} should be small compared to the feedback divider impedance at the desired switching frequency. The impedance of the feedback network is the parallel combination of R1||R2. The impedance of C_{FF} at the switching frequency can be taken to be about one tenth of this value.

$$C_{FF} = \frac{10 \times (R_1+R_2)}{2\pi f_S R_1 R_2} \quad (6)$$

• Select R_{INJ}. When SW voltage is equal to V_{IN}, the current injected in the feed-forward capacitor C_{FF} is calculated as $(V_{IN}-V_{OUT})/R_{INJ}$, neglecting the DC resistance of inductor and the small amount of current flowing through R_1 and R_2. Given an injected voltage ripple ΔV_{FB} into the feedback node, R_{INJ} can be calculated as:

$$R_{INJ} = \frac{t_{ON}}{C_{FF}} \times \frac{V_{IN} - V_{OUT}}{\Delta V_{FB}} \quad (7)$$

• Select C_{INJ} as DC blocking capacitor which should be 3 to 4 times larger than the C_{FF}.

$$C_{INJ} = 4 \times C_{FF} \quad (8)$$

APPLICATION INFORMATION

Setting the Output Voltage

The output voltage of the regulator is determined by an external resistor divider from the output node to the FB pin as shown in Figure 8. It is recommended to use resistors with 1% tolerance or better because it directly affects the output accuracy. The recommended range for selection of R_1 is between 10kΩ to 100kΩ. Note that the R_1 value larger than 400kΩ is not recommended, because it makes the feedback path more susceptible to noise. To avoid the noise too large to disturb the V_{FB}, the R_2 must less than 50kΩ.

$$V_{OUT} = 0.575 \times \left(1 + \frac{R_1}{R_2}\right) \quad (9)$$

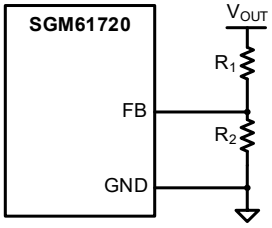


Figure 8. Setting the Output Voltage

Output Inductor (L)

Four parameters of the inductor should be considered in the design: nominal inductance value, DC resistance, saturation current and maximum RMS current.

A good compromise among size, loss, and cost is to set the inductor ripple current to be equal to 40% of the maximum output current.

$$L = \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{0.4 \times I_{OUT(MAX)} \times f_S \times V_{IN(MAX)}} \quad (10)$$

The peak inductor current is equal to the average output current plus one half of the peak-to-peak inductor current ripple.

$$I_{L(PK)} = I_{OUT(MAX)} + 0.5 \times \Delta I_{L(PP)} \quad (11)$$

The input and output voltages and the inductance of the inductor determine the peak-to-peak inductor current ripple (given by Equation 12).

$$\Delta I_{L(PP)} = \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{L \times f_S \times V_{IN(MAX)}} \quad (12)$$

where:

$\Delta I_{L(PP)}$ = peak-to-peak inductor current ripple.

f_S = switching frequency.

Larger peak-to-peak current ripple increases the power dissipation in the inductor and MOSFETs. Larger output current ripple also requires more output capacitance to smooth out the larger current ripple. Smaller peak-to-peak current ripple requires a larger inductance value and therefore a larger and more expensive inductor.

Output Capacitors

The output capacitors and inductor filter the AC part of the PWM switching voltage and provide an acceptable level of output voltage ripple superimposed on the desired output DC voltage. Capacitors also store energy to help maintaining of the output voltage regulation during a load transient. The output voltage ripple (ΔV_{OUT}) depends on the output capacitor value at the operating voltage and temperature (℃) and its parasitics (ESR and ESL):

$$\Delta V_{OUT} = \Delta I_L \times ESR + \frac{V_{IN} - V_{OUT}}{L} \times ESL + \frac{\Delta I_L}{8 f_S C} \quad (13)$$

The voltage rating of the output capacitors should be selected with enough margins to ensure that capacitance drop (voltage and temperature derating) is not significant. The type of output capacitors will determine which terms of Equation 13 are dominant. For ceramic output capacitors, the ESR and ESL are virtually zero so the output voltage ripple will be dominated by the capacitive term.

$$\Delta V_{OUT} \approx \frac{\Delta I_L}{8 f_S C} \quad (14)$$

To reduce the voltage ripple either switching frequency or the total capacitance is increased. Inductance may also be increased to reduce the inductor current ripple. For electrolytic output capacitors, the value of capacitance is relatively high, and the third term in Equation 15 can be ignored compared to the ESR and ESL terms:

$$\Delta V_{OUT} = \Delta I_L \times ESR + \frac{V_{IN} - V_{OUT}}{L} \times ESL \quad (15)$$

APPLICATION INFORMATION (continued)

Higher quality capacitors, larger inductance or using parallel capacitors can help reduce the output ripple in a design using electrolytic output capacitors. The ESR of some commercial electrolytic capacitors can be quite high, and it is recommended to use quality capacitors with the ESR or the total impedance clearly documented in their datasheet. ESR of an electrolytic capacitor may increase significantly at cold ambient temperatures with a factor of 10 or so, which increases the ripple and can deteriorate the regulator stability.

The transient response of the regulator also depends on the quantity and type of output capacitors. In general, reducing the ESR of the output capacitance will result in a better transient response. The ESR can be minimized by simply adding more capacitors in parallel or by using higher quality capacitors. When a fast load transient of magnitude ΔI and rate of di/dt occurs, the output voltage will jump or dip by a transient magnitude of ΔV_{OUT}:

$$\Delta V_{OUT} = \Delta I \times ESR + \frac{di}{dt} \times ESL \quad (16)$$

Right after the transient, the inductor current remains almost constant especially for larger inductors and the transient current is carried by the capacitor. The output voltage will deviate from its nominal value for a short time depending on the system bandwidth, the inductor and the output capacitance. Eventually, the error amplifier and feedback bring the output voltage back to its nominal value. A higher bandwidth is usually preferred to get shorter settling time; however, it may be more difficult to get acceptable gain and phase margins.

Input Capacitors

Four parameters of the input capacitors should be considered in the design: capacitance value, ESR, current rating and voltage rating. The capacitance value should be large enough and ESR must be small enough to limit the input voltage ripples much less than the hysteresis of the input for UVLO (V_{UVLO_HYS}). This value is nominally 700mV for the SGM61720. The worst case occurs at full load and minimum input voltage. The C_{IN} voltage rating should have adequate design margin to handle the highest expected input surge voltage. Also, the capacitance drop (derating) at maximum operating voltage and the worst ambient temperature must be considered for the design. Finally, the capacitor RMS current rating must be higher than the expected RMS input current to the regulator with the temperature derating considerations. Note that the input current has two main AC components that both should circulate in the input capacitor and only the DC component of regulator input must be taken from the source. The AC current in the input capacitor includes a high frequency component caused by switching transients (due to the hard switching and gate driving) and a main AC component caused by the inductor ripple at the switching frequency. To decouple these two currents, typically the two capacitor types should be paralleled. Small low-ESR ceramic capacitor is used right beside the IN and GND pins of the regulator to carry the high frequency switching transients (ringings) and larger capacitor is paralleled to carry the inductor ripple and load transient currents to minimize the input voltage ripple. The input capacitors must deliver the RMS current according to:

$$I_{RMS} = I_O \sqrt{D \times (1 - D)} \quad (17)$$

where the duty cycle is $D \approx V_{OUT}/V_{IN}$. For example, at D = 20% duty cycle, the input/output current multiplier is 0.40. Therefore, if the regulator is delivering 3A of steady-state load current, the input capacitor(s) must support an RMS current of 1.2A (0.40 × 3A).

APPLICATION INFORMATION (continued)

The input capacitor(s) must limit the voltage deviations at the IN pin to something significantly less than the UVLO hysteresis during maximum load and minimum input voltage. Considering a conservative factor of 0.83 for frequency deviation, the minimum input capacitance can be calculated as follows:

$$C_{IN} > 1.2 \times \frac{I_{OUT} \times D \times (1-D)}{f_S \times \Delta V_{IN(MIN)}} \quad (18)$$

where $\Delta V_{IN(MIN)}$ is chosen to be much less than the hysteresis of the V_{IN} UVLO comparator ($\Delta V_{IN(MIN)} \leq$ 150mV is recommended), and f_S is the nominal PWM frequency. The D × (1 - D) term in Equation 18 has an absolute maximum value of 0.25 at 50% duty cycle. So, for example, a very conservative design based on I_{OUT} = 2A, and V_{OUT} =5V (f_S = 316kHz), D × (1 - D) = 0.25, and ΔV_{IN} = 150mV.

$$C_{IN} \geq 1.2 \times \frac{2A \times 0.25}{316kHz \times 150mV} = 12.7\mu F \quad (19)$$

As discussed before, DC bias effect (voltage derating) on the ceramic capacitors needs to be considered. The capacitance drop with voltage is huge with the Y5V and Z5U temperature characteristic ceramic capacitors (as much as 90% reduction) and these types should be avoided. The X5R and X7R type capacitors are the primary choices due to their stability against DC bias and temperature. The DC bias drop effect is larger for smaller physical capacitor sizes, however, the self-resonance frequency of larger package capacitors is typically lower, so a compromise is needed. Self-resonance frequency of the capacitor should be higher than the expected operating frequency range of the capacitor. Beyond the resonant, the impedance of the capacitor will be more inductive rather than capacitive. Self-resonance of the HF decoupling input capacitors must be higher than the converter switching noise and ringing frequency. It can be several times higher than switching frequency.

LAYOUT GUIDE

The PCB layout is quite important in the power supply design. An incorrect layout could cause many problems, such as instability, load and line transient regulation problems, output voltage noise, and EMI issues. Good grounding becomes important, especially with heavy load current.

The following PCB layout guide should be applied:
1. Use short, wide and direct traces for high-current connections (IN, SW and GND).
2. Traces of switching node (SW) should be short and away from feedback network traces.
3. Keep the BS voltage path as short as possible.
4. Place decoupling capacitors close to the IN and GND pins.
5. If a bulk capacitor is used at output, add an additional 1μF ceramic capacitor or larger value as close as possible to the OUT and GND pins.
6. Decoupling capacitors should be as close as possible to the LDO and GND pins.
7. Place the feedback resistors as close as possible to the FB pin that is sensitive to noise.

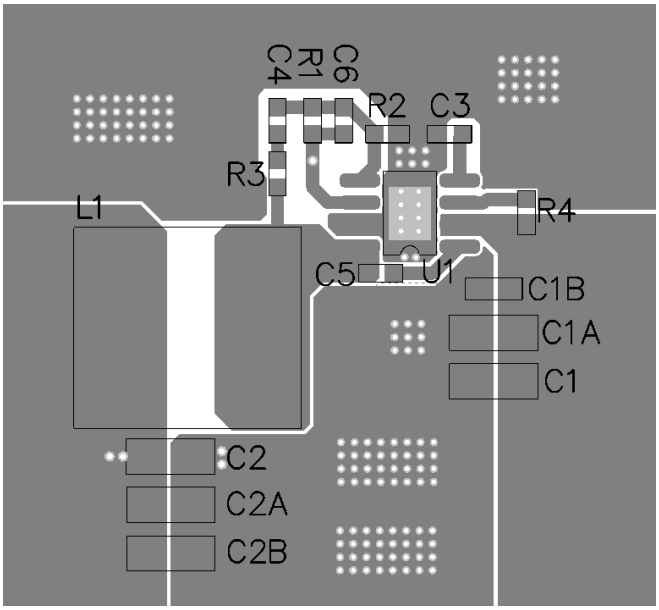


Figure 9. Top Layer

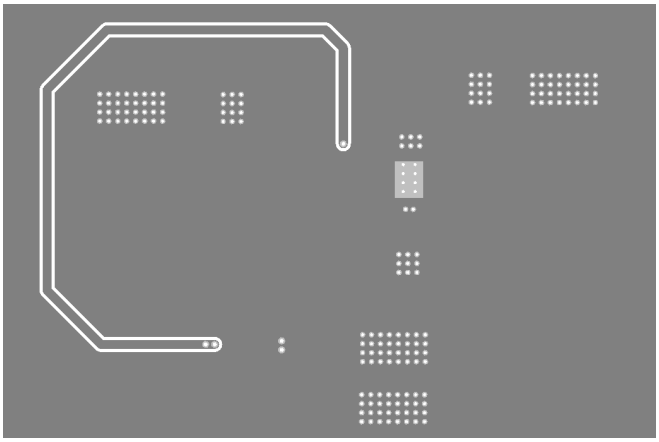


Figure 10. Bottom Layer

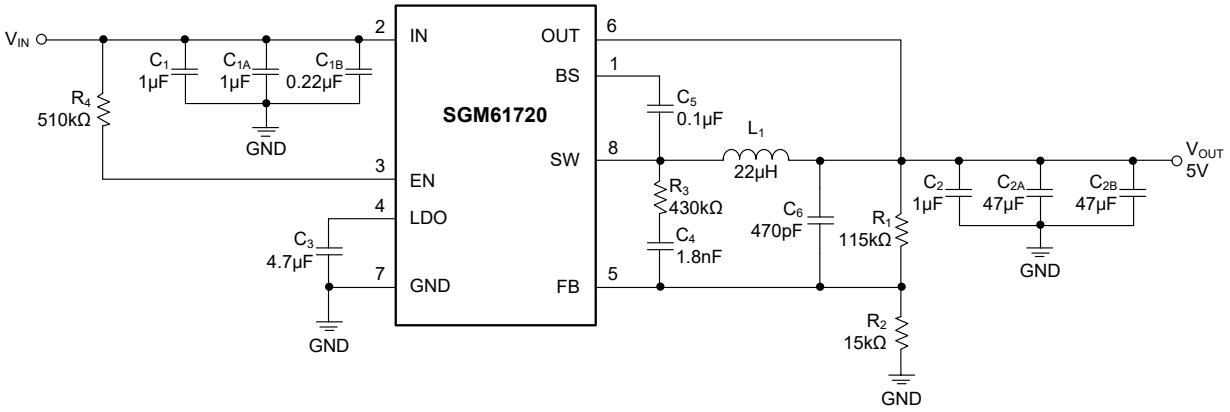


Figure 11. Typical Application Circuit

REVISION HISTORY

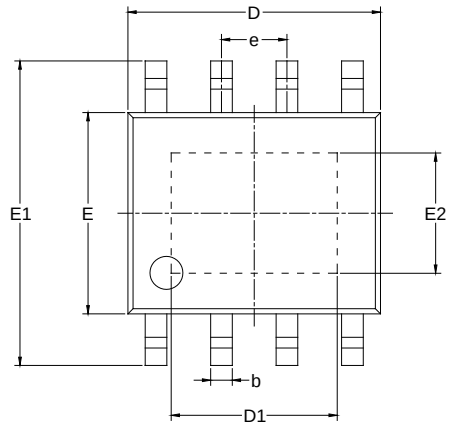
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

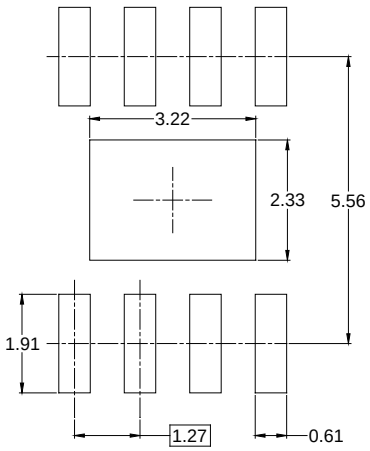
JUNE 2021 – REV.A to REV.A.1	Page
Changed operating ambient temperature to operating junction temperature in General Description	1

Changes from Original (DECEMBER 2020) to REV.A	Page
Changed from product preview to production data	All

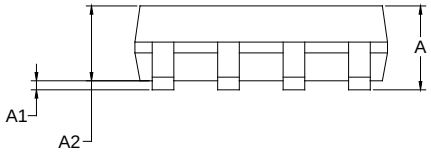
PACKAGE OUTLINE DIMENSIONS

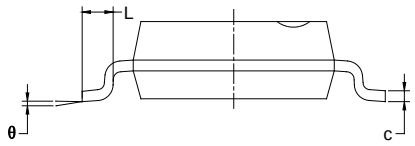
SOIC-8 (Exposed Pad)





RECOMMENDED LAND PATTERN (Unit: mm)





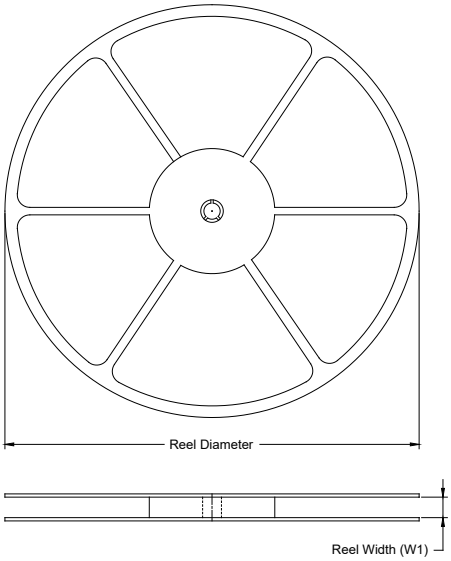
Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A			1.700
A1	0.000	-	0.150
A2	1.250	-	1.650
b	0.330	-	0.510
c	0.170	-	0.250
D	4.700	-	5.100
D1	3.020	-	3.420
E	3.800	-	4.000
E1	5.800	-	6.200
E2	2.130	-	2.530
e	1.27 BSC		
L	0.400	-	1.270
θ	0°	-	8°

NOTES:

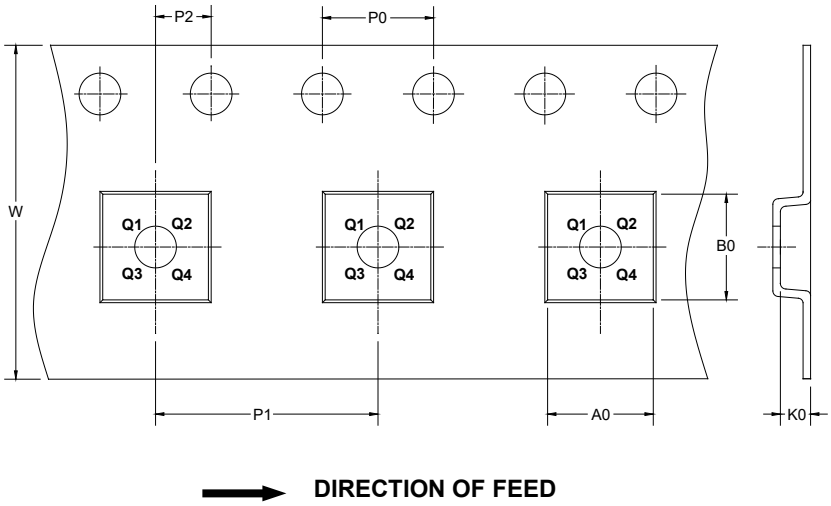
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



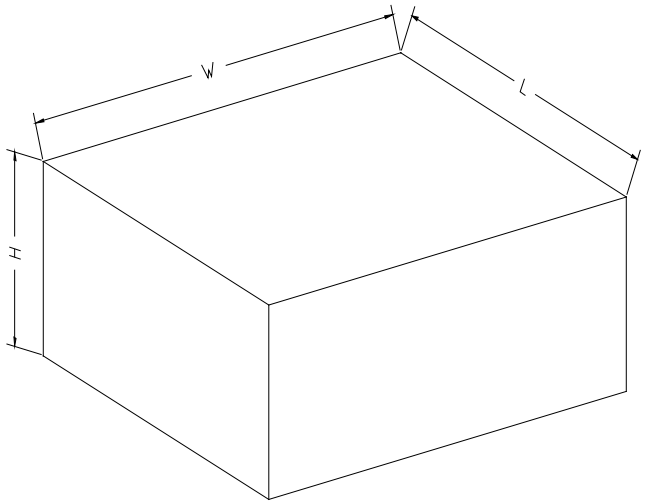
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-8 (Exposed Pad)	13″	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002