TPS22976 5.7-V, 6-A, 14-mΩ On-Resistance Dual-Channel Load Switch

1 Features

- Integrated dual-channel load switch
- Input voltage range: 0.6 V to V_{BIAS}
- V_{BIAS} voltage range: 2.5 V to 5.7 V
- On-resistance
  - R_{ON} = 14 mΩ (typical) at V_{IN} = 0.6 V to 5 V, V_{BIAS} = 5 V
  - R_{ON} = 18 mΩ (typical) at V_{IN} = 0.6 V to 2.5 V, V_{BIAS} = 2.5 V
- 6-A maximum continuous switch current per channel
- Quiescent current for TPS22976, TPS22976N
  - 37 µA (typical, both channels) at V_{IN} = V_{BIAS} = 5 V
  - 35 µA (typical, single channel) at V_{IN} = V_{BIAS} = 5 V
- Quiescent current for TPS22976A
  - 85 µA (typical, both channels) at V_{IN} = V_{BIAS} = 5 V
  - 83 µA (typical, single channel) at V_{IN} = V_{BIAS} = 5 V
- Control input threshold enables use of 1.2-, 1.8-, 2.5-, and 3.3-V logic
- Configurable rise time
- Fast turn ON time (TPS22976A)
  - t_{ON} = 17µs at V_{IN} = 1.05V
- Thermal shutdown
- Quick Output Discharge (QOD) (optional)
- SON 14-pin package with thermal pad
- ESD performance tested per JESD 22
  - 2-kV HBM and 1-kV CDM

2 Applications

- Ultrabook™
- Notebooks and Netbooks
- Tablet PCs
- Set-top Boxes and Residential Gateways
- Telecom Systems
- Solid-State Drives (SSD)

3 Description

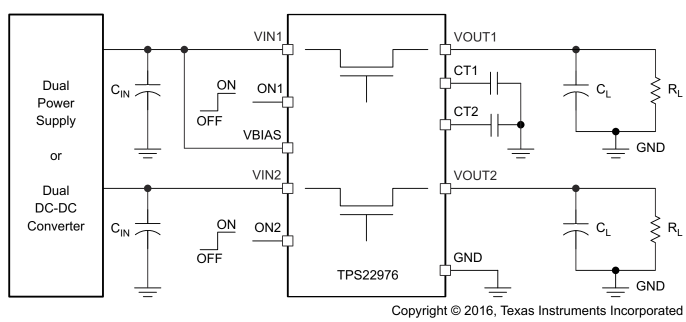
The TPS22976 product family consists of three devices: TPS22976, TPS22976A and TPS22976N. Each device is a dual-channel load switch with controlled turnon. The device contains two N-channel MOSFETs that can operate over an input voltage range of 0.6 V to 5.7 V, and can support a maximum continuous current of 6 A per channel. Each switch is independently controlled by an on and off input (ON1 and ON2), which can interface directly with low-voltage control signals. The TPS22976 is capable of thermal shutdown when the junction temperature is above the threshold, turning the switch off. The switch turns on again when the junction temperature stabilizes to a safe range. The TPS22976 also offers an optional integrated 230-Ω on-chip load resistor for quick output discharge when the switch is turned off.

The TPS22976 is available in a small, space-saving 3-mm × 2-mm 14-SON package (DPU) with integrated thermal pad allowing for high power dissipation. The device is characterized for operation over the free-air temperature range of –40°C to 105°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS22976 TPS22976A TPS22976N	WSON (14)	3.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Application Circuit

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4 Revision History

Changes from Revision B (September 2017) to Revision C (September 2020)	Page
• Added quiescent current and rise time for TPS22976A in the *Features* list	1
• Added TPS22976A to the *Device Information* table	1
• Added *Switching Characteristics (TPS22976A)* table	4
• Added a line for quiescent current for TPS22976A in all of the *Specifications* tables	4
• Added two quiescent current graphs in *Typical DC Characteristics* for the TPS22976A	9
• Added section for the TPS22976A in *Typical AC Characteristics*	12
• Added CT pin equation for the TPS22976A in *Adjustable Rise Time* section	25

Changes from Revision A (March 2017) to Revision B (September 2017)	Page
• Updated V_{IH} in *Recommended Operating Conditions*	4

Changes from Revision * (February 2016) to Revision A (March 2017)	Page
• Updated statement for Equation 4 in *Adjustable Rise Time* section from "CT = 0 pF" to "CT < 100 pF"	25

5 Device Comparison Table

DEVICE	R_{ON} AT $V_{IN} = V_{BIAS}$ = 5 V (TYPICAL)	QUICK OUTPUT DISCHARGE	MAXIMUM OUTPUT CURRENT	TURN ON TIME <65µs AT V_{IN} = 1.05V
TPS22976	14 mΩ	Yes	6 A	No
TPS22976A	14 mΩ	Yes	6 A	Yes
TPS22976N	14 mΩ	No	6 A	No

6 Pin Configuration and Functions

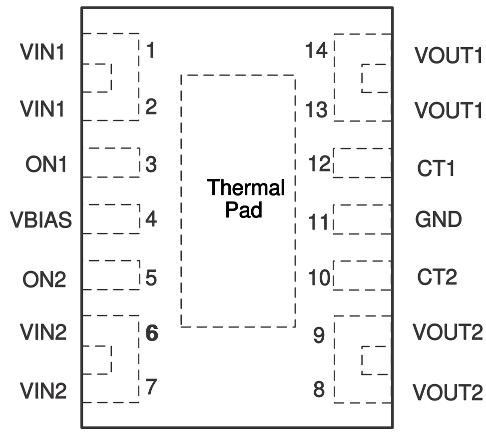


Figure 6-1. DPU Package 14-Pin WSON with Exposed Thermal Pad Top View

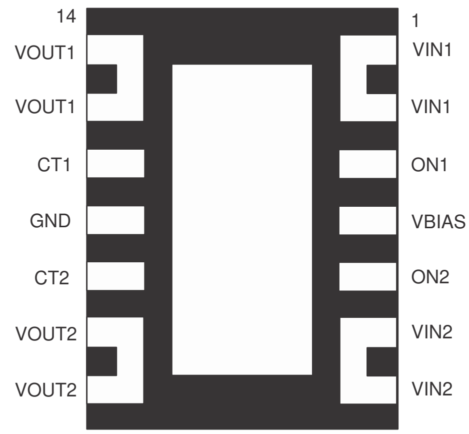


Figure 6-2. DPU Package 14-Pin WSON with Exposed Thermal Pad Bottom View

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1, 2	VIN1	I	Switch 1 input. Recommended voltage range for these pins for optimal R_{ON} performance is 0.6 V to V_{BIAS}. Place an optional decoupling capacitor between these pins and GND to reduce V_{IN1} dip during turnon of the channel. See the *Application Information* section for more information.
3	ON1	I	Active-high switch 1 control input. Do not leave floating.
4	VBIAS	I	Bias voltage. Power supply to the device. Recommended voltage range for this pin is 2.5 V to 5.7 V. See the *Application Information* section.
5	ON2	I	Active-high switch 2 control input. Do not leave floating.
6, 7	VIN2	I	Switch 2 input. Recommended voltage range for these pins for optimal R_{ON} performance is 0.6 V to V_{BIAS}. Place an optional decoupling capacitor between these pins and GND to reduce V_{IN2} dip during turn-on of the channel. See the *Application Information* section for more information.
8, 9	VOUT2	O	Switch 2 output.
10	CT2	O	Switch 2 slew rate control. Can be left floating. Capacitor used on this pin must be rated for a minimum of 25 V for desired rise time performance.
11	GND	—	Ground.
12	CT1	O	Switch 1 slew rate control. Can be left floating. Capacitor used on this pin must be rated for a minimum of 25 V for desired rise time performance.
13, 14	VOUT1	O	Switch 1 output.
—	Thermal pad	—	Thermal pad (exposed center pad) to alleviate thermal stress. Tie to GND. See the *Layout* section for layout guidelines.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
$V_{IN1,2}$	Input Voltage	–0.3	6	V
$V_{OUT1,2}$	Output Voltage	–0.3	6	V
$V_{ON1,2}$	ON Pin Voltage	–0.3	6	V
V_{BIAS}	Bias Voltage	–0.3	6	V
I_{MAX}	Maximum continuous current per channel		6	A
$I_{MAX,PLS}$	Maximum pulsed current switch per channel, pulse <300µs, 3% duty cycle		8	A
T_J	Junction temperature		125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[(2)]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{IN1,2}$	Input Voltage	0.6		V_{BIAS}	V
V_{BIAS}	Bias Voltage	2.5		5.7	V
$V_{ON1,2}$	ON Pin Voltage	0		5.7	V
$V_{OUT1,2}$	Output Voltage	0		V_{IN}	V
V_{IH}	High-Level Input Voltage, ON	1.2		5.7	V
V_{IL}	Low-Level Input Voltage, ON	0		0.5	V
T_A	Ambient Temperature	–40		105	°C

7.4 Thermal Information

THERMAL METRIC[(1)]		TPS22976 DPU (WSON) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	50.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	18.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	18.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics (VBIAS = 5V)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
Power Supplies and Currents								
$I_{Q,VBIAS}$	V_{BIAS} Quiescent Current (TPS22976, both channels)	$I_{OUT1} = I_{OUT2} = 0mA$, $V_{IN1,2} = V_{ON1,2} = 5V$		-40°C to 85°C		37	48	µA
$I_{Q,VBIAS}$	V_{BIAS} Quiescent Current (TPS22976, both channels)	$I_{OUT1} = I_{OUT2} = 0mA$, $V_{IN1,2} = V_{ON1,2} = 5V$		-40°C to 105°C			49	µA
$I_{Q,VBIAS}$	V_{BIAS} Quiescent Current (TPS22976, single-channel)	$I_{OUT1} = I_{OUT2} = 0mA$, $V_{ON2} = 0V$, $V_{IN1,2} = V_{IN1} = 5V$		-40°C to 85°C		35	43	µA
$I_{Q,VBIAS}$	V_{BIAS} Quiescent Current (TPS22976, single-channel)	$I_{OUT1} = I_{OUT2} = 0mA$, $V_{ON2} = 0V$, $V_{IN1,2} = V_{IN1} = 5V$		-40°C to 105°C			44	µA
$I_{Q,VBIAS}$	V_{BIAS} Quiescent Current (TPS22976A, both channels)	$I_{OUT1} = I_{OUT2} = 0mA$, $V_{IN1,2} = V_{ON1,2} = 5V$		-40°C to 85°C		85	106	µA
$I_{Q,VBIAS}$	V_{BIAS} Quiescent Current (TPS22976A, both channels)	$I_{OUT1} = I_{OUT2} = 0mA$, $V_{IN1,2} = V_{ON1,2} = 5V$		-40°C to 105°C			106	µA
$I_{Q,VBIAS}$	V_{BIAS} Quiescent Current (TPS22976A, single-channel)	$I_{OUT1} = I_{OUT2} = 0mA$, $V_{ON2} = 0V$, $V_{IN1,2} = V_{IN1} = 5V$		-40°C to 85°C		83	102	µA
$I_{Q,VBIAS}$	V_{BIAS} Quiescent Current (TPS22976A, single-channel)	$I_{OUT1} = I_{OUT2} = 0mA$, $V_{ON2} = 0V$, $V_{IN1,2} = V_{IN1} = 5V$		-40°C to 105°C			102	µA
$I_{SD,VBIAS}$	V_{BIAS} Shutdown Current	$V_{ON1,2} = 0V$, $V_{OUT1,2} = 0V$		-40°C to 105°C		1.37	2.3	µA
$I_{SD,VIN}$	V_{IN} Shutdown Current (per channel)	$V_{ON} = 0V$, $V_{OUT} = 0V$	$V_{IN} = 5V$	-40°C to 85°C		0.005	5.5	µA
$I_{SD,VIN}$	V_{IN} Shutdown Current (per channel)	$V_{ON} = 0V$, $V_{OUT} = 0V$	$V_{IN} = 5V$	-40°C to 105°C			11.3	µA
$I_{SD,VIN}$	V_{IN} Shutdown Current (per channel)	$V_{ON} = 0V$, $V_{OUT} = 0V$	$V_{IN} = 3.3V$	-40°C to 85°C		0.002	1.4	µA
$I_{SD,VIN}$	V_{IN} Shutdown Current (per channel)	$V_{ON} = 0V$, $V_{OUT} = 0V$	$V_{IN} = 3.3V$	-40°C to 105°C			3.4	µA
$I_{SD,VIN}$	V_{IN} Shutdown Current (per channel)	$V_{ON} = 0V$, $V_{OUT} = 0V$	$V_{IN} = 1.8V$	-40°C to 85°C		0.002	0.5	µA
$I_{SD,VIN}$	V_{IN} Shutdown Current (per channel)	$V_{ON} = 0V$, $V_{OUT} = 0V$	$V_{IN} = 1.8V$	-40°C to 105°C			1.4	µA
$I_{SD,VIN}$	V_{IN} Shutdown Current (per channel)	$V_{ON} = 0V$, $V_{OUT} = 0V$	$V_{IN} = 0.6V$	-40°C to 85°C		0.001	0.3	µA
$I_{SD,VIN}$	V_{IN} Shutdown Current (per channel)	$V_{ON} = 0V$, $V_{OUT} = 0V$	$V_{IN} = 0.6V$	-40°C to 105°C			0.8	µA
I_{ON}	ON Pin Leakage Current		$V_{ON} = 5.5V$	-40°C to 105°C			0.1	µA
Resistance Characteristics								
R_{ON}	On-Resistance	$I_{OUT} = -200mA$	$V_{IN} = 5V$	25°C		14	18	mΩ
R_{ON}	On-Resistance	$I_{OUT} = -200mA$	$V_{IN} = 5V$	-40°C to 85°C			22	mΩ
R_{ON}	On-Resistance	$I_{OUT} = -200mA$	$V_{IN} = 5V$	-40°C to 105°C			23	mΩ
R_{ON}	On-Resistance	$I_{OUT} = -200mA$	$V_{IN} = 3.3V$	25°C		14	18	mΩ
R_{ON}	On-Resistance	$I_{OUT} = -200mA$	$V_{IN} = 3.3V$	-40°C to 85°C			22	mΩ
R_{ON}	On-Resistance	$I_{OUT} = -200mA$	$V_{IN} = 3.3V$	-40°C to 105°C			23	mΩ
R_{ON}	On-Resistance	$I_{OUT} = -200mA$	$V_{IN} = 1.8V$	25°C		14	18	mΩ
R_{ON}	On-Resistance	$I_{OUT} = -200mA$	$V_{IN} = 1.8V$	-40°C to 85°C			22	mΩ
R_{ON}	On-Resistance	$I_{OUT} = -200mA$	$V_{IN} = 1.8V$	-40°C to 105°C			23	mΩ
R_{ON}	On-Resistance	$I_{OUT} = -200mA$	$V_{IN} = 1.2V$	25°C		14	18	mΩ
R_{ON}	On-Resistance	$I_{OUT} = -200mA$	$V_{IN} = 1.2V$	-40°C to 85°C			22	mΩ
R_{ON}	On-Resistance	$I_{OUT} = -200mA$	$V_{IN} = 1.2V$	-40°C to 105°C			23	mΩ
R_{ON}	On-Resistance	$I_{OUT} = -200mA$	$V_{IN} = 1.05V$	25°C		14	18	mΩ
R_{ON}	On-Resistance	$I_{OUT} = -200mA$	$V_{IN} = 1.05V$	-40°C to 85°C			22	mΩ
R_{ON}	On-Resistance	$I_{OUT} = -200mA$	$V_{IN} = 1.05V$	-40°C to 105°C			23	mΩ
R_{ON}	On-Resistance	$I_{OUT} = -200mA$	$V_{IN} = 0.6V$	25°C		14	18	mΩ
R_{ON}	On-Resistance	$I_{OUT} = -200mA$	$V_{IN} = 0.6V$	-40°C to 85°C			22	mΩ
R_{ON}	On-Resistance	$I_{OUT} = -200mA$	$V_{IN} = 0.6V$	-40°C to 105°C			23	mΩ
$V_{ON,HYS}$	ON Pin Hysteresis	$V_{IN} = 5V$		25°C		90		mV
R_{PD}	Output Pulldown Resistance	$V_{IN} = V_{OUT} = 5V$, $VO_N = 0V$		-40°C to 105°C		230	280	Ω
T_{SD}	Thermal Shutdown	Junction Temperature Rising		-		160		°C
$T_{SD,HYS}$	Thermal Shutdown Hysteresis	Junction Temperature Falling		-		20		°C

7.6 Electrical Characteristics (VBIAS = 2.5V)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
Power Supplies and Currents								
$I_{Q,VBIAS}$	V_{BIAS} Quiescent Current (TPS22976, both channels)	$I_{OUT1} = I_{OUT2} = 0mA$, $V_{IN1,2} = V_{ON1,2} = 2.5V$		-40°C to 85°C		15	20	µA
				-40°C to 105°C			20	µA
	V_{BIAS} Quiescent Current (TPS22976, single-channel)	$I_{OUT1} = I_{OUT2} = 0mA$, $V_{ON2} = 0V$, $V_{IN1,2} = V_{IN1} = 2.5V$		-40°C to 85°C		14	19	µA
				-40°C to 105°C			19	µA
$I_{Q,VBIAS}$	V_{BIAS} Quiescent Current (TPS22976A, both channels)	$I_{OUT1} = I_{OUT2} = 0mA$, $V_{IN1,2} = V_{ON1,2} = 2.5V$		-40°C to 85°C		26	37	µA
				-40°C to 105°C			37	µA
	V_{BIAS} Quiescent Current (TPS22976A, single-channel)	$I_{OUT1} = I_{OUT2} = 0mA$, $V_{IN1,2} = V_{ON1,2} = 2.5V$		-40°C to 85°C		25	36	µA
				-40°C to 105°C			36	µA
$I_{SD,VBIAS}$	V_{BIAS} Shutdown Current	$V_{ON1,2} = 0V$, $V_{OUT1,2} = 0V$		-40°C to 105°C		0.58	1.1	µA
$I_{SD,VIN}$	V_{IN} Shutdown Current (per channel)	$V_{ON} = 0V$, $V_{OUT} = 0V$	$V_{IN} = 2.5V$	-40°C to 85°C		0.005	0.8	µA
				-40°C to 105°C			2.1	µA
			$V_{IN} = 1.8V$	-40°C to 85°C		0.002	0.5	µA
				-40°C to 105°C			1.4	µA
			$V_{IN} = 1.05V$	-40°C to 85°C		0.002	0.3	µA
				-40°C to 105°C			1	µA
			$V_{IN} = 0.6V$	-40°C to 85°C		0.001	0.3	µA
				-40°C to 105°C			0.8	µA
I_{ON}	ON Pin Leakage Current		$V_{ON} = 5.5V$	-40°C to 105°C			0.1	µA
Resistance Characteristics								
R_{ON}	On-Resistance	$I_{OUT} = -200mA$	$V_{IN} = 2.5V$	25°C		18	23	mΩ
				-40°C to 85°C			28	mΩ
				-40°C to 105°C			30	mΩ
			$V_{IN} = 1.8V$	25°C		16	23	mΩ
				-40°C to 85°C			28	mΩ
				-40°C to 105°C			29	mΩ
			$V_{IN} = 1.5V$	25°C		16	22	mΩ
				-40°C to 85°C			27	mΩ
				-40°C to 105°C			28	mΩ
			$V_{IN} = 1.2V$	25°C		16	21	mΩ
				-40°C to 85°C			26	mΩ
				-40°C to 105°C			28	mΩ
			$V_{IN} = 1.05V$	25°C		16	21	mΩ
				-40°C to 85°C			25	mΩ
				-40°C to 105°C			27	mΩ
			$V_{IN} = 0.6V$	25°C		15	20	mΩ
				-40°C to 85°C			25	mΩ
				-40°C to 105°C			26	mΩ
$V_{ON,HYS}$	ON Pin Hysteresis	$V_{IN} = 2.5V$		25°C		70		mV
R_{PD}	Output Pulldown Resistance	$V_{IN} = V_{OUT} = 2.5V$, $V_{ON} = 0V$		-40°C to 105°C		250	330	Ω
T_{SD}	Thermal Shutdown	Junction Temperature Rising		-		160		°C
$T_{SD,HYS}$	Thermal Shutdown Hysteresis	Junction Temperature Falling		-		20		°C

7.7 Switching Characteristics (TPS22976, TPS22976N)

over operating free-air temperature range (unless otherwise noted)

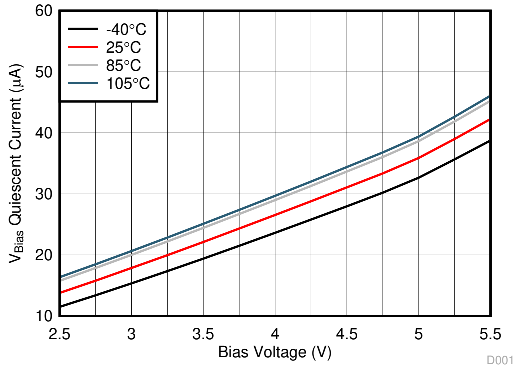
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN = VON = VBIAS = 5V, TA = 25°C						
t_{ON}	Turn ON Time	R_L = 10Ω, C_L = 0.1uF, CT = 1000pF		2390		µs
t_{OFF}	Turn OFF Time	R_L = 10Ω, C_L = 0.1uF, CT = 1000pF		3		µs
t_R	Rise Time	R_L = 10Ω, C_L = 0.1uF, CT = 1000pF		1770		µs
t_F	Fall Time	R_L = 10Ω, C_L = 0.1uF, CT = 1000pF		2		µs
t_D	Delay Time	R_L = 10Ω, C_L = 0.1uF, CT = 1000pF		620		µs
VIN = 0.6V, VON = VBIAS = 5V, TA = 25°C						
t_{ON}	Turn ON Time	R_L = 10Ω, C_L = 0.1uF, CT = 1000pF		745		µs
t_{OFF}	Turn OFF Time	R_L = 10Ω, C_L = 0.1uF, CT = 1000pF		3		µs
t_R	Rise Time	R_L = 10Ω, C_L = 0.1uF, CT = 1000pF		285		µs
t_F	Fall Time	R_L = 10Ω, C_L = 0.1uF, CT = 1000pF		2		µs
t_D	Delay Time	R_L = 10Ω, C_L = 0.1uF, CT = 1000pF		460		µs
VIN = 2.5V, VON = 5V, VBIAS = 2.5V, TA = 25°C						
t_{ON}	Turn ON Time	R_L = 10Ω, C_L = 0.1uF, CT = 1000pF		3485		µs
t_{OFF}	Turn OFF Time	R_L = 10Ω, C_L = 0.1uF, CT = 1000pF		4		µs
t_R	Rise Time	R_L = 10Ω, C_L = 0.1uF, CT = 1000pF		2275		µs
t_F	Fall Time	R_L = 10Ω, C_L = 0.1uF, CT = 1000pF		2		µs
t_D	Delay Time	R_L = 10Ω, C_L = 0.1uF, CT = 1000pF		1210		µs
VIN = 0.6V, VON = 5V, VBIAS = 2.5V, TA = 25°C						
t_{ON}	Turn ON Time	R_L = 10Ω, C_L = 0.1uF, CT = 1000pF		1730		µs
t_{OFF}	Turn OFF Time	R_L = 10Ω, C_L = 0.1uF, CT = 1000pF		5		µs
t_R	Rise Time	R_L = 10Ω, C_L = 0.1uF, CT = 1000pF		700		µs
t_F	Fall Time	R_L = 10Ω, C_L = 0.1uF, CT = 1000pF		2		µs
t_D	Delay Time	R_L = 10Ω, C_L = 0.1uF, CT = 1000pF		1030		µs
VIN = 1.05V, VON = VBIAS = 5V, TA = -40°C to 85°C						

7.8 Switching Characteristics (TPS22976A)

over operating free-air temperature range (unless otherwise noted)

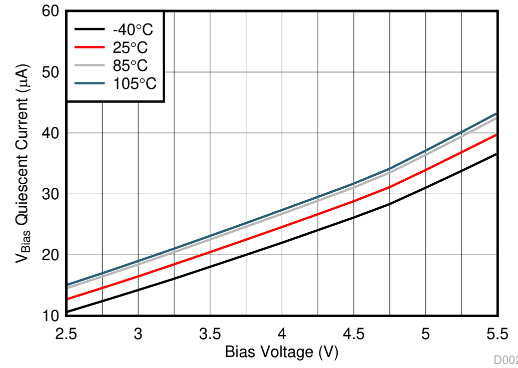
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN = VON = VBIAS = 5V, TA = 25°C						
t_{ON}	Turn ON Time	R_L = 10Ω, C_L = 0.1uF, CT = 1000pF		350		µs
t_{OFF}	Turn OFF Time	R_L = 10Ω, C_L = 0.1uF, CT = 1000pF		2		µs
t_R	Rise Time	R_L = 10Ω, C_L = 0.1uF, CT = 1000pF		263		µs
t_F	Fall Time	R_L = 10Ω, C_L = 0.1uF, CT = 1000pF		2		µs
t_D	Delay Time	R_L = 10Ω, C_L = 0.1uF, CT = 1000pF		86		µs
VIN = 0.6V, VON = VBIAS = 5V, TA = 25°C						
t_{ON}	Turn ON Time	R_L = 10Ω, C_L = 0.1uF, CT = 1000pF		100		µs
t_{OFF}	Turn OFF Time	R_L = 10Ω, C_L = 0.1uF, CT = 1000pF		2		µs
t_R	Rise Time	R_L = 10Ω, C_L = 0.1uF, CT = 1000pF		41		µs
t_F	Fall Time	R_L = 10Ω, C_L = 0.1uF, CT = 1000pF		2		µs
t_D	Delay Time	R_L = 10Ω, C_L = 0.1uF, CT = 1000pF		58		µs
VIN = 2.5V, VON = 5V, VBIAS = 2.5V, TA = 25°C						
t_{ON}	Turn ON Time	R_L = 10Ω, C_L = 0.1uF, CT = 1000pF		612		µs
t_{OFF}	Turn OFF Time	R_L = 10Ω, C_L = 0.1uF, CT = 1000pF		3		µs
t_R	Rise Time	R_L = 10Ω, C_L = 0.1uF, CT = 1000pF		392		µs
t_F	Fall Time	R_L = 10Ω, C_L = 0.1uF, CT = 1000pF		2		µs
t_D	Delay Time	R_L = 10Ω, C_L = 0.1uF, CT = 1000pF		221		µs
VIN = 0.6V, VON = 5V, VBIAS = 2.5V, TA = 25°C						
t_{ON}	Turn ON Time	R_L = 10Ω, C_L = 0.1uF, CT = 1000pF		301		µs
t_{OFF}	Turn OFF Time	R_L = 10Ω, C_L = 0.1uF, CT = 1000pF		3		µs
t_R	Rise Time	R_L = 10Ω, C_L = 0.1uF, CT = 1000pF		119		µs
t_F	Fall Time	R_L = 10Ω, C_L = 0.1uF, CT = 1000pF		2		µs
t_D	Delay Time	R_L = 10Ω, C_L = 0.1uF, CT = 1000pF		182		µs
VIN = 1.05V, VON = VBIAS = 5V, TA = -40°C to 85°C						
t_{ON}	Turn ON Time	R_L = 10Ω, C_L = 0.1uF, CT = 0pF		17	42	µs
t_{OFF}	Turn OFF Time	R_L = 10Ω, C_L = 0.1uF, CT = 0pF		2		µs
t_R	Rise Time	R_L = 10Ω, C_L = 0.1uF, CT = 0pF		6	25	µs
t_F	Fall Time	R_L = 10Ω, C_L = 0.1uF, CT = 0pF		2		µs
t_D	Delay Time	R_L = 10Ω, C_L = 0.1uF, CT = 0pF		11	25	µs

7.9 Typical DC Characteristics



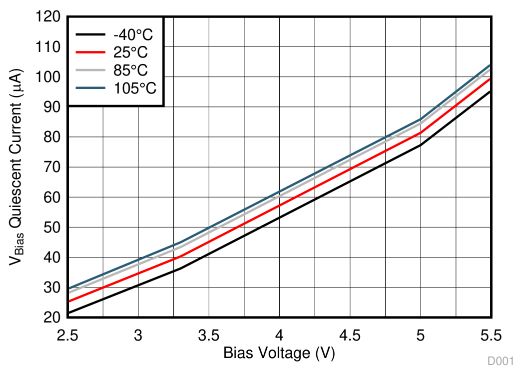
$V_{IN1} = V_{IN2} = V_{BIAS}$ $V_{ON1} = V_{ON2} = 5$ V V_{OUT} = Open

Figure 7-1. V_{BIAS} Quiescent Current vs Bias Voltage Both Channels (TPS22976, TPS22976N)



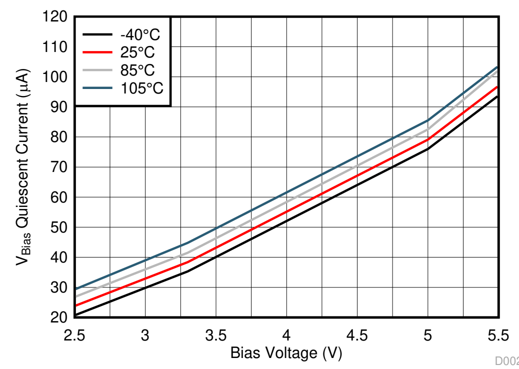
$V_{IN1} = V_{BIAS}$ $V_{ON1} = 5$ V V_{OUT} = Open

Figure 7-2. V_{BIAS} Quiescent Current vs Bias Voltage Single Channel (TPS22976, TPS22976N)



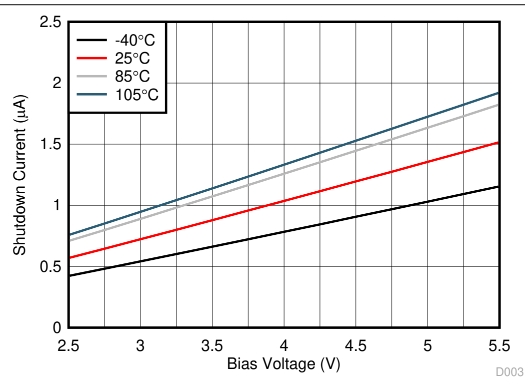
$V_{IN1} = V_{IN2} = V_{BIAS}$ $V_{ON1} = V_{ON2} = 5$ V V_{OUT} = Open

Figure 7-3. V_{BIAS} Quiescent Current vs Bias Voltage Both Channels (TPS22976A)



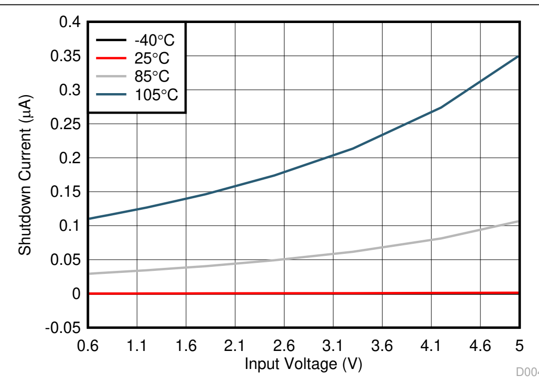
$V_{IN1} = V_{BIAS}$ $V_{ON1} = 5$ V V_{OUT} = Open

Figure 7-4. V_{BIAS} Quiescent Current vs Bias Voltage Single Channel (TPS22976A)



$V_{IN1} = V_{IN2} = V_{BIAS}$ $V_{ON1} = V_{ON2} = 0$ V $V_{OUT} = 0$ V

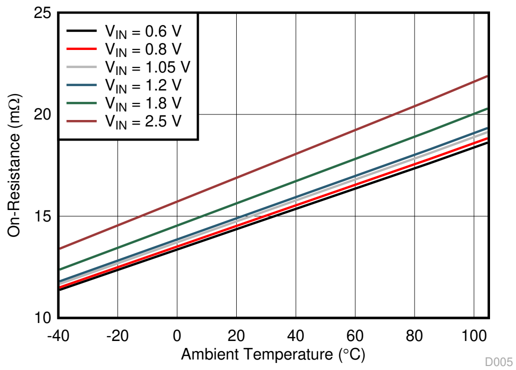
Figure 7-5. V_{BIAS} Shutdown Current vs Bias Voltage Both Channels



$V_{BIAS} = 5$ V $V_{ON} = 0$ V $V_{OUT} = 0$ V

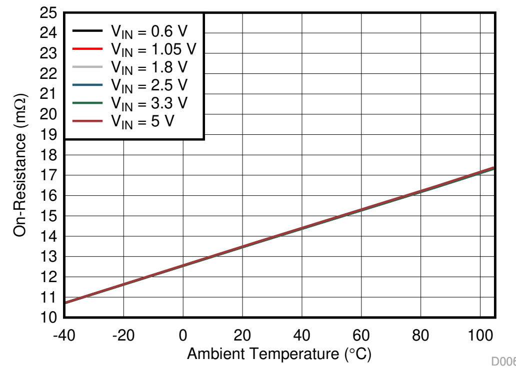
Note: –40°C and 25°C curves have similar values, therefore only one line is visible.

Figure 7-6. Off-State V_{IN} Current vs Input Voltage Single Channel



V_{BIAS} = 2.5 V I_{OUT} = –200 mA V_{ON} = 5 V

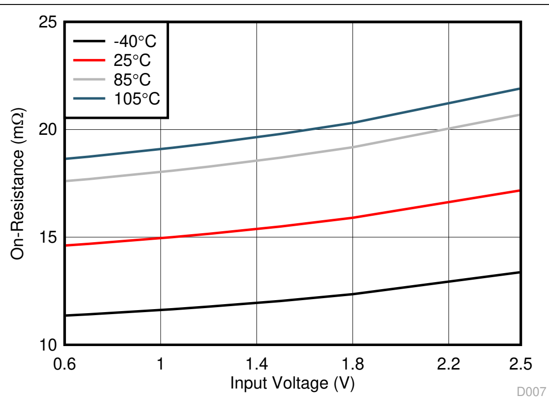
Figure 7-7. On-Resistance vs Ambient Temperature Single Channel



V_{BIAS} = 5 V I_{OUT} = –200 mA V_{ON} = 5 V

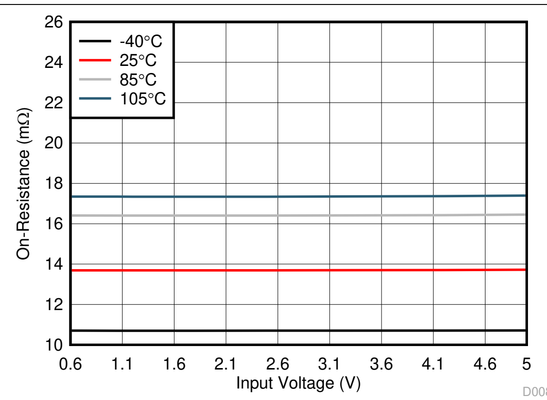
Note: All R_{ON} curves have similar values, therefore only one line is visible.

Figure 7-8. On-Resistance vs Ambient Temperature Single Channel



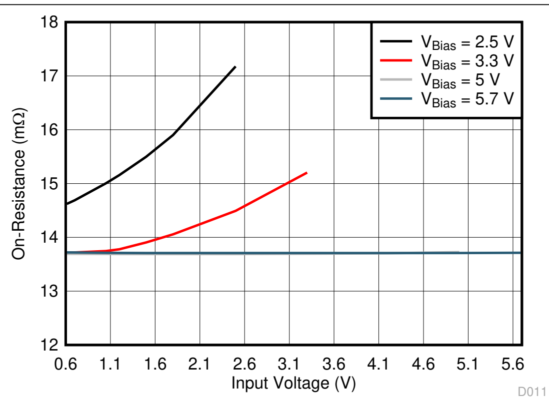
V_{BIAS} = 2.5 V I_{OUT} = –200 mA V_{ON} = 5 V

Figure 7-9. On-Resistance vs Input Voltage Single Channel - Across Ambient Temperatures



V_{BIAS} = 5 V I_{OUT} = –200 mA V_{ON} = 5 V

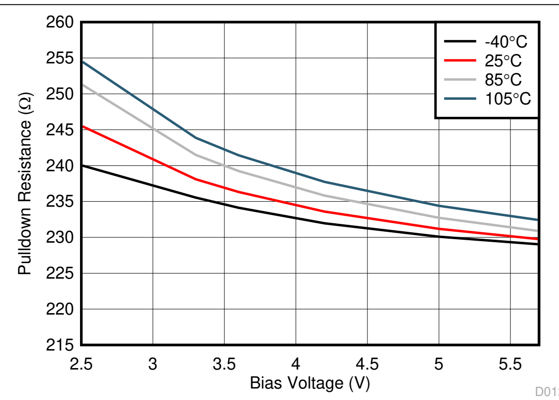
Figure 7-10. On-Resistance vs Input Voltage Single Channel - Across Ambient Temperatures



T_A = 25°C

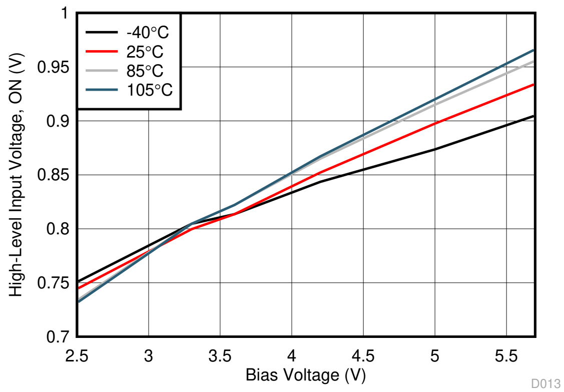
Note: V_{BIAS} = 5 V and 5.7 V curves have similar values, therefore only one line is visible.

Figure 7-11. On-Resistance vs Input Voltage Single Channel - Across V_{BIAS}



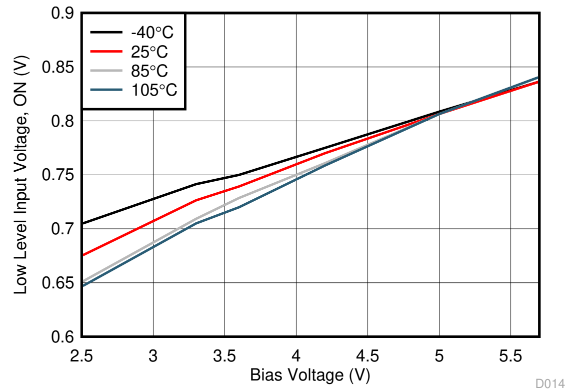
V_{IN} = 2.5 V V_{ON} = 0 V

Figure 7-12. Pulldown Resistance vs Bias Voltage Single Channel



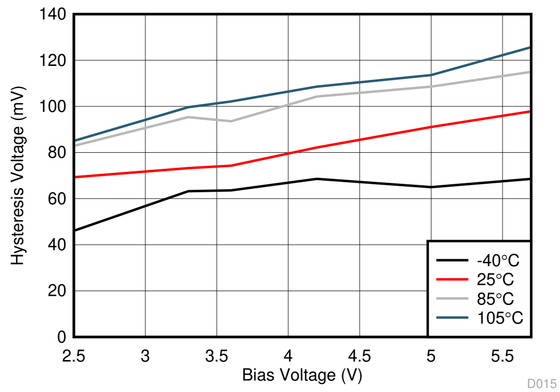
$V_{IN} = V_{BIAS}$

Figure 7-13. High-Level Input Voltage vs Bias Voltage



$V_{IN} = V_{BIAS}$

Figure 7-14. Low-Level Input Voltage vs Bias Voltage



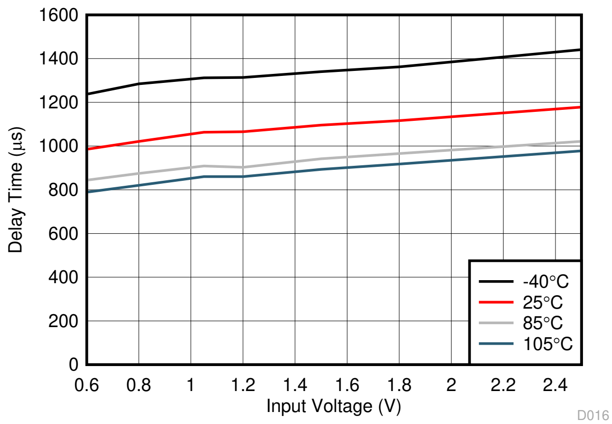
$V_{IN} = V_{BIAS}$

Figure 7-15. Voltage Input Hysteresis vs Bias Voltage

7.10 Typical AC Characteristics

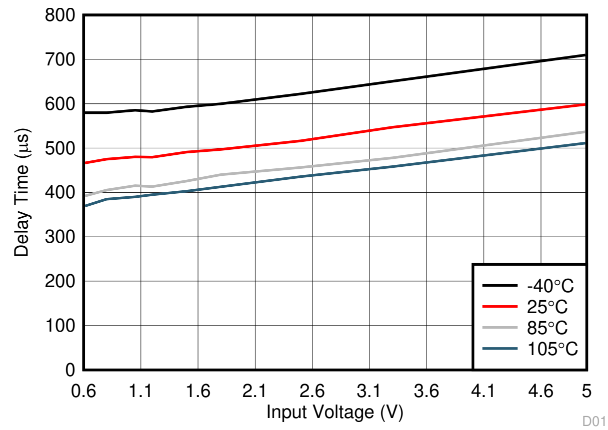
AC Characteristics (TPS22976, TPS22976N)

T_A = 25°C, C_T = 1000 pF, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω, V_{ON} = 5 V



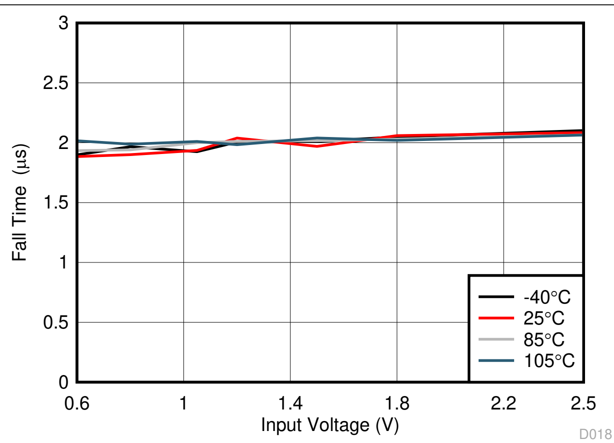
V_{BIAS} = 2.5 V

Figure 7-16. Delay Time vs Input Voltage



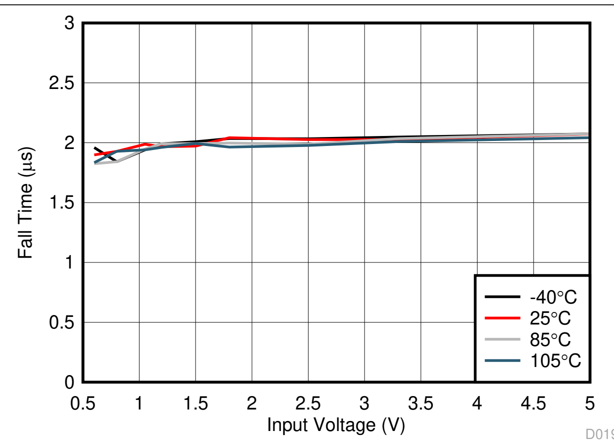
V_{BIAS} = 5 V

Figure 7-17. Delay Time vs Input Voltage



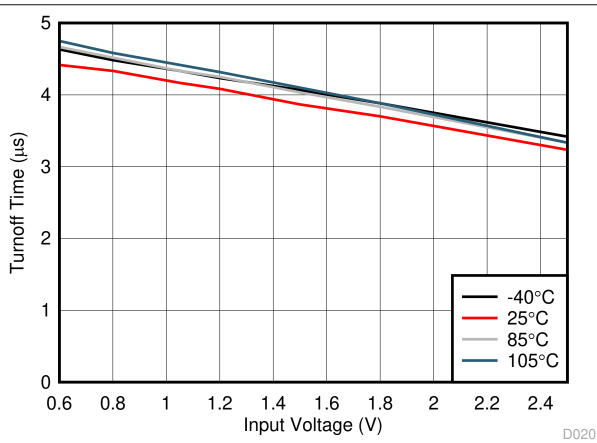
V_{BIAS} = 2.5 V

Figure 7-18. Fall Time vs Input Voltage



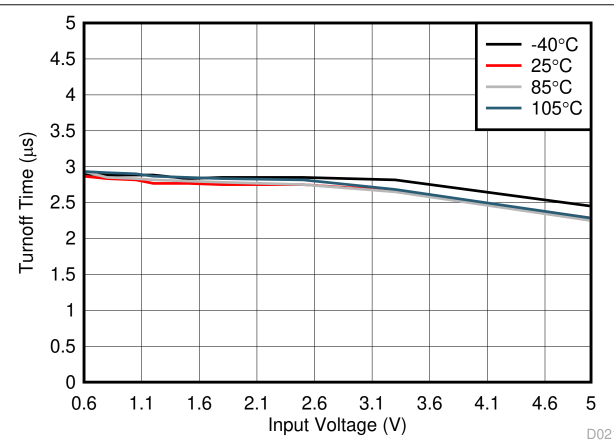
V_{BIAS} = 5 V

Figure 7-19. Fall Time vs Input Voltage



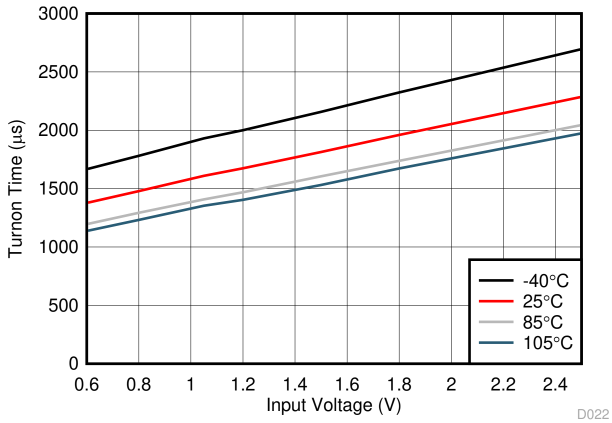
V_{BIAS} = 2.5 V

Figure 7-20. Turnoff Time vs Input Voltage



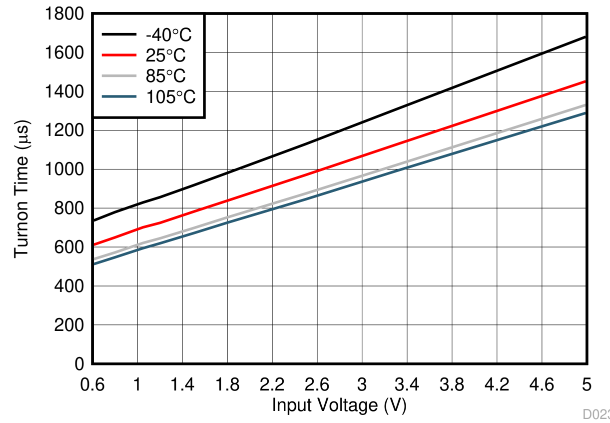
V_{BIAS} = 5 V

Figure 7-21. Turnoff Time vs Input Voltage



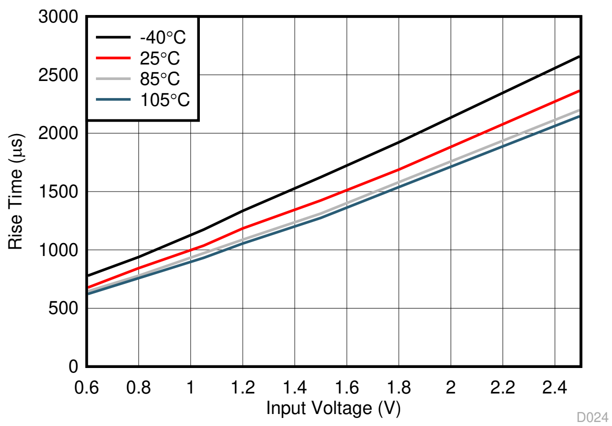
V_{BIAS} = 2.5 V

Figure 7-22. Turnon Time vs Input Voltage



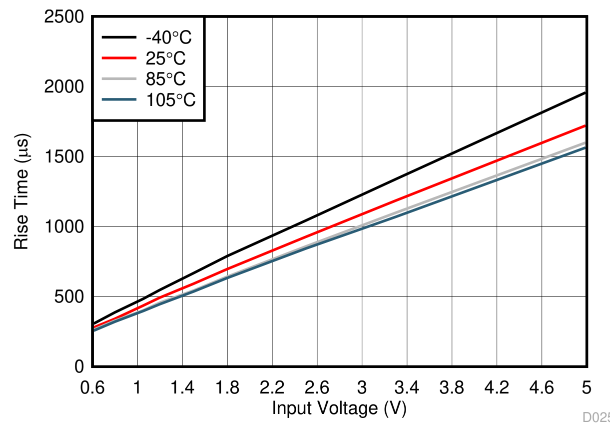
V_{BIAS} = 5 V

Figure 7-23. Turnon Time vs Input Voltage



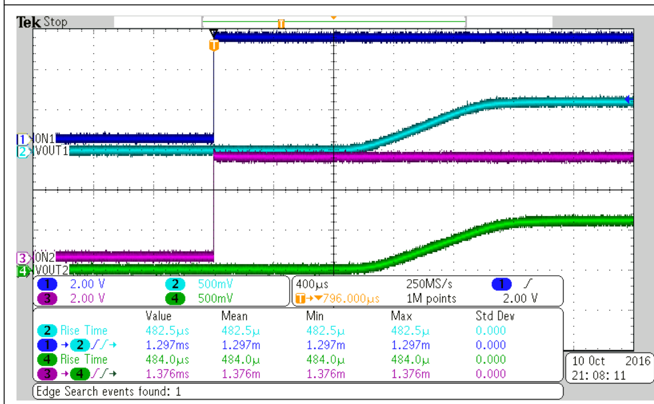
V_{BIAS} = 2.5 V

Figure 7-24. Rise Time vs Input Voltage



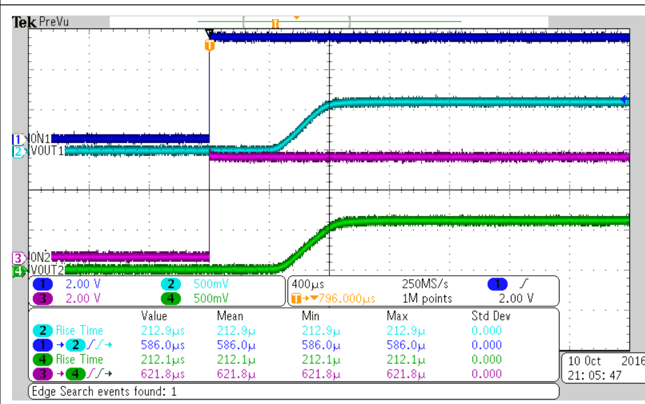
V_{BIAS} = 5 V

Figure 7-25. Rise Time vs Input Voltage



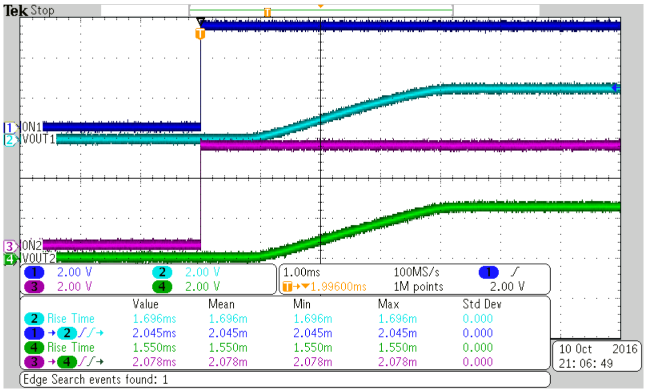
V_{IN} = 0.6 V V_{BIAS} = 2.5 V

Figure 7-26. Turnon Response Time



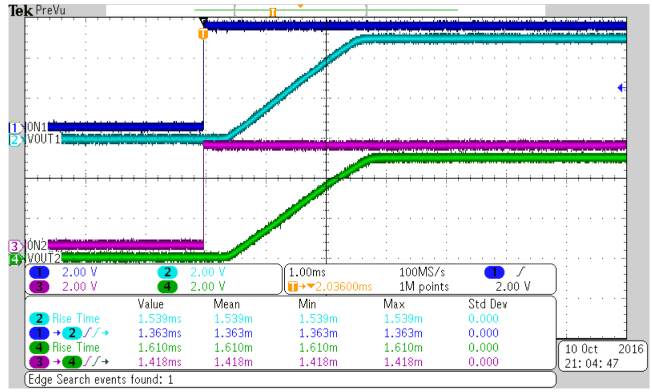
V_{IN} = 0.6 V V_{BIAS} = 5 V

Figure 7-27. Turnon Response Time



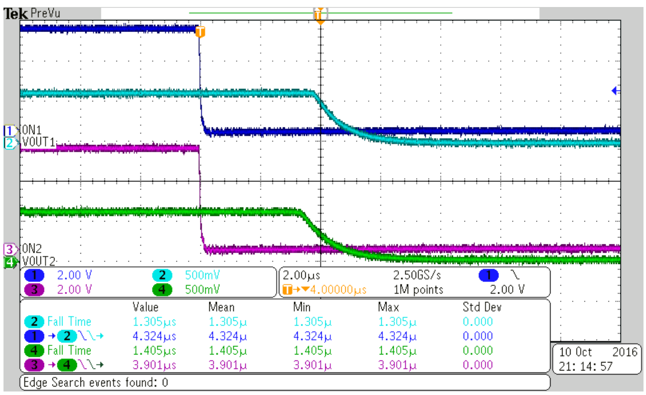
V_{IN} = 2.5 V V_{BIAS} = 2.5 V

Figure 7-28. Turnon Response Time



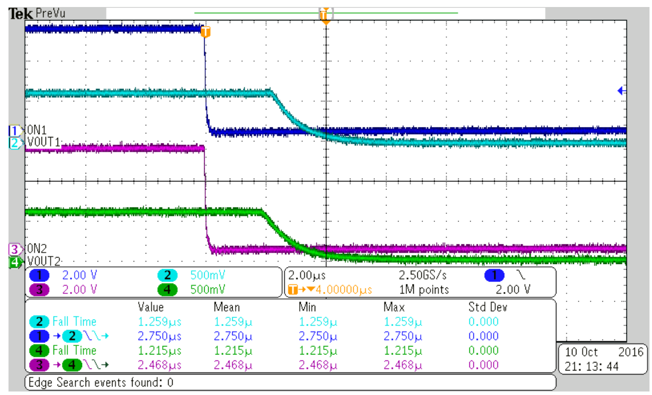
V_{IN} = 5 V V_{BIAS} = 5 V

Figure 7-29. Turnon Response Time



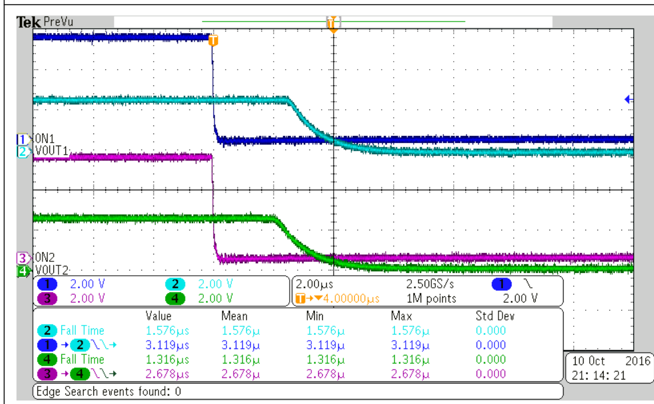
V_{IN} = 0.6 V V_{BIAS} = 2.5 V

Figure 7-30. Turnoff Response Time



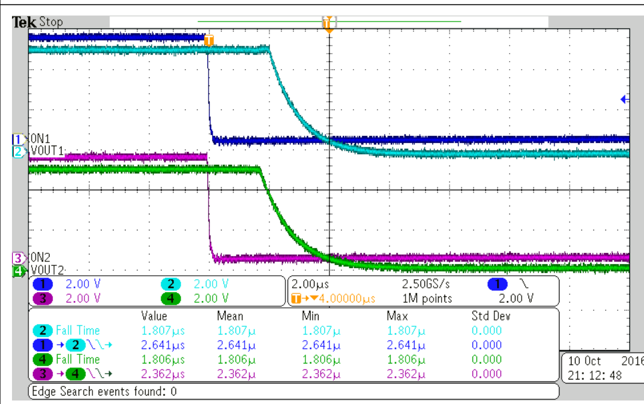
V_{IN} = 0.6 V V_{BIAS} = 5 V

Figure 7-31. Turnoff Response Time



V_{IN} = 2.5 V V_{BIAS} = 2.5 V

Figure 7-32. Turnoff Response Time

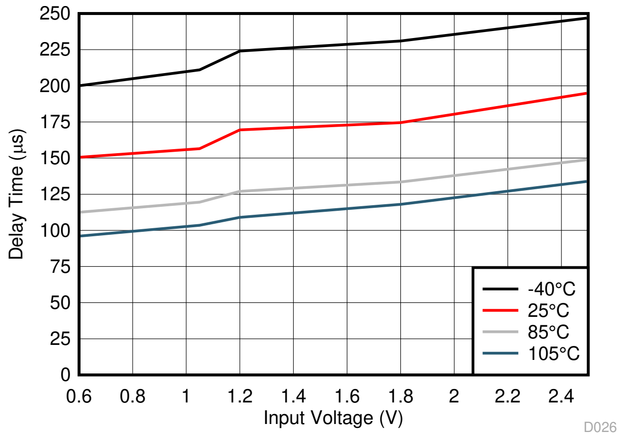


V_{IN} = 5 V V_{BIAS} = 5 V

Figure 7-33. Turnoff Response Time

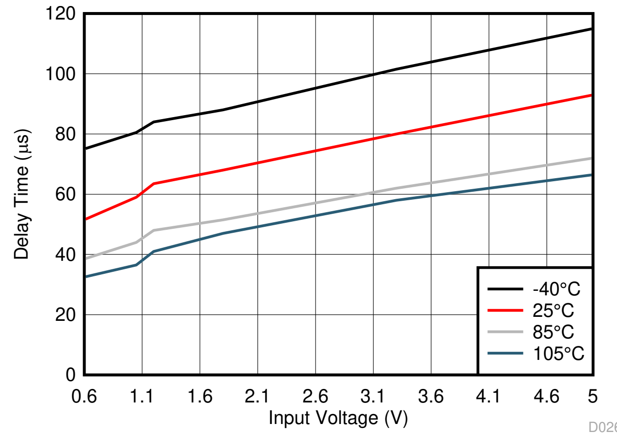
AC Characteristics (TPS22976A)

T_A = 25°C, C_T = 1000 pF, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω, V_{ON} = 5 V



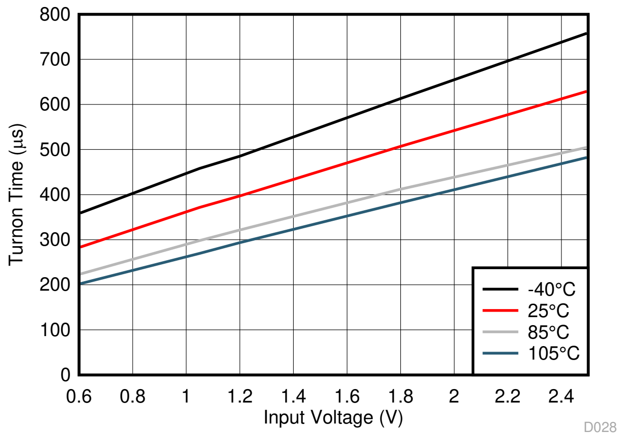
V_{BIAS} = 2.5 V

Figure 7-34. Delay Time vs Input Voltage



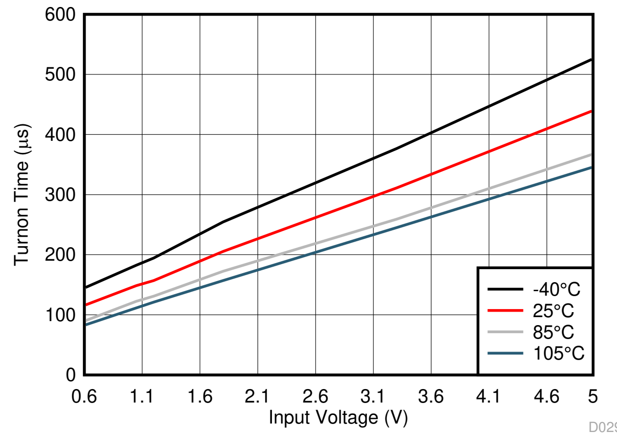
V_{BIAS} = 5 V

Figure 7-35. Delay Time vs Input Voltage



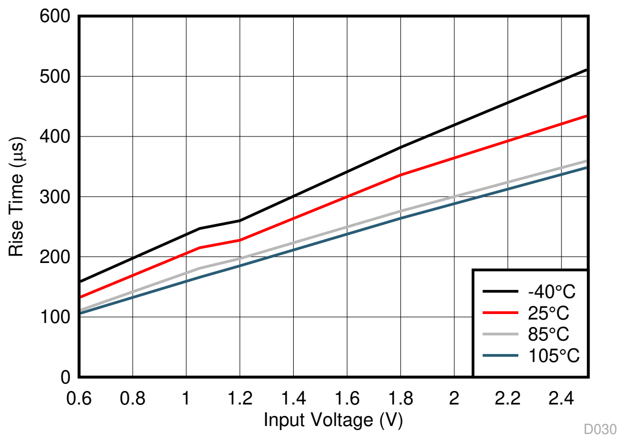
V_{BIAS} = 2.5 V

Figure 7-36. Turnon Time vs Input Voltage



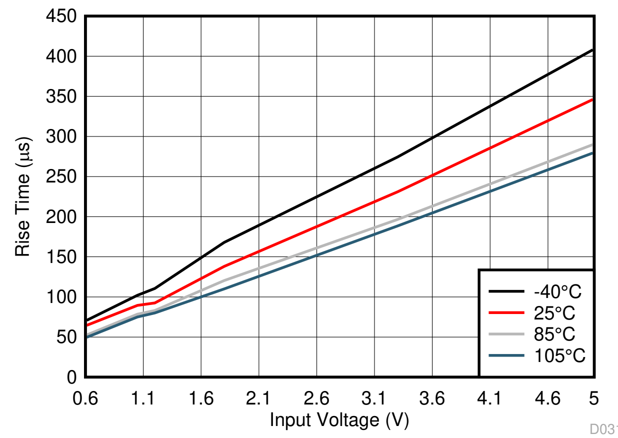
V_{BIAS} = 5 V

Figure 7-37. Turnon Time vs Input Voltage



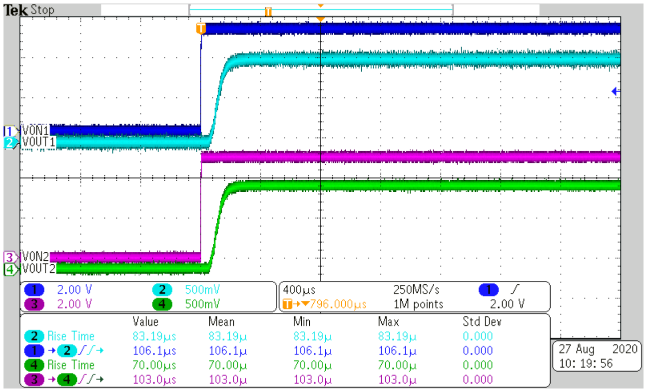
V_{BIAS} = 2.5 V

Figure 7-38. Rise Time vs Input Voltage



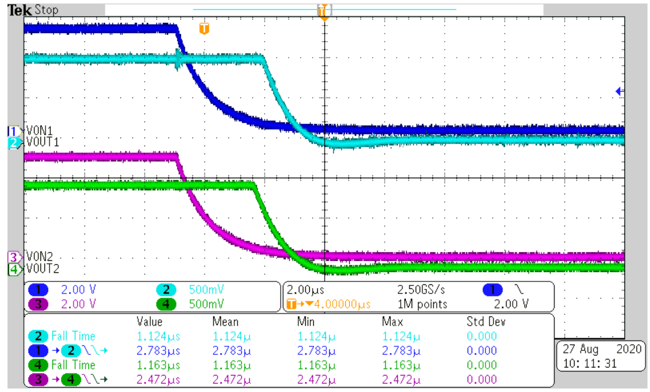
V_{BIAS} = 5 V

Figure 7-39. Rise Time vs Input Voltage



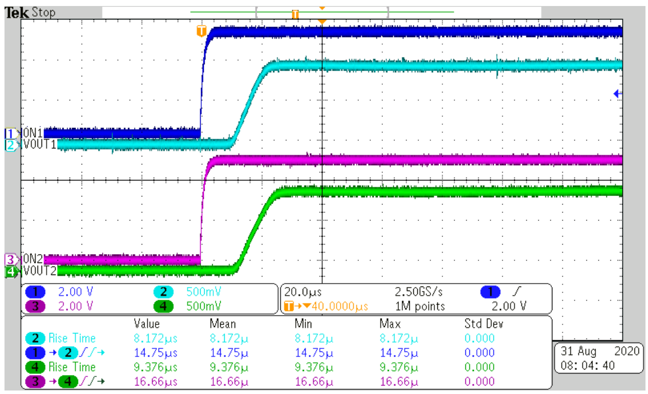
V_{IN} = 1.05 V V_{BIAS} = 5 V

Figure 7-40. Turnon Response Time



V_{IN} = 1.05 V V_{BIAS} = 5 V

Figure 7-41. Turnoff Response Time



V_{IN} = 1.05 V V_{BIAS} = 5 V C_T = 0pF

Figure 7-42. Turnon Response Time

8 Parameter Measurement Information

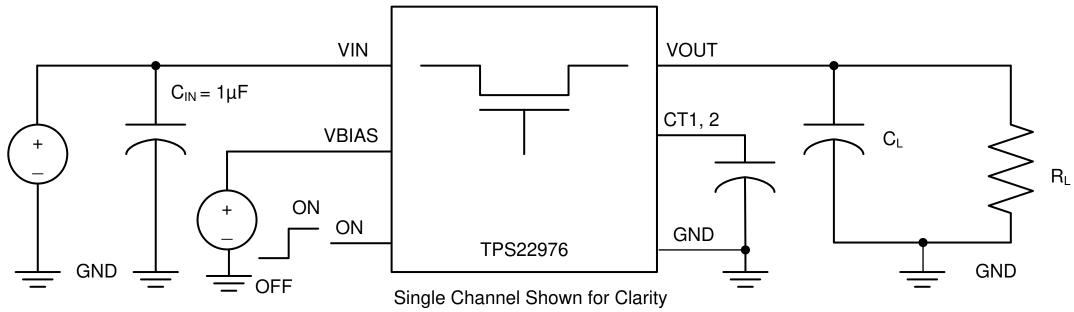


Figure 8-1. Test Circuit

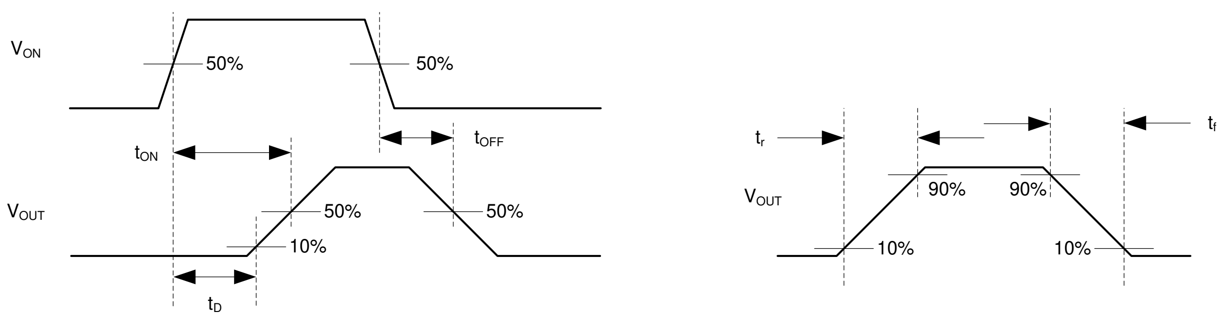


Figure 8-2. t_{ON} and t_{OFF} Waveforms

9 Detailed Description

9.1 Overview

The TPS22976 is a 5.7-V, dual-channel, 14-mΩ (typical) R_{ON} load switch in a 14-pin WSON package. Each channel can support a maximum continuous current of 6 A and is controlled by an on and off GPIO-compatible input. To reduce the voltage drop in high current rails, the device implements N-channel MOSFETs. Note that the ON pins must be connected and cannot be left floating. The device has a configurable slew rate for applications that require specific rise-time, which controls the inrush current. By controlling the inrush current, power supply sag can be reduced during turnon. Furthermore, the slew rate is proportional to the capacitor on the CT pin. See the *Adjustable Rise Time* section to determine the correct CT value for a desired rise time.

The internal circuitry is powered by the V_{BIAS} pin, which supports voltages from 2.5 V to 5.7 V. This circuitry includes the charge pump, QOD (optional), and control logic. When a voltage is applied to V_{BIAS}, and the $ON_{1,2}$ pins transition to a low state, the QOD functionality is activated. This connects V_{OUT1} and V_{OUT2} to ground through the on-chip resistor. The typical pulldown resistance (R_{PD}) is 230 Ω.

During the off state, the device prevents downstream circuits from pulling high standby current from the supply. The integrated control logic, driver, power supply, and output discharge FET eliminates the need for any external components, reducing solution size and bill of materials (BOM) count.

9.2 Functional Block Diagram

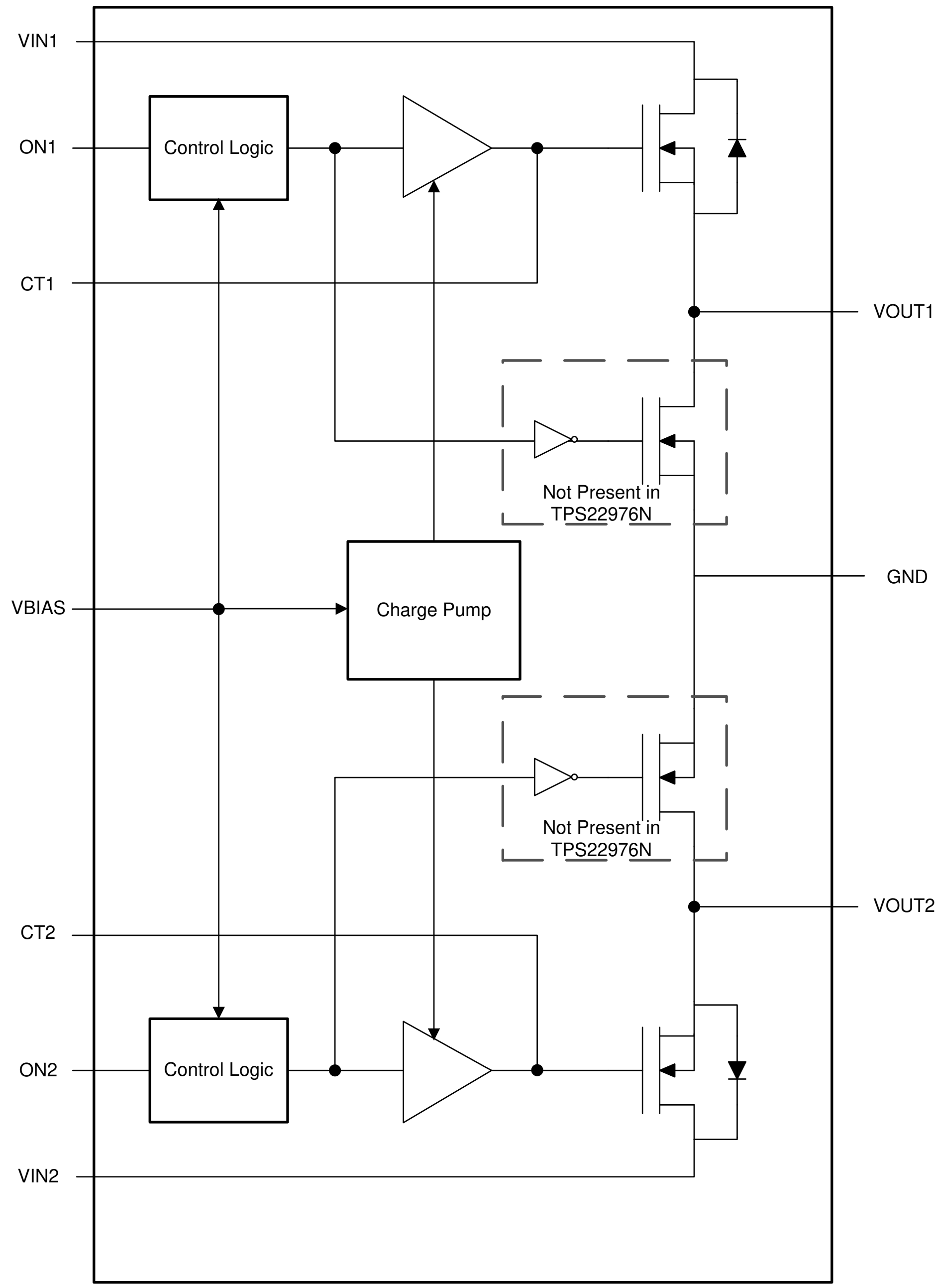


Figure 9-1. TPS22976 Functional Block Diagram

9.3 Feature Description

9.3.1 ON and OFF Control

The ON pins control the state of the switch. Asserting ON high enables the switch. ON is active high with a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2 V or higher GPIO voltage. This pin cannot be left floating and must be tied either high or low for proper functionality.

9.3.2 Input Capacitor (Optional)

To limit the voltage drop on the input supply caused by transient inrush currents when the switch turns on into a discharged load capacitor, a capacitor needs to be placed between VIN and GND. A 1-µF ceramic capacitor, C_{IN}, placed close to the pins is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high-current application. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop.

9.3.3 Output Capacitor (Optional)

Due to the integrated body diode in the NMOS switch, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from VOUT to VIN. A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup, however a 10 to 1 ratio for capacitance is not required for proper functionality of the device. A ratio smaller than 10 to 1 (such as 1 to 1) could cause slightly more V_{IN} dip upon turnon due to inrush currents. This can be mitigated by increasing the capacitance on the CT pin for a longer rise time (see the *Adjustable Rise Time* section).

9.3.4 Quick Output Discharge (QOD) (Not Present in TPS22976N)

The TPS22976 and TPS22976A include a QOD feature. When the switch is disabled, an internal discharge resistance is connected between VOUT and GND to remove the remaining charge from the output. This resistance prevents the output from floating while the switch is disabled. For best results, it is recommended that the device gets disabled before V_{BIAS} falls below the minimum recommended voltage.

9.3.5 Thermal Shutdown

Thermal Shutdown protects the part from internally or externally generated excessive temperatures. When the device temperature exceeds T_{SD} (typical 160°C), the switch is turned off. The switch automatically turns on again if the temperature of the die drops 20 degrees below the T_{SD} threshold.

9.4 Device Functional Modes

Table 9-1 lists the TPS22976 and TPS22976A functions.

Table 9-1. TPS22976 and TPS22976A Functions Table

ON	VIN to VOUT	VOUT
L	Off	GND
H	On	VIN

Table 9-2 lists the TPS22976N functions.

Table 9-2. TPS22976N Functions Table

ON	VIN to VOUT	VOUT
L	Off	Floating
H	On	VIN

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

This section highlights some of the design considerations for implementing the device in various applications. A PSPICE model for this device is also available on the product page for additional information.

10.1.1 Parallel Configuration

To increase current capabilities and to lower R_{ON}, both channels can be placed in parallel as seen in Figure 10-1. With this configuration, the CT1 and CT2 pins can be tied together to use one capacitor, CT.

See the *TPS22966 Dual-Channel Load Switch in Parallel Configuration* application report and *Parallel Load Switches for Higher Output Current & Reduced ON-Resistance Design Guide* for more information.

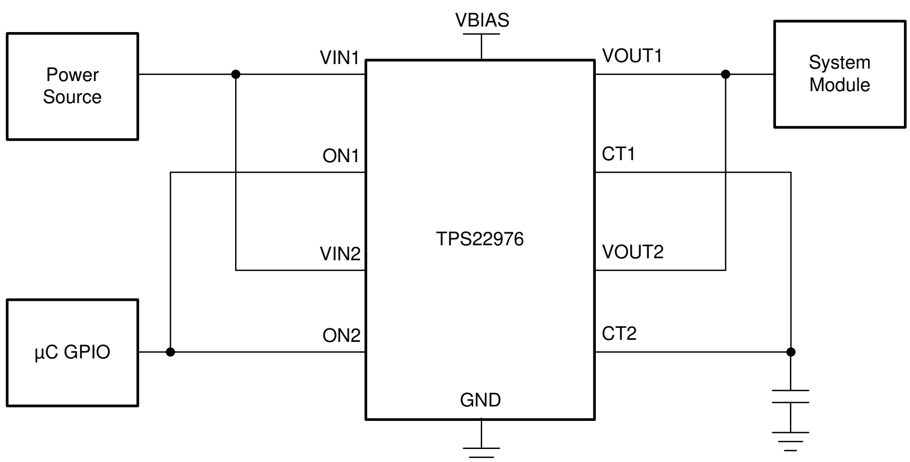


Figure 10-1. Parallel Configuration

10.1.2 Standby Power Reduction

Battery powered end equipments often have strict power budgets, in which there is a need to reduce current consumption. The TPS22976 significantly reduces system current consumption by disabling the supply voltage to subsystems in standby states. Alternatively, the TPS22976 reduces the leakage current overhead of the modules in standby mode as achieved in Figure 10-2. Note that standby power reduction can be achieved on either channel, as well as dual-channel operation.

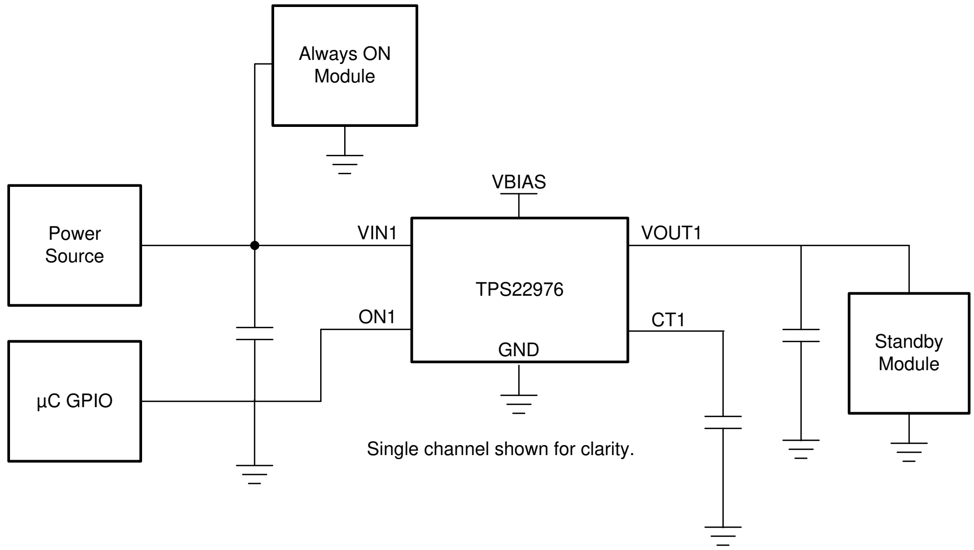


Figure 10-2. Standby Power Reduction

10.1.3 Power Supply Sequencing without GPIO Input

Sequential startup of several subsystems is often burdensome and adds complexity for several end equipments. The TPS22976 provides a power sequencing solution that reduces the overall system complexity, as seen in Figure 10-3.

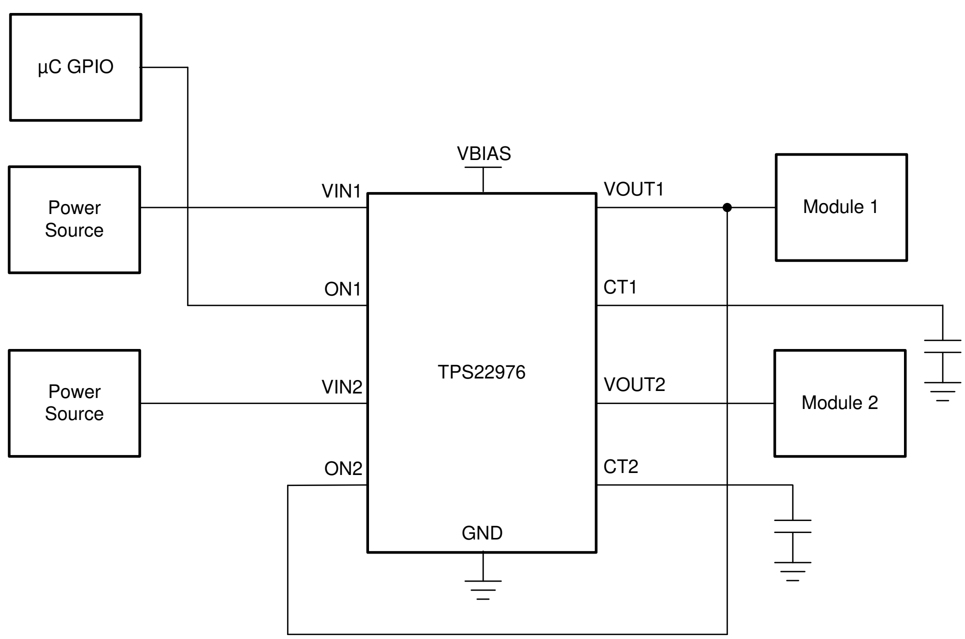


Figure 10-3. Power Sequencing without a GPIO Input

10.1.4 Reverse Current Blocking

Reverse current blocking is often desired in specific applications, as it prevents current from flowing from the output to the input of the load switch when the device is disabled. With the configuration illustrated in Figure

10-4, the TPS22976 can be converted into a single-channel switch with reverse current blocking. VIN1 or VIN2 can be used as the input and VIN2 or VIN1 as the output.

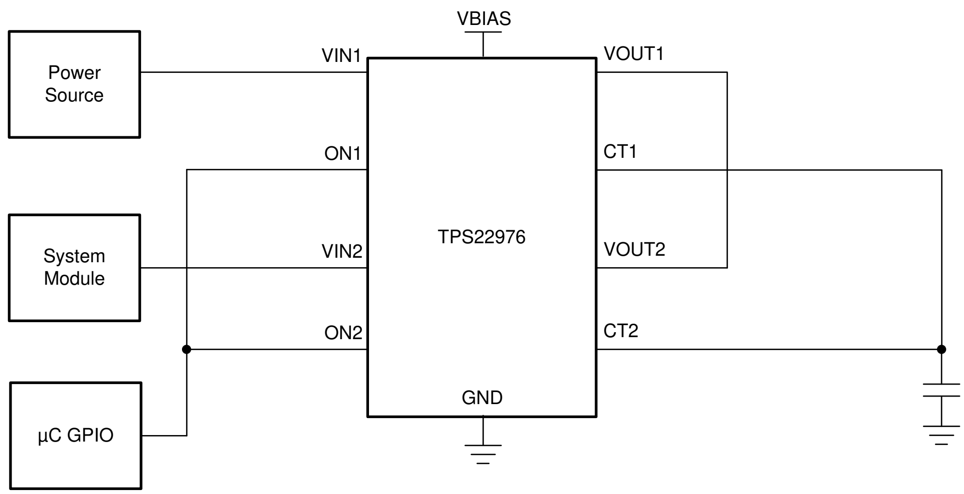


Figure 10-4. Reverse Current Blocking

10.2 Typical Application

This application demonstrates how the TPS22976 can be used to limit the inrush current when powering on downstream modules.

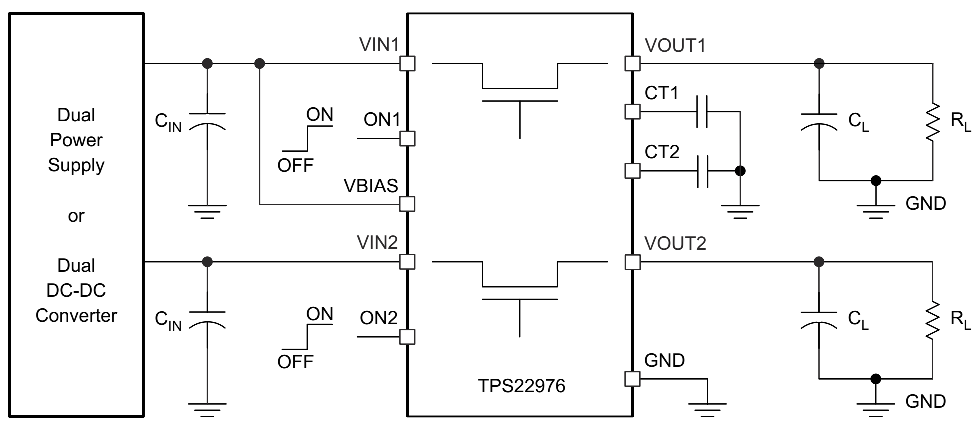


Figure 10-5. Typical Application Circuit

10.2.1 Design Requirements

Table 10-1 shows the TPS22976 design parameters.

Table 10-1. Design Parameters

DESIGN PARAMETER	VALUE
Input voltage	3.3 V
Bias voltage	5 V
Load capacitance (C_L)	22 µF
Maximum acceptable inrush current	400 mA

10.2.2 Detailed Design Procedure

10.2.2.1 Inrush Current

When the switch is enabled, the output capacitors must be charged up from 0 V to the set value (3.3 V in this example). This charge arrives in the form of inrush current. Inrush current can be calculated using Equation 1.

$$\text{Inrush Current} = C \times dV/dt \quad (1)$$

where

- C is the output capacitance
- dV is the output voltage
- dt is the rise time

The TPS22976 offers adjustable rise time for VOUT. This feature allows the user to control the inrush current during turnon. The appropriate rise time can be calculated using Table 10-1 and the inrush current equation. See Equation 2 and Equation 3.

$$400\text{ mA} = 22\ \mu\text{F} \times 3.3\text{ V}/dt \quad (2)$$

$$dt = 181.5\ \mu\text{s} \quad (3)$$

To ensure an inrush current of less than 400 mA, choose a CT value that yields a rise time of more than 181.5 µs. See the oscilloscope captures in the *Application Curves* section for an example of how the CT capacitor can be used to reduce inrush current.

10.2.2.2 Adjustable Rise Time

A capacitor to GND on the CT pins sets the slew rate for each channel. To ensure desired performance, a capacitor with a minimum voltage rating of 25 V must be used on either CT pins. An approximate formula for the relationship between CT and slew rate is shown in Equation 4, and this is valid for TPS22976 and TPS22976N. The TPS22976A has a faster rise time and is represented by Equation 5.

Equation 4 and Equation 5 account for 10% to 90% measurement on V_{OUT} and do not apply for CT < 100 pF. Use Table 10-2 to determine rise times for when CT = 0 pF.

TPS22976, TPS22976N:

$$SR = 0.42 \times CT + 66 \quad (4)$$

TPS22976A:

$$SR = 0.0606 \times CT + 22 \quad (5)$$

where

- SR is the slew rate (in µs/V)
- CT is the capacitance value on the CT pin (in pF)
- The units for the constants 66 and 22 are in µs/V.

Rise time can be calculated by multiplying the input voltage by the slew rate. Table 10-2 shows rise time values measured on a typical device. Rise times shown below are only valid for the power-up sequence where V_{IN} and V_{BIAS} are already in steady state condition, and the ON pin is asserted high.

Table 10-2. Rise Time Values (TPS22976, TPS22976N)

CT (pF)	RISE TIME (µs) 10% - 90%, C_L = 0.1 µF, C_{IN} = 1 µF, R_L = 10 Ω(1)						
	5 V	3.3 V	1.8 V	1.5 V	1.2 V	1.05 V	0.6 V
0	149	112	77	70	60	56	42
220	548	388	236	206	173	154	103
470	968	673	401	342	289	256	169
1000	1768	1220	711	608	505	445	286
2200	3916	2678	1554	1332	1097	949	627
4700	8040	5477	3179	2691	2240	1964	1249
10000	16520	11150	6410	5401	4430	3933	2526

(1) TYPICAL VALUES at 25°C, V_{BIAS} = 5 V, 25 V X7R 10% CERAMIC CAP

10.2.3 Application Curves

V_{BIAS} = 5 V ; V_{IN} = 3.3 V ; C_L = 22 µF

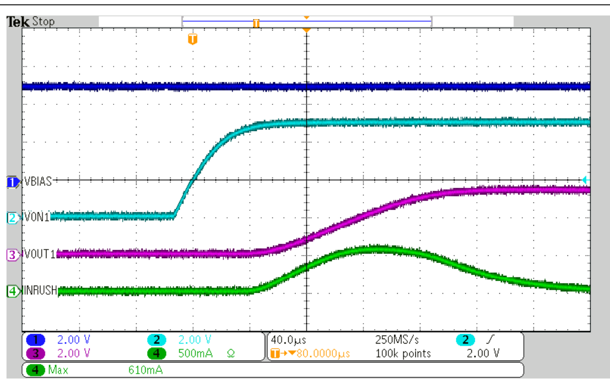


Figure 10-6. Inrush Current With CT = 0 pF

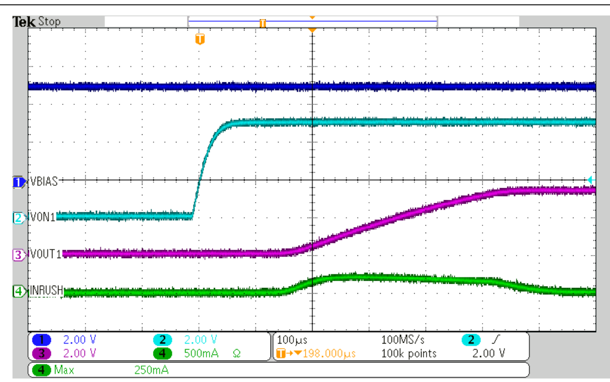


Figure 10-7. Inrush Current With CT = 220 pF

11 Power Supply Recommendations

The device is designed to operate from a V_{BIAS} range of 2.5 V to 5.7 V and a V_{IN} range of 0.6 V to V_{BIAS}.

12 Layout

12.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for V_{IN}, V_{OUT}, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

12.2 Layout Example

Notice the thermal vias located under the exposed thermal pad of the device. This allows for thermal diffusion away from the device.

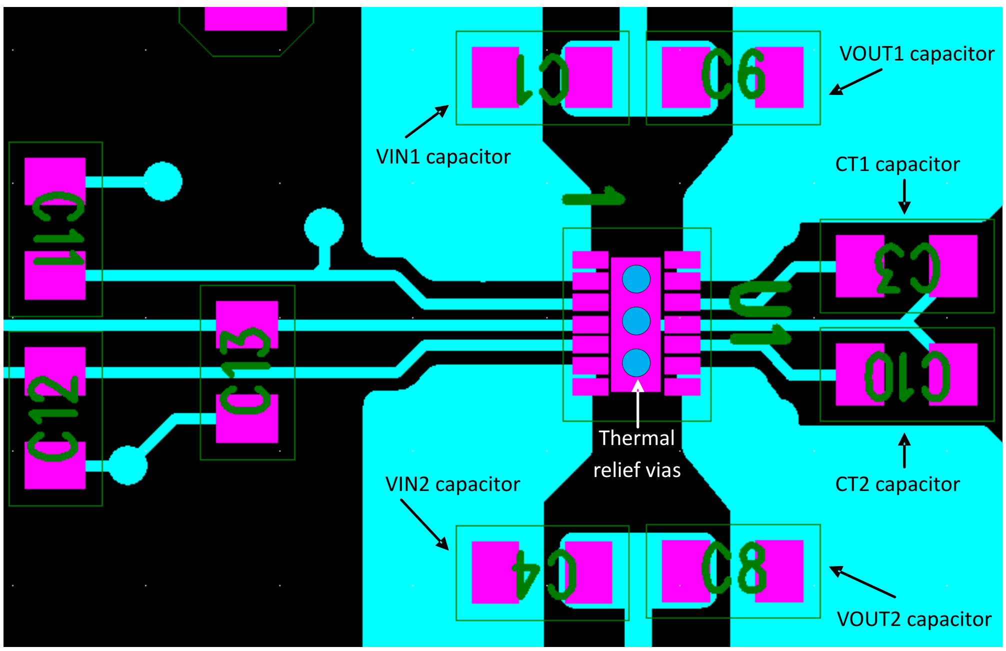


Figure 12-1. PCB Layout Example

12.3 Power Dissipation

The maximum IC junction temperature must be restricted to 125°C under normal operating conditions. To calculate the maximum allowable power dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use Equation 6.

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{\theta_{JA}} \quad (6)$$

where

- $P_{D(max)}$ is the maximum allowable power dissipation.
- $T_{J(max)}$ is the maximum allowable junction temperature (125°C for the TPS22976).
- T_A is the ambient temperature of the device.
- θ_{JA} is the junction to air thermal impedance. See the *Thermal Information* section. This parameter is highly dependent upon board layout.

13 Device and Documentation Support

13.1 Device Support

13.1.1 Developmental Support

For the TPS22976N PSpice Transient Model, see SLVMBV5.

For the TPS22976 PSpice Transient Model, see SLVMBV6.

13.2 Documentation Support

13.2.1 Related Documentation

For related documentation see the following:

TPS22976 Evaluation Module User's Guide

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

13.5 Trademarks

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13.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.7 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22976ADPUR	ACTIVE	WSON	DPU	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	22976A	Samples
TPS22976DPUR	ACTIVE	WSON	DPU	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	22976	Samples
TPS22976DPUT	ACTIVE	WSON	DPU	14	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	22976	Samples
TPS22976NDPUR	ACTIVE	WSON	DPU	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	22976N	Samples
TPS22976NDPUT	ACTIVE	WSON	DPU	14	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	22976N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

10-Dec-2020

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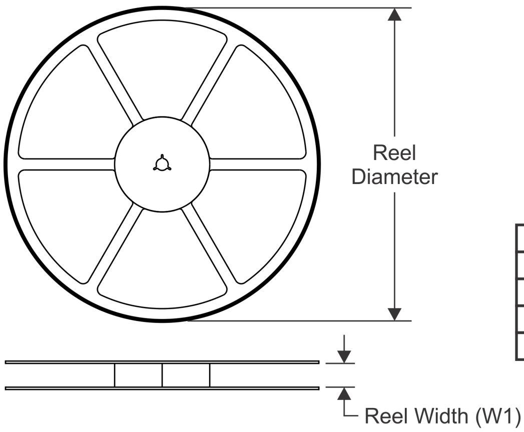
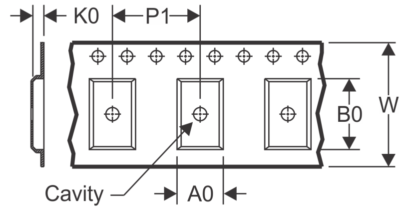
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

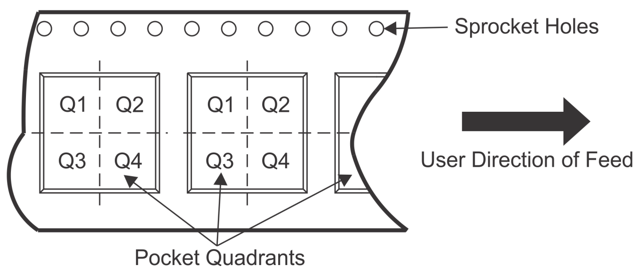


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

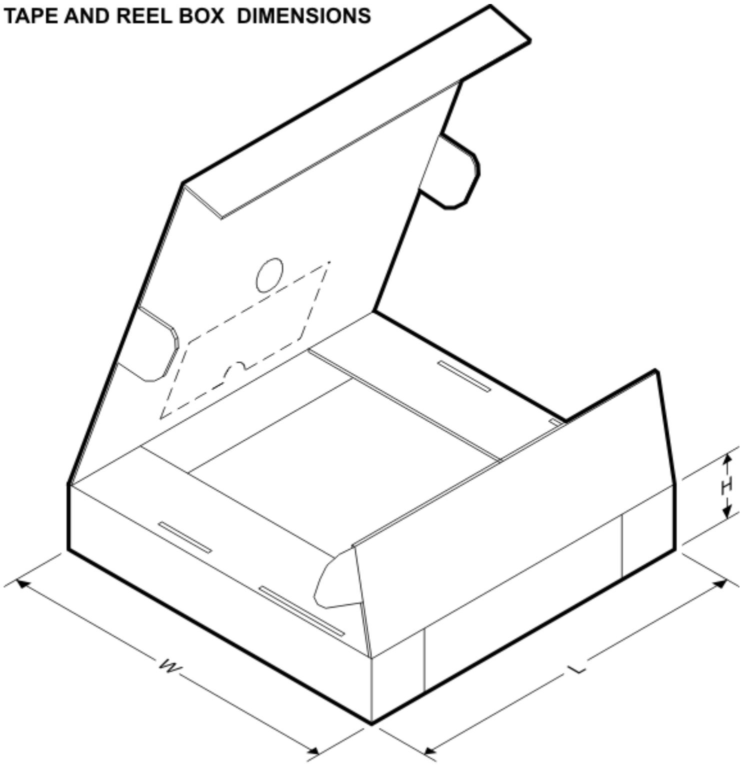
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22976ADPUR	WSON	DPU	14	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS22976ADPUR	WSON	DPU	14	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS22976DPUR	WSON	DPU	14	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS22976DPUT	WSON	DPU	14	250	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS22976NDPUR	WSON	DPU	14	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS22976NDPUT	WSON	DPU	14	250	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS22976NDPUT	WSON	DPU	14	250	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1

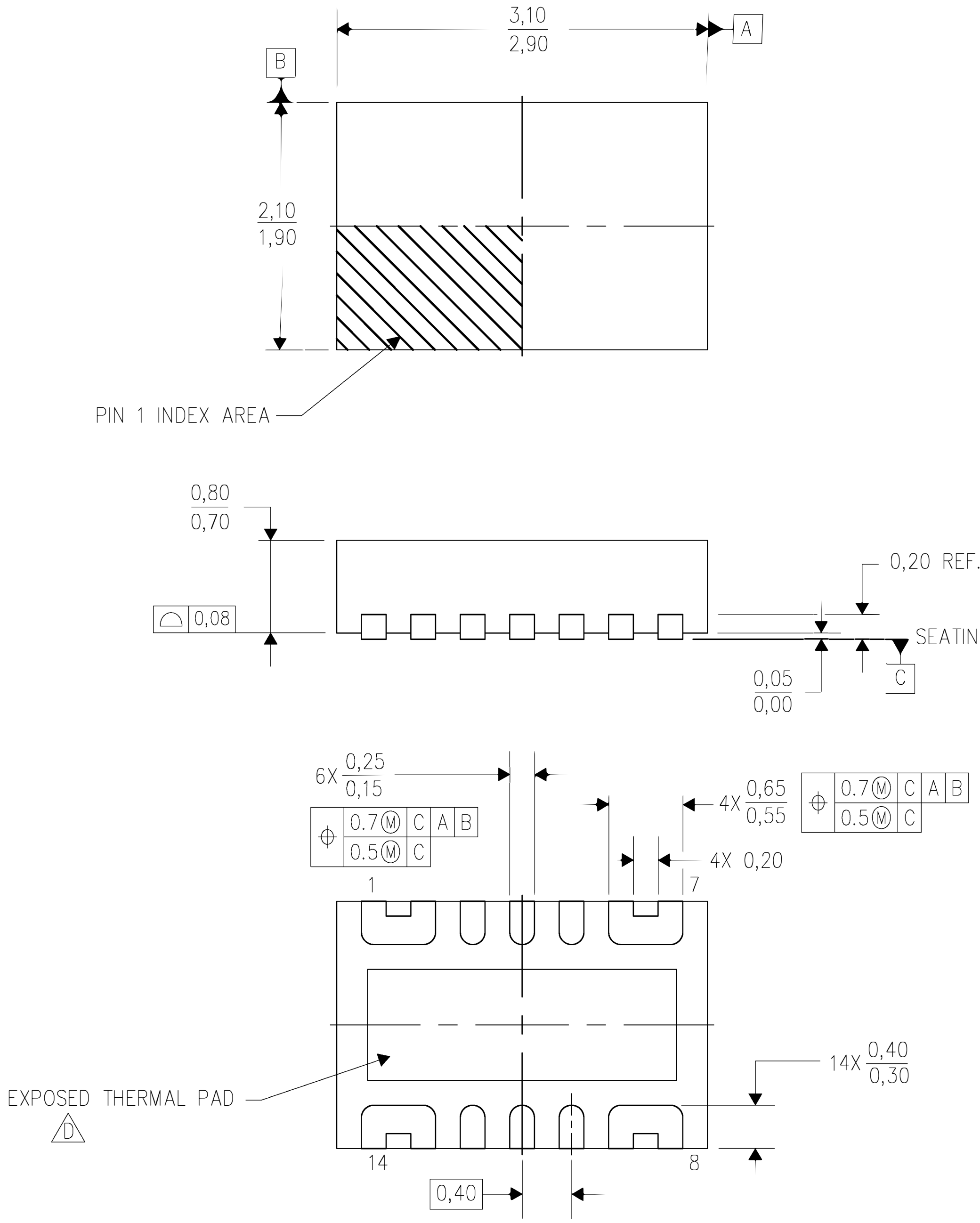
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22976ADPUR	WSON	DPU	14	3000	210.0	185.0	35.0
TPS22976ADPUR	WSON	DPU	14	3000	210.0	185.0	35.0
TPS22976DPUR	WSON	DPU	14	3000	210.0	185.0	35.0
TPS22976DPUT	WSON	DPU	14	250	210.0	185.0	35.0
TPS22976NDPUR	WSON	DPU	14	3000	210.0	185.0	35.0
TPS22976NDPUT	WSON	DPU	14	250	210.0	185.0	35.0
TPS22976NDPUT	WSON	DPU	14	250	210.0	185.0	35.0

DPU (R-PWSON-N14) PLASTIC SMALL OUTLINE NO-LEAD



4211321/B 11/10

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. Small Outline No-Lead (SON) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
- E. This package is Pb-free.

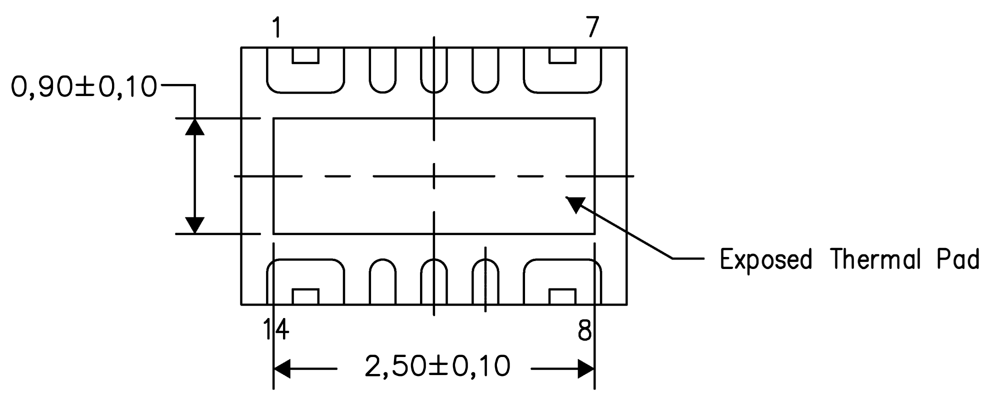
DPU (R-PWSON-N14) PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



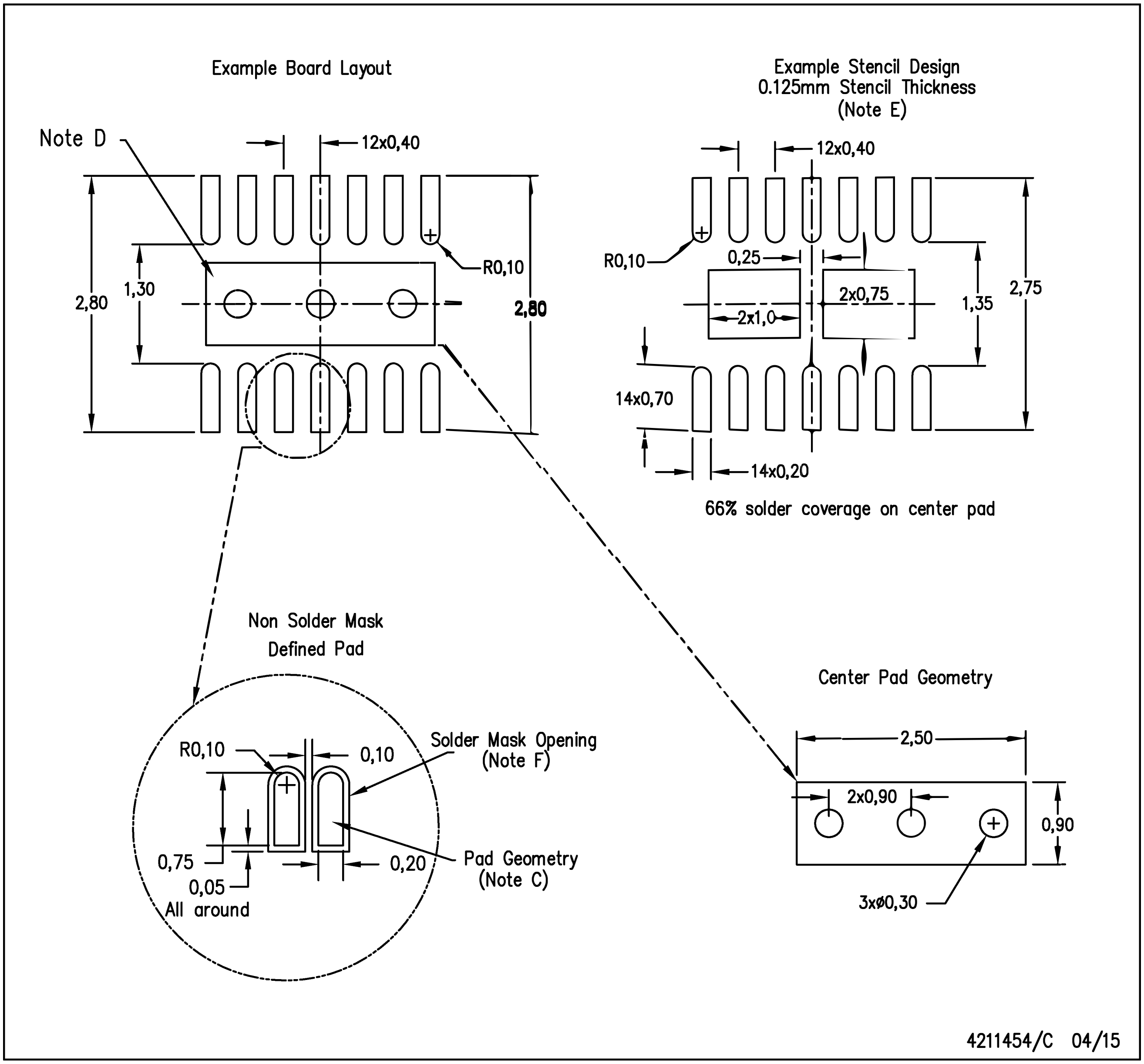
Bottom View

Exposed Thermal Pad Dimensions

4211395/C 04/15

NOTE: All linear dimensions are in millimeters

DPU (R–PWSON–N14) PLASTIC SMALL OUTLINE NO–LEAD



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Publication IPC–7351 is recommended for alternate designs.

D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.

E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.

F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.