TC4423A/TC4424A/TC4425A

3A Dual High-Speed Power MOSFET Drivers

Features

- High Peak Output Current: 4.5A (typical)
- Wide Input Supply Voltage Operating Range:
  - 4.5V to 18V
- High Capacitive Load Drive Capability:
  - 1800 pF in 12 ns
- Short Delay Times: 40 ns (typical)
- Matched Rise/Fall Times
- Low Supply Current:
  - With Logic '1' Input – 1.0 mA (maximum)
  - With Logic '0' Input – 150 µA (maximum)
- Low Output Impedance: 2.5Ω (typical)
- Latch-Up Protected: Will Withstand 1.5A Reverse Current
- Logic Input Will Withstand Negative Swing Up To 5V
- Pin compatible with the TC4423/TC4424/TC4425 and TC4426A/TC4427A/TC4428A devices
- Space-saving 8-Pin 150 mil body SOIC and 8-Pin 6x5 DFN Packages

Applications

- Switch Mode Power Supplies
- Pulse Transformer Drive
- Line Drivers
- Direct Drive of Small DC Motors

General Description

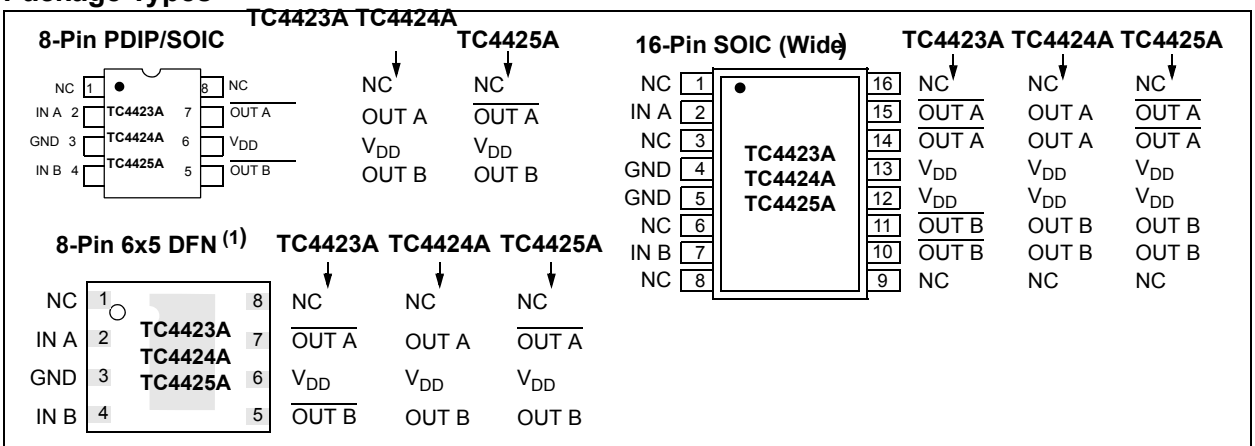
The TC4423A/TC4424A/TC4425A devices are a family of dual-output 3A buffers/MOSFET drivers. These devices are improved versions of the earlier TC4423/TC4424/TC4425 dual-output 3A driver family. This improved version features higher peak output current drive capability, lower shoot-throught current, matched rise/fall times and propagation delay times. The TC4423A/TC4424A/TC4425A devices are pin-compatible with the existing TC4423/TC4424/TC4425 family. An 8-pin SOIC package option has been added to the family. The 8-pin DFN package option offers increased power dissipation capability for driving heavier capacitive or resistive loads.

The TC4423A/TC4424A/TC4425A MOSFET drivers can easily charge and discharge 1800 pF gate capacitance in under 20 ns, provide low enough impedances in both the on and off states to ensure the MOSFET's intended state will not be affected, even by large transients.

The TC4423A/TC4424A/TC4425A inputs may be driven directly from either TTL or CMOS (2.4V to 18V). In addition, the 300 mV of built-in hysteresis provides noise immunity and allows the device to be driven from slow rising or falling waveforms.

The TC4423A/TC4424A/TC4425A dual-output 3A MOSFET driver family is offerd with a -40°C to +125°C temperature rating, making it useful in any wide temperature range application.

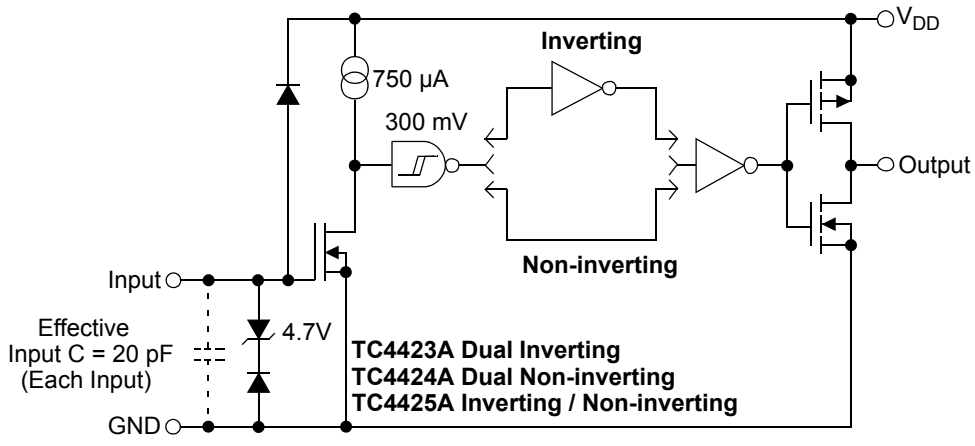
Package Types



Note 1: Exposed pad of the DFN package is electrically isolated.

2: Duplicate pins must both be connected for proper operation.

Functional Block Diagram(1)



Note 1: Unused inputs should be grounded.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage .....+20V
Input Voltage, IN A or IN B .....(V_{DD} + 0.3V) to (GND – 5V)
Package Power Dissipation (T_A=50°C)
8L PDIP 1.2W
8L SOIC..... 0.61W
16L SOIC.....1.1W
8L DFN ..... **Note 3**

† **Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS (NOTE 2)

Electrical Specifications: Unless otherwise indicated, T_A = +25°C, with 4.5V ≤ V_{DD} ≤ 18V.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input						
Logic '1', High Input Voltage	V_{IH}	2.4	1.5	—	V	
Logic '0', Low Input Voltage	V_{IL}	—	1.3	0.8	V	
Input Current	I_{IN}	–1	—	1	µA	0V ≤ V_{IN} ≤ V_{DD}
Input Voltage	V_{IN}	-5	—	V_{DD}+0.3	V	
Output						
High Output Voltage	V_{OH}	V_{DD} – 0.025	—	—	V	DC Test
Low Output Voltage	V_{OL}	—	—	0.025	V	DC Test
Output Resistance, High	R_{OH}	—	2.2	3.0	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Output Resistance, Low	R_{OL}	—	2.8	3.5	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Peak Output Current	I_{PK}	—	4.5	—	A	10V≤ V_{DD} ≤18V **(Note 2)**
Latch-Up Protection With-stand Reverse Current	I_{REV}	—	>1.5	—	A	Duty cycle ≤ 2%, t ≤ 300 µsec.
Switching Time (Note 1)						
Rise Time	t_R	—	12	21	ns	Figure 4-1, Figure 4-2, C_L = 1800 pF
Fall Time	t_F	—	12	21	ns	Figure 4-1, Figure 4-2, C_L = 1800 pF
Delay Time	t_{D1}	—	40	48	ns	Figure 4-1, Figure 4-2, C_L = 1800 pF
Delay Time	t_{D2}	—	41	48	ns	Figure 4-1, Figure 4-2, C_L = 1800 pF
Power Supply						
Supply Voltage	V_{DD}	4.5	—	18	V	
Power Supply Current	I_S	—	1.0	2.0	mA	V_{IN} = 3V (Both inputs)
	I_S	—	0.15	0.25	mA	V_{IN} = 0V (Both inputs)

Note 1: Switching times ensured by design.
2: Tested during characterization, not production tested.
3: Package power dissipation is dependent on the copper pad area on the PCB.

DC CHARACTERISTICS (OVER OPERATING TEMPERATURE RANGE)

Electrical Specifications: Unless otherwise indicated, operating temperature range with 4.5V ≤ V_{DD} ≤ 18V.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input						
Logic '1', High Input Voltage	V_{IH}	2.4	—	—	V	
Logic '0', Low Input Voltage	V_{IL}	—	—	0.8	V	
Input Current	I_{IN}	–10	—	+10	µA	0V ≤ V_{IN} ≤ V_{DD}
Output						
High Output Voltage	V_{OH}	V_{DD} – 0.025	—	—	V	
Low Output Voltage	V_{OL}	—	—	0.025	V	
Output Resistance, High	R_{OH}	—	3.1	6	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Output Resistance, Low	R_{OL}	—	3.7	7	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Switching Time (Note 1)						
Rise Time	t_R	—	20	31	ns	Figure 4-1, Figure 4-2, C_L = 1800 pF
Fall Time	t_F	—	22	31	ns	Figure 4-1, Figure 4-2, C_L = 1800 pF
Delay Time	t_{D1}	—	50	66	ns	Figure 4-1, Figure 4-2, C_L = 1800 pF
Delay Time	t_{D2}	—	50	66	ns	Figure 4-1, Figure 4-2, C_L = 1800 pF
Power Supply						
Power Supply Current	I_S	— —	2.0 0.2	3.0 0.3	mA	V_{IN} = 3V (Both inputs) V_{IN} = 0V (Both inputs)

Note 1: Switching times ensured by design.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, all parameters apply with 4.5V ≤ V_{DD} ≤ 18V.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Specified Temperature Range (V)	T_A	–40	—	+125	°C	
Maximum Junction Temperature	T_J	—	—	+150	°C	
Storage Temperature Range	T_A	–65	—	+150	°C	
Package Thermal Resistances						
Thermal Resistance, 8L-6x5 DFN	θ_{JA}	—	33.2	—	°C/W	Typical four-layer board with vias to ground plane
Thermal Resistance, 8L-PDIP	θ_{JA}	—	84.6	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	163	—	°C/W	
Thermal Resistance, 16L-SOIC	θ_{JA}	—	90	—	°C/W	

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C with 4.5V <= V_{DD} <= 18V.

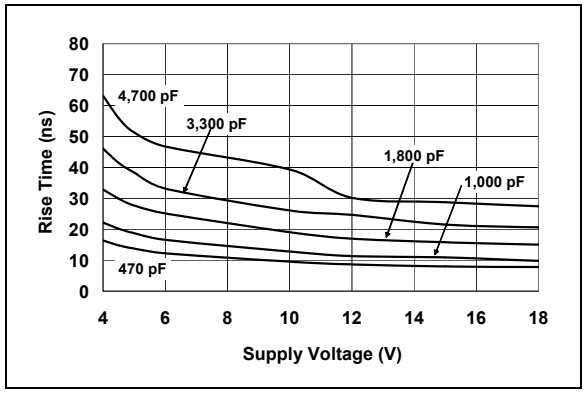


FIGURE 2-1: *Rise Time vs. Supply Voltage.*

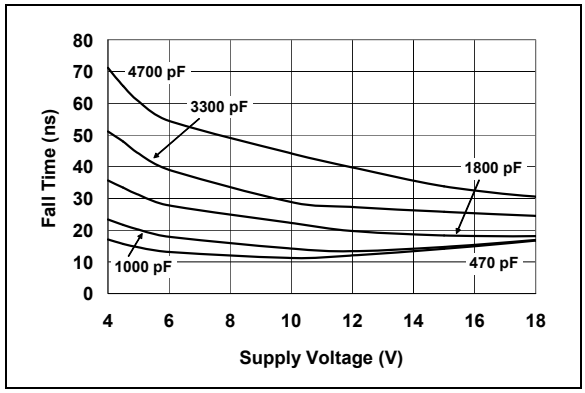


FIGURE 2-4: *Fall Time vs. Supply Voltage.*

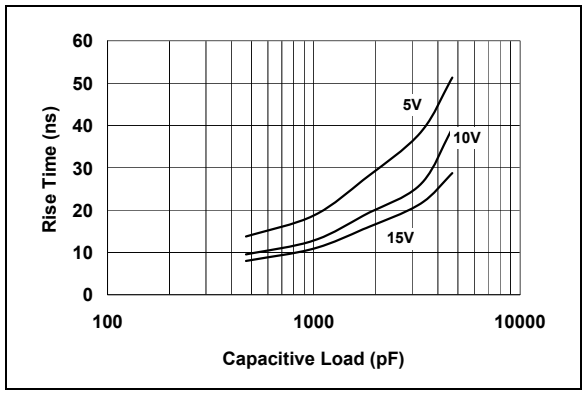


FIGURE 2-2: *Rise Time vs. Capacitive Load.*

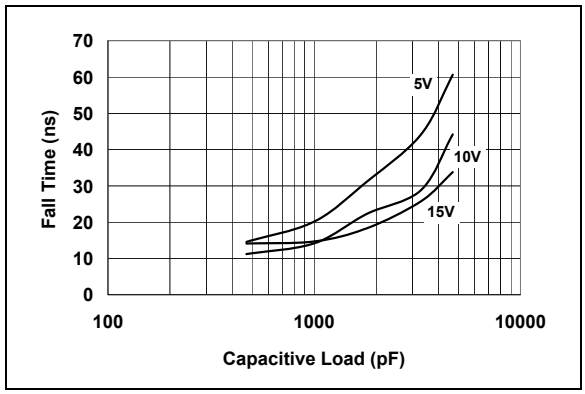


FIGURE 2-5: *Fall Time vs. Capacitive Load.*

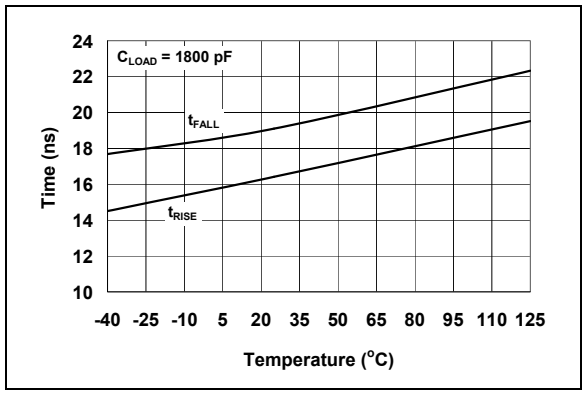


FIGURE 2-3: *Rise and Fall Times vs. Temperature.*

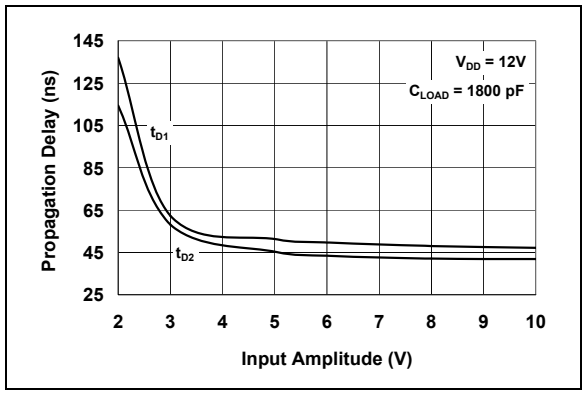


FIGURE 2-6: *Propagation Delay vs. Input Amplitude.*

Typical Performance Curves (Continued)

Note: Unless otherwise indicated, T_A = +25°C with 4.5V <= V_{DD} <= 18V.

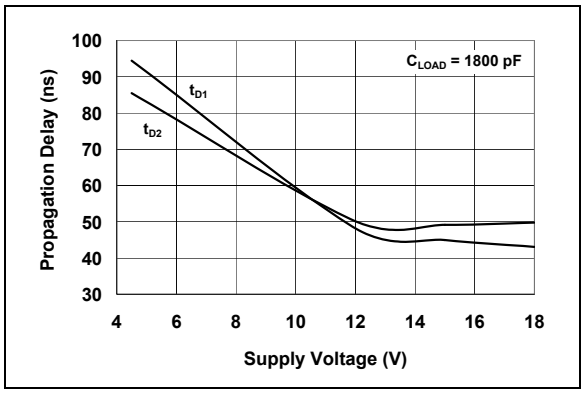


FIGURE 2-7: *Propagation Delay Time vs. Supply Voltage.*

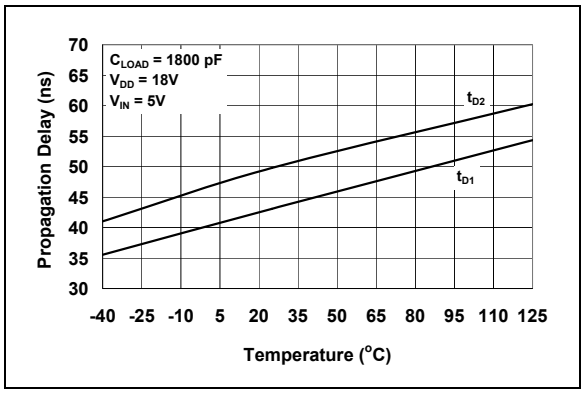


FIGURE 2-10: *Propagation Delay Time vs. Temperature.*

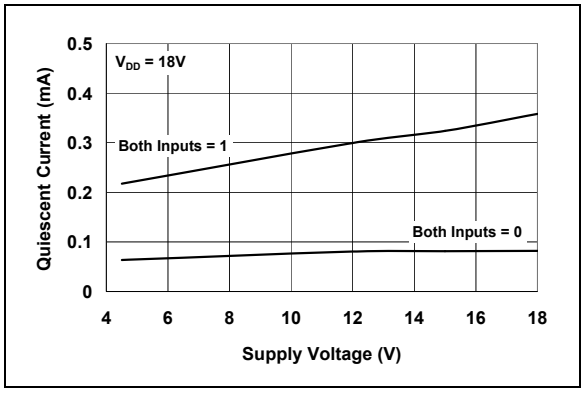


FIGURE 2-8: *Quiescent Current vs. Supply Voltage.*

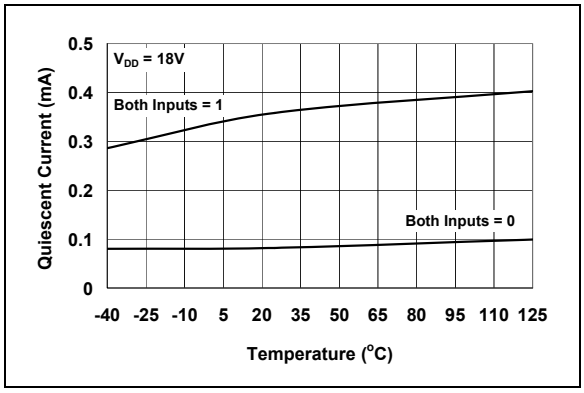


FIGURE 2-11: *Quiescent Current vs. Temperature.*

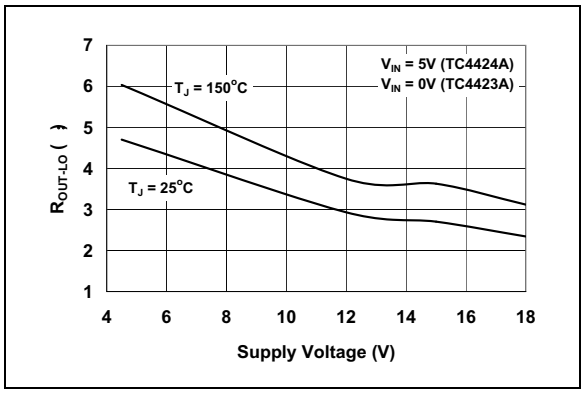


FIGURE 2-9: *Output Resistance (Output Low) vs. Supply Voltage.*

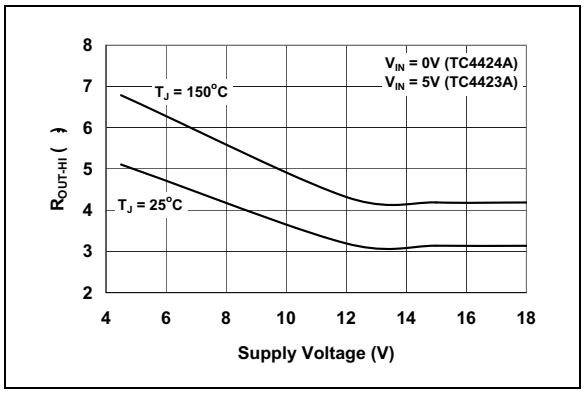


FIGURE 2-12: *Output Resistance (Output High) vs. Supply Voltage.*

Typical Performance Curves (Continued)

Note: Unless otherwise indicated, T_A = +25°C with 4.5V <= V_{DD} <= 18V.

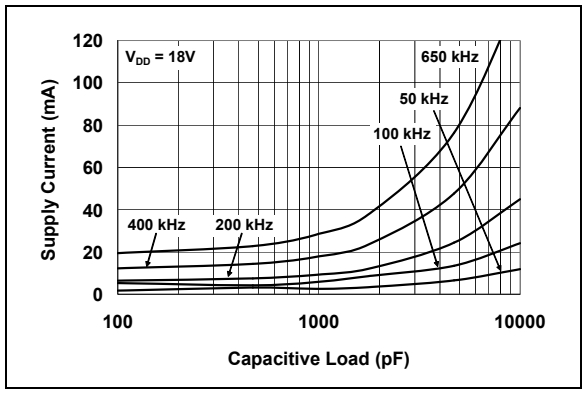


FIGURE 2-13: *Supply Current vs. Capacitive Load.*

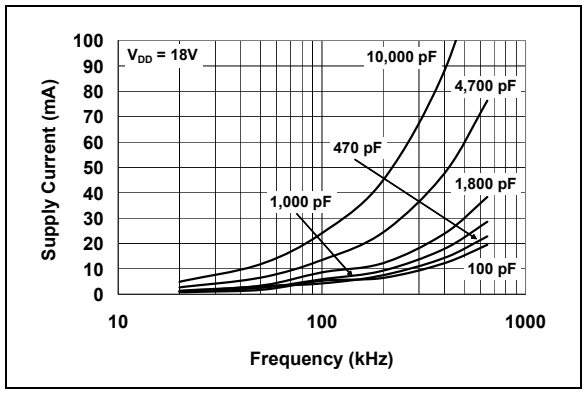


FIGURE 2-16: *Supply Current vs. Frequency.*

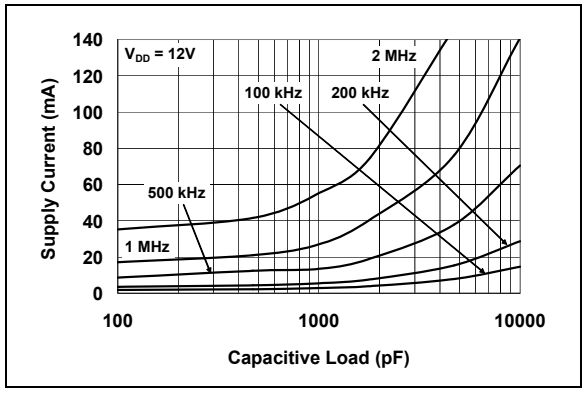


FIGURE 2-14: *Supply Current vs. Capacitive Load.*

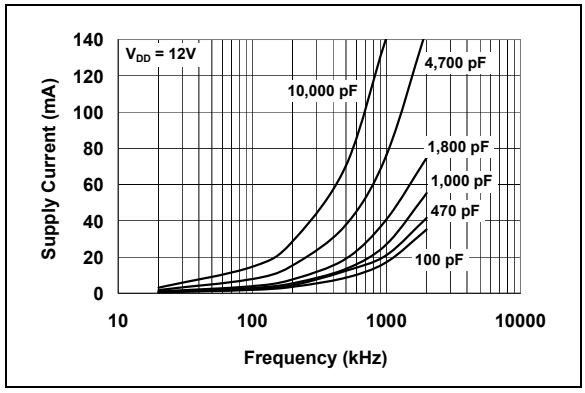


FIGURE 2-17: *Supply Current vs. Frequency.*

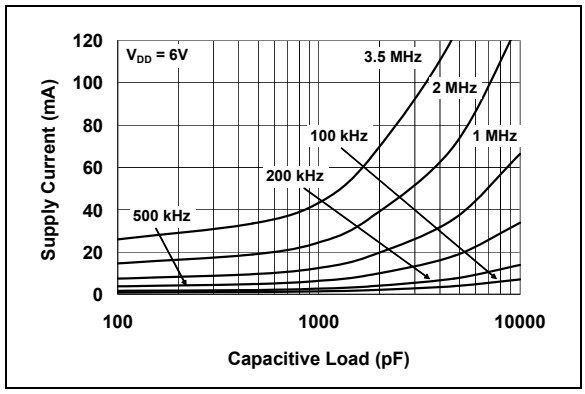


FIGURE 2-15: *Supply Current vs. Capacitive Load.*

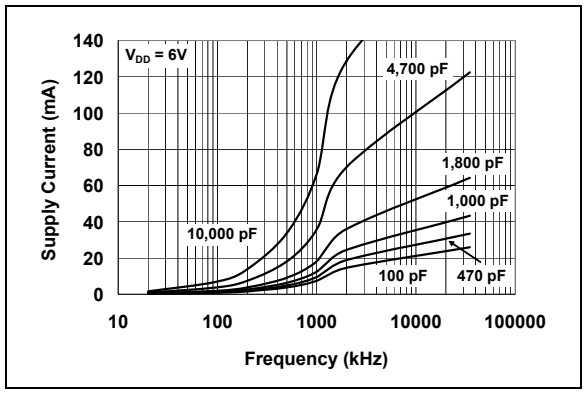
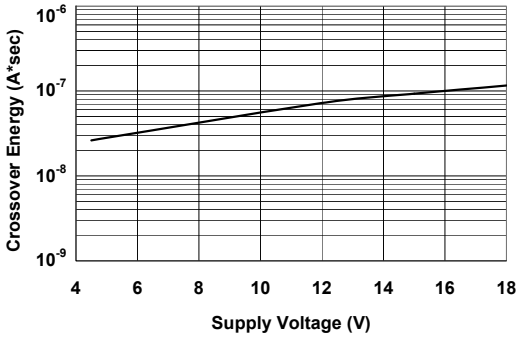


FIGURE 2-18: *Supply Current vs. Frequency.*

Typical Performance Curves (Continued)

Note: Unless otherwise indicated, T_A = +25°C with 4.5V <= V_{DD} <= 18V.



Note: The values on this graph represents the loss seen by both drivers in a package during one complete cycle. For a single driver, divide the stated values by 2. For a single transition of a single driver, divide the stated value by 4.

FIGURE 2-19: Crossover Energy vs. Supply Voltage.

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE [1]

8-Pin PDIP	8-Pin DFN	16-Pin SOIC (Wide)	Symbol	Description
1	1	1	NC	No connection
2	2	2	IN A	Input A
—	—	3	NC	No connection
3	3	4	GND	Ground
—	—	5	GND	Ground
—	—	6	NC	No connection
4	4	7	IN B	Input B
—	—	8	NC	No connection
—	—	9	NC	No connection
5	5	10	OUT B	Output B
—	—	11	OUT B	Output B
6	6	12	V_{DD}	Supply input
—	—	13	V_{DD}	Supply input
7	7	14	OUT A	Output A
—	—	15	OUT A	Output A
8	8	16	NC	No connection
—	PAD	—	NC	Exposed Metal Pad

Note 1: Duplicate pins must be connected for proper operation.

3.1 Inputs A and B

Inputs A and B are TTL/CMOS compatible inputs that control outputs A and B, respectively. These inputs have 300 mV of hysteresis between the high and low input levels, allowing them to be driven from slow rising and falling signals, and to provide noise immunity.

3.2 Outputs A and B

Outputs A and B are CMOS push-pull outputs that are capable of sourcing and sinking 3A peaks of current (V_{DD} = 18V). The low output impedance ensures the gate of the external MOSFET will stay in the intended state even during large transients. These outputs also have a reverse current latch-up rating of 1.5A.

3.3 Supply Input (V_{DD})

V_{DD} is the bias supply input for the MOSFET driver and has a voltage range of 4.5V to 18V. This input must be decoupled to ground with a local ceramic capacitor. This bypass capacitor provides a localized low-impedance path for the peak currents that are to be provided to the load.

3.4 Ground (GND)

Ground is the device return pin. The ground pin should have a low-impedance connection to the bias supply source return. High peak currents will flow out the ground pin when the capacitive load is being discharged.

3.5 Exposed Metal Pad

The exposed metal pad of the DFN package is not internally connected to any potential. Therefore, this pad can be connected to a ground plane or other copper plane on a printed circuit board to aid in heat removal from the package.

4.0 APPLICATIONS INFORMATION

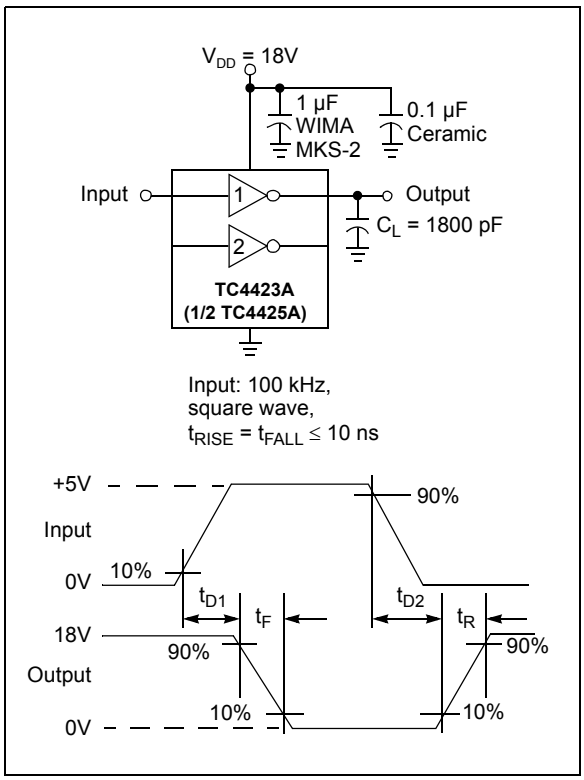


FIGURE 4-1: *Inverting Driver Switching Time.*

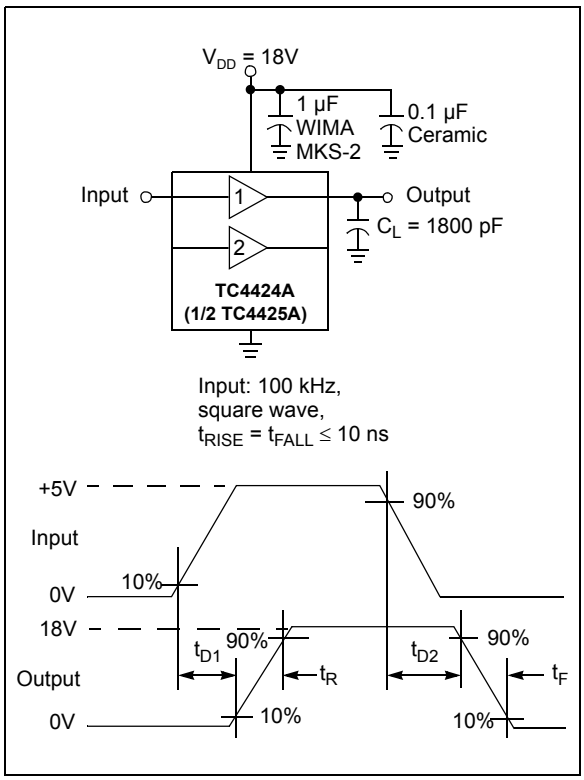
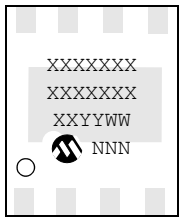


FIGURE 4-2: *Non-inverting Driver Switching Time.*

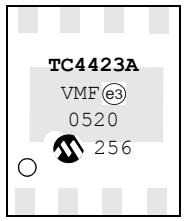
5.0 PACKAGING INFORMATION

5.1 Package Marking Information (Not to Scale)

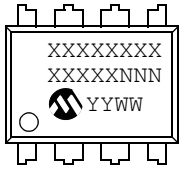
8-Lead DFN (6x5)



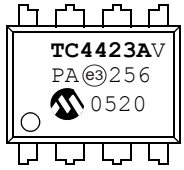
Example:



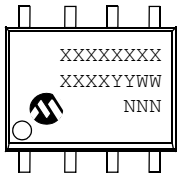
8-Lead PDIP (300 mil)



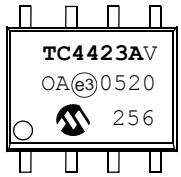
Example:



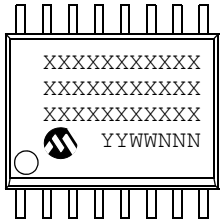
8-Lead SOIC (150 mil)



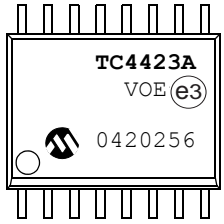
Example:



16-Lead SOIC (300 mil)



Example:

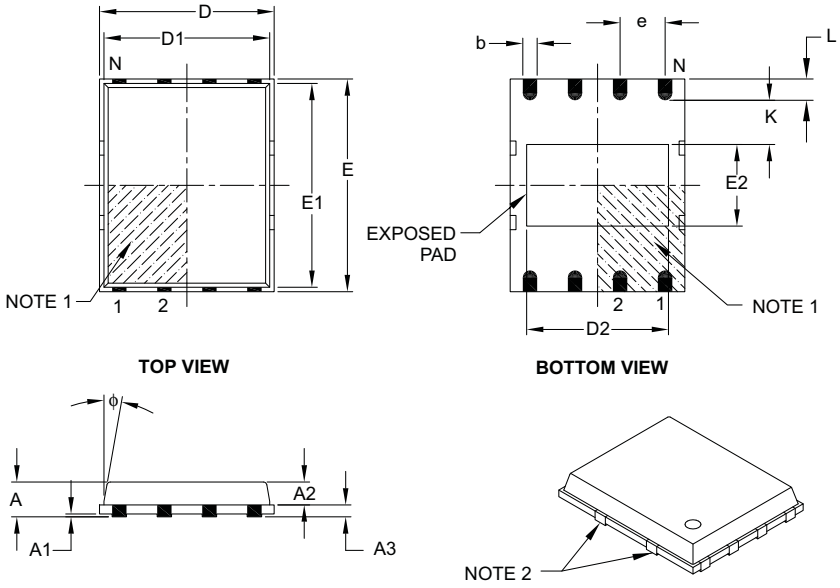


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Dual Flat, No Lead Package (MF) – 6x5 mm Body [DFN-S] PUNCH SINGULATED

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	0.85	1.00
Molded Package Thickness	A2	–	0.65	0.80
Standoff	A1	0.00	0.01	0.05
Base Thickness	A3		0.20 REF	
Overall Length	D		4.92 BSC	
Molded Package Length	D1		4.67 BSC	
Exposed Pad Length	D2	3.85	4.00	4.15
Overall Width	E		5.99 BSC	
Molded Package Width	E1		5.74 BSC	
Exposed Pad Width	E2	2.16	2.31	2.46
Contact Width	b	0.35	0.40	0.47
Contact Length	L	0.50	0.60	0.75
Contact-to-Exposed Pad	K	0.20	–	–
Model Draft Angle Top	ϕ	–	–	12°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Dimensioning and tolerancing per ASME Y14.5M.

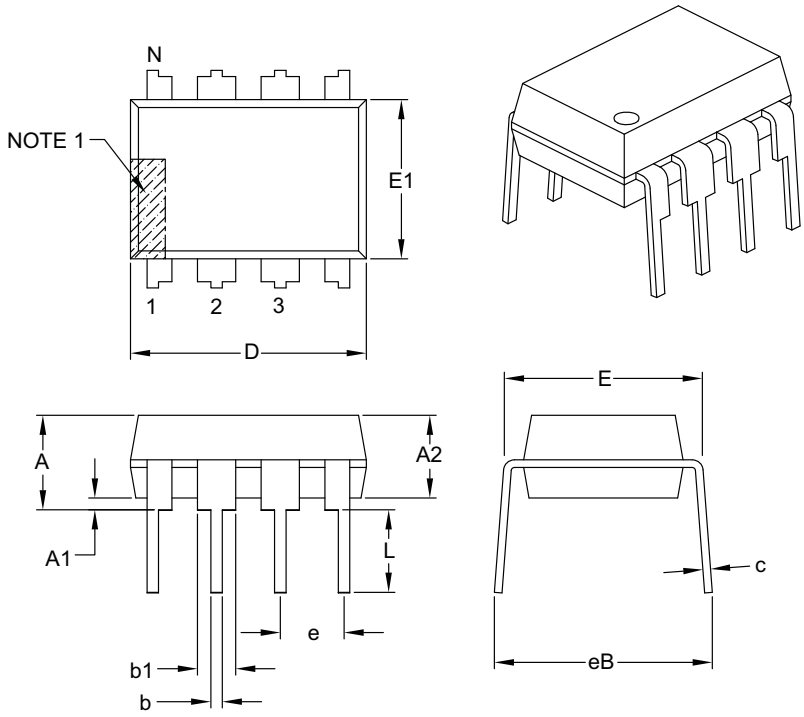
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-113B

8-Lead Plastic Dual In-Line (PA) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

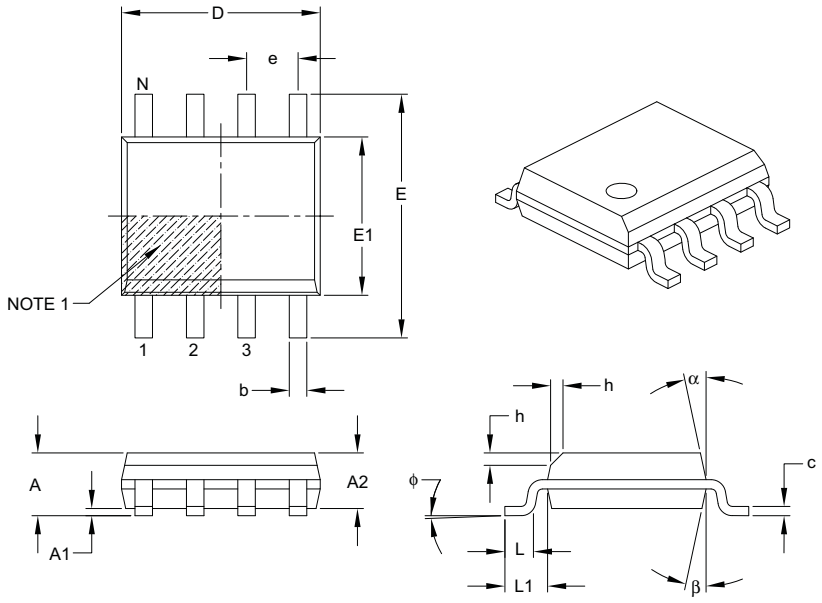
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

8-Lead Plastic Small Outline (OA) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

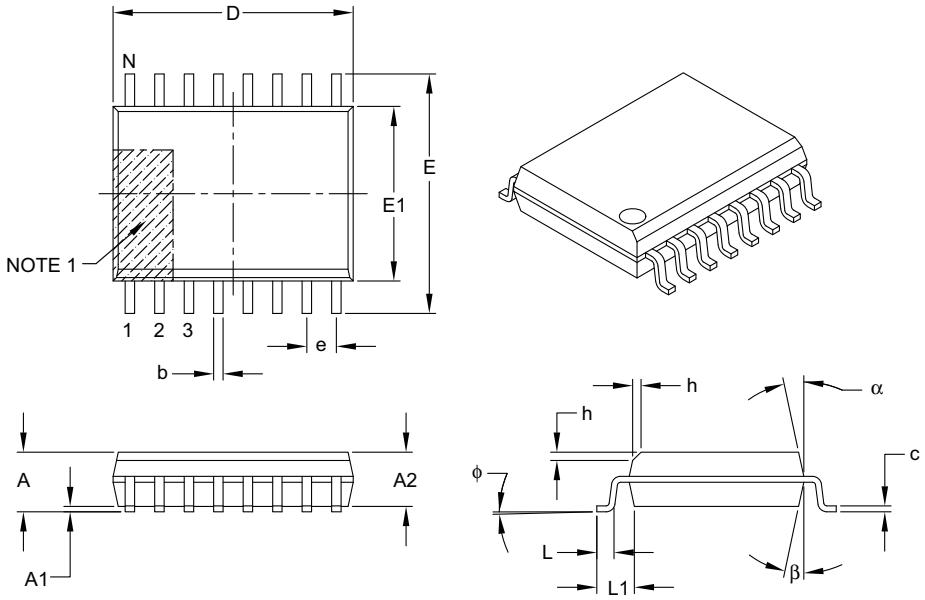
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

16-Lead Plastic Small Outline (OE) – Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		16	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	2.65
Molded Package Thickness	A2	2.05	–	–
Standoff §	A1	0.10	–	0.30
Overall Width	E		10.30 BSC	
Molded Package Width	E1		7.50 BSC	
Overall Length	D		10.30 BSC	
Chamfer (optional)	h	0.25	–	0.75
Foot Length	L	0.40	–	1.27
Footprint	L1		1.40 REF	
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.20	–	0.33
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-102B

APPENDIX A: REVISION HISTORY

Revision B (April 2007)

- Correct numerous errors throughout document.
- Page 3: Added Package Power Dissipation information about DC Characteristic Table.
- Page 3: Added Note 3 to DC Characteristic Table.
- Page 4: Changed Thermal Resistance for 8L-PDIP device from 125 to 84.6.
  Changed Thermal Resistance for 8L-SOIC from 155 to 163.
- Page 12: Updated Package Outline Drawing.
- Page 13: Updated Package Outline Drawing.
- Page 14: Updated Package Outline Drawing.
- Page 15: Added 16-Lead SOIC Package Outline Drawing
- Page 17: Updated Revision History.

Revision A (June 2006)

- Original Release of this Document.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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