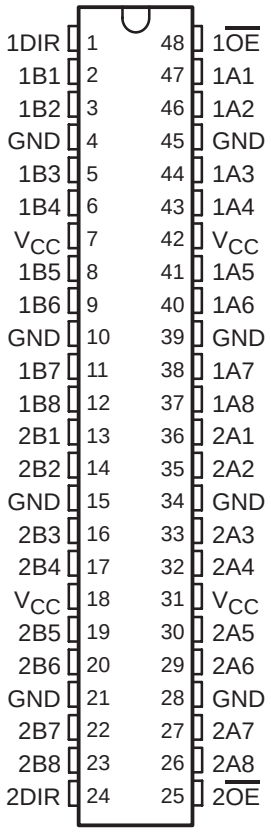
- **State-of-the-Art Advanced BiCMOS Technology (ABT) Widebus™ Design for 2.5-V and 3.3-V Operation and Low Static-Power Dissipation**
- **Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 2.3-V to 3.6-V $V_{CC}$)**
- **Typical $V_{OLP}$ (Output Ground Bounce) <0.8 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C**
- **High Drive (−32/64 mA at 3.3-V $V_{CC}$)**
- **$I_{off}$ and Power-Up 3-State Support Hot Insertion**
- **Use Bus Hold on Data Inputs in Place of External Pullup/Pulldown Resistors to Prevent the Bus From Floating**
- **Flow-Through Architecture Facilitates Printed Circuit Board Layout**
- **Distributed $V_{CC}$ and GND Pins Minimize High-Speed Switching Noise**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**

**SN54ALVTH16245 . . . WD PACKAGE**
**SN74ALVTH16245 . . . DGG, DGV, OR DL PACKAGE**
**(TOP VIEW)**




## description

The ’ALVTH16245 devices are 16-bit (dual-octal) noninverting 3-state transceivers designed for 2.5-V or 3.3-V $V_{CC}$ operation, but with the capability to provide a TTL interface to a 5-V system environment.

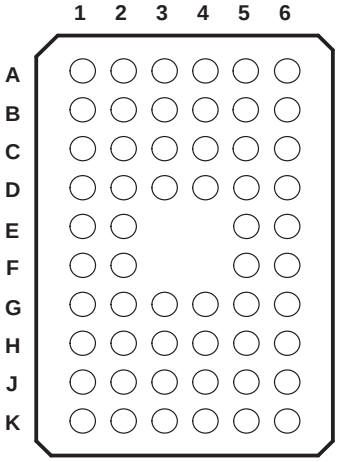
These devices can be used as two 8-bit transceivers or one 16-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

These devices are fully specified for hot-insertion applications using $I_{off}$ and power-up 3-state. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When $V_{CC}$ is between 0 and 1.2 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.2 V, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

**SN74ALVTH16245 . . . GQL PACKAGE**
**(TOP VIEW)**




## terminal assignments

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| A | 1DIR | NC | NC | NC | NC | $1\overline{OE}$ |
| B | 1B2 | 1B1 | GND | GND | 1A1 | 1A2 |
| C | 1B4 | 1B3 | $V_{CC}$ | $V_{CC}$ | 1A3 | 1A4 |
| D | 1B6 | 1B5 | GND | GND | 1A5 | 1A6 |
| E | 1B8 | 1B7 | | | 1A7 | 1A8 |
| F | 2B1 | 2B2 | | | 2A2 | 2A1 |
| G | 2B3 | 2B4 | GND | GND | 2A4 | 2A3 |
| H | 2B5 | 2B6 | $V_{CC}$ | $V_{CC}$ | 2A6 | 2A5 |
| J | 2B7 | 2B8 | GND | GND | 2A8 | 2A7 |
| K | 2DIR | NC | NC | NC | NC | $2\overline{OE}$ |

NC − No internal connection

## ORDERING INFORMATION

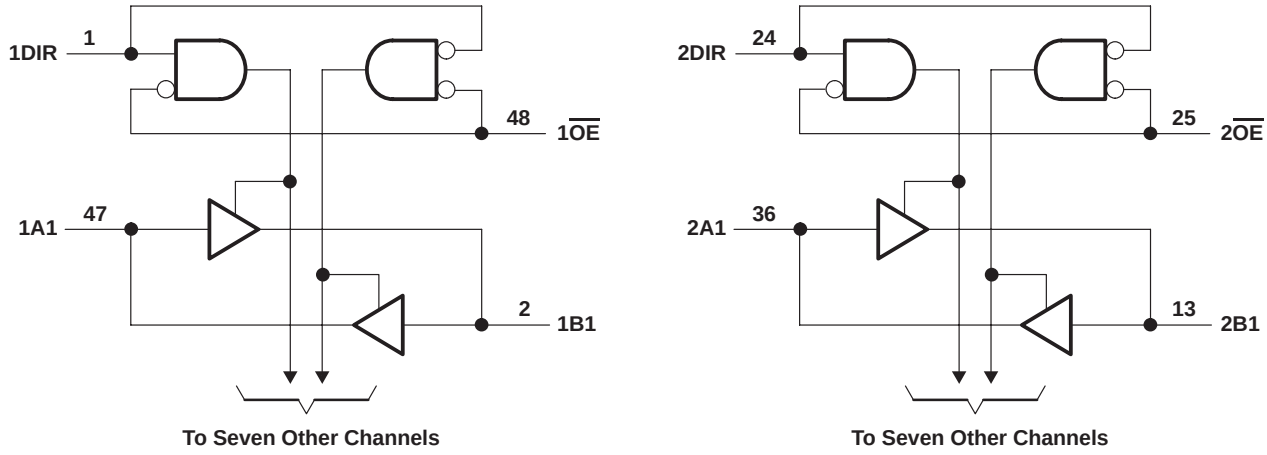
| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| −40°C to 85°C | SSOP − DL | Tape and reel | SN74ALVTH16245DLR | ALVTH16245 |
| | TSSOP − DGG | Tape and reel | SN74ALVTH16245GR | ALVTH16245 |
| | TVSOP − DGV | Tape and reel | SN74ALVTH16245VR | VT245 |
| | VFBGA − GQL | Tape and reel | SN74ALVTH16245QR | |
| −55°C to 125°C | CFP − WD | Tube | SNJ54ALVTH16245WD | SNJ54ALVTH16245WD |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

**FUNCTION TABLE**
**(each 8-bit section)**

| INPUTS | | OPERATION |
|---|---|---|
| $\overline{OE}$ | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

## logic diagram (positive logic)




Pin numbers shown are for the DGG, DGV, DL, and WD packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . −0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) . . . . . −0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, $V_O$ (see Note 1) . . . . . −0.5 V to 7 V
Output current in the low state, $I_O$: SN54ALVTH16245 . . . . . 96 mA
SN74ALVTH16245 . . . . . 128 mA
Output current in the high state, $I_O$: SN54ALVTH16245 . . . . . −48 mA
SN74ALVTH16245 . . . . . −64 mA
Input clamp current, $I_{IK}$ ($V_I < 0$) . . . . . −50 mA
Output clamp current, $I_{OK}$ ($V_O < 0$) . . . . . −50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package . . . . . 70°C/W
DGV package . . . . . 58°C/W
DL package . . . . . 63°C/W
GQL package . . . . . 42°C/W
Storage temperature range, $T_{stg}$ . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions, $V_{CC}$ = 2.5 V ± 0.2 V (see Note 3)

| | | | SN54ALVTH16245 | | | SN74ALVTH16245 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{CC}$ | Supply voltage | | 2.3 | | 2.7 | 2.3 | | 2.7 | V |
| $V_{IH}$ | High-level input voltage | | 1.7 | | | 1.7 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.7 | | | 0.7 | V |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | 5.5 | 0 | $V_{CC}$ | 5.5 | V |
| $I_{OH}$ | High-level output current | | | | −6 | | | −8 | mA |
| $I_{OL}$ | Low-level output current | | | | 6 | | | 8 | mA |
| | Low-level output current; current duty cycle ≤ 50%; f ≥ 1 kHz | | | | 18 | | | 24 | |
| Δt/Δv | Input transition rise or fall rate | Outputs enabled | | | 10 | | | 10 | ns/V |
| $\Delta t/\Delta V_{CC}$ | Power-up ramp rate | | 200 | | | 200 | | | µs/V |
| $T_A$ | Operating free-air temperature | | −55 | | 125 | −40 | | 85 | °C |



NOTE 3: All unused control inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## recommended operating conditions, $V_{CC}$ = 3.3 V ± 0.3 V (see Note 3)

| | | | SN54ALVTH16245 | | | SN74ALVTH16245 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{CC}$ | Supply voltage | | 3 | | 3.6 | 3 | | 3.6 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | | | 0.8 | V |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | 5.5 | 0 | $V_{CC}$ | 5.5 | V |
| $I_{OH}$ | High-level output current | | | | −24 | | | −32 | mA |
| $I_{OL}$ | Low-level output current | | | | 24 | | | 32 | mA |
| | Low-level output current; current duty cycle ≤ 50%; f ≥ 1 kHz | | | | 48 | | | 64 | |
| Δt/Δv | Input transition rise or fall rate | Outputs enabled | | | 10 | | | 10 | ns/V |
| $\Delta t/\Delta V_{CC}$ | Power-up ramp rate | | 200 | | | 200 | | | µs/V |
| $T_A$ | Operating free-air temperature | | −55 | | 125 | −40 | | 85 | °C |



NOTE 3: All unused control inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range, $V_{CC}$ = 2.5 V ± 0.2 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54ALVTH16245 | | | SN74ALVTH16245 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 2.3 V, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 2.3 V to 2.7 V, | $I_{OH}$ = −100 µA | $V_{CC}$−0.2 | | | $V_{CC}$−0.2 | | | V |
| | | $V_{CC}$ = 2.3 V | $I_{OH}$ = −6 mA | 1.8 | | | | | | |
| | | | $I_{OH}$ = −8 mA | | | | 1.8 | | | |
| $V_{OL}$ | | $V_{CC}$ = 2.3 V to 2.7 V, | $I_{OL}$ = 100 µA | | | 0.2 | | | 0.2 | V |
| | | $V_{CC}$ = 2.3 V | $I_{OL}$ = 6 mA | | | 0.4 | | | | |
| | | | $I_{OL}$ = 8 mA | | | | | | 0.4 | |
| | | | $I_{OL}$ = 18 mA | | | 0.5 | | | | |
| | | | $I_{OL}$ = 24 mA | | | | | | 0.5 | |
| $I_I$ | Control inputs | $V_{CC}$ = 2.7 V, | $V_I$ = $V_{CC}$ or GND | | | ±1 | | | ±1 | µA |
| | | $V_{CC}$ = 0 or 2.7 V, | $V_I$ = 5.5 V | | | 10 | | | 10 | |
| | A or B ports | $V_{CC}$ = 2.7 V | $V_I$ = 5.5 V | | | 20 | | | 20 | |
| | | | $V_I$ = $V_{CC}$ | | | 1 | | | 1 | |
| | | | $V_I$ = 0 | | | −5 | | | −5 | |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_I$ or $V_O$ = 0 to 4.5 V | | | | | | ±100 | µA |
| $I_{BHL}$‡ | | $V_{CC}$ = 2.3 V, | $V_I$ = 0.7 V | | 115 | | | 115 | | µA |
| $I_{BHH}$§ | | $V_{CC}$ = 2.3 V, | $V_I$ = 1.7 V | | −10 | | | −10 | | µA |
| $I_{BHLO}$¶ | | $V_{CC}$ = 2.7 V, | $V_I$ = 0 to $V_{CC}$ | 300 | | | 300 | | | µA |
| $I_{BHHO}$# | | $V_{CC}$ = 2.7 V, | $V_I$ = 0 to $V_{CC}$ | −300 | | | −300 | | | µA |
| $I_{EX}$‖ | | $V_{CC}$ = 2.3 V, | $V_O$ = 5.5 V | | | 125 | | | 125 | µA |
| $I_{OZ(PU/PD)}$☆ | | $V_{CC}$ ≤ 1.2 V, $V_O$ = 0.5 V to $V_{CC}$, $V_I$ = GND or $V_{CC}$, $\overline{OE}$ = don't care | | | | ±100 | | | ±100 | µA |
| $I_{CC}$ | | $V_{CC}$ = 2.7 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | Outputs high | | 0.04 | 0.1 | | 0.04 | 0.1 | mA |
| | | | Outputs low | | 2.3 | 4.5 | | 2.3 | 4.5 | |
| | | | Outputs disabled | | 0.04 | 0.1 | | 0.04 | 0.1 | |
| $C_i$ | | $V_{CC}$ = 2.5 V, | $V_I$ = 2.5 V or 0 | | 3.5 | | | 3.5 | | pF |
| $C_{io}$ | | $V_{CC}$ = 2.5 V, | $V_O$ = 2.5 V or 0 | | 8 | | | 8 | | pF |



† All typical values are at $V_{CC}$ = 2.5 V, $T_A$ = 25°C.
‡ The bus-hold circuit can sink at least the minimum low sustaining current at $V_{IL}$ max. $I_{BHL}$ should be measured after lowering $V_{IN}$ to GND and then raising it to $V_{IL}$ max.
§ The bus-hold circuit can source at least the minimum high sustaining current at $V_{IH}$ min. $I_{BHH}$ should be measured after raising $V_{IN}$ to $V_{CC}$ and then lowering it to $V_{IH}$ min.
¶ An external driver must source at least $I_{BHLO}$ to switch this node from low to high.
# An external driver must sink at least $I_{BHHO}$ to switch this node from high to low.
‖ Current into an output in the high state when $V_O$ > $V_{CC}$
☆ High-impedance state during power up or power down

## electrical characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54ALVTH16245 | | | SN74ALVTH16245 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 3 V, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 3 V to 3.6 V, | $I_{OH}$ = −100 µA | $V_{CC}$−0.2 | | | $V_{CC}$−0.2 | | | V |
| | | $V_{CC}$ = 3 V | $I_{OH}$ = −24 mA | 2 | | | | | | |
| | | | $I_{OH}$ = −32 mA | | | | 2 | | | |
| $V_{OL}$ | | $V_{CC}$ = 3 V to 3.6 V, | $I_{OL}$ = 100 µA | | | 0.2 | | | 0.2 | V |
| | | $V_{CC}$ = 3 V | $I_{OL}$ = 16 mA | | | | | | 0.4 | |
| | | | $I_{OL}$ = 24 mA | | | 0.5 | | | | |
| | | | $I_{OL}$ = 32 mA | | | | | | 0.5 | |
| | | | $I_{OL}$ = 48 mA | | | 0.55 | | | | |
| | | | $I_{OL}$ = 64 mA | | | | | | 0.55 | |
| $I_I$ | Control inputs | $V_{CC}$ = 3.6 V, | $V_I$ = $V_{CC}$ or GND | | | ±1 | | | ±1 | µA |
| | | $V_{CC}$ = 0 or 3.6 V, | $V_I$ = 5.5 V | | | 10 | | | 10 | |
| | A or B ports | $V_{CC}$ = 3.6 V | $V_I$ = 5.5 V | | | 20 | | | 20 | |
| | | | $V_I$ = $V_{CC}$ | | | 1 | | | 1 | |
| | | | $V_I$ = 0 | | | −5 | | | −5 | |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_I$ or $V_O$ = 0 to 4.5 V | | | | | | ±100 | µA |
| $I_{BHL}$‡ | | $V_{CC}$ = 3 V, | $V_I$ = 0.8 V | 75 | | | 75 | | | µA |
| $I_{BHH}$§ | | $V_{CC}$ = 3 V, | $V_I$ = 2 V | −75 | | | −75 | | | µA |
| $I_{BHLO}$¶ | | $V_{CC}$ = 3.6 V, | $V_I$ = 0 to $V_{CC}$ | 500 | | | 500 | | | µA |
| $I_{BHHO}$# | | $V_{CC}$ = 3.6 V, | $V_I$ = 0 to $V_{CC}$ | −500 | | | −500 | | | µA |
| $I_{EX}$‖ | | $V_{CC}$ = 3 V, | $V_O$ = 5.5 V | | | 125 | | | 125 | µA |
| $I_{OZ(PU/PD)}$☆ | | $V_{CC}$ ≤ 1.2 V, $V_O$ = 0.5 V to $V_{CC}$, $V_I$ = GND or $V_{CC}$, $\overline{OE}$ = don't care | | | | ±100 | | | ±100 | µA |
| $I_{CC}$ | | $V_{CC}$ = 3.6 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | Outputs high | | 0.07 | 0.1 | | 0.07 | 0.1 | mA |
| | | | Outputs low | | 3.2 | 5 | | 3.2 | 5 | |
| | | | Outputs disabled | | 0.07 | 0.1 | | 0.07 | 0.1 | |
| $\Delta I_{CC}$□ | | $V_{CC}$ = 3 V to 3.6 V, One input at $V_{CC}$ − 0.6 V, Other inputs at $V_{CC}$ or GND | | | | 0.2 | | | 0.2 | mA |
| $C_i$ | | $V_{CC}$ = 3.3 V, | $V_I$ = 3.3 V or 0 | | 3.5 | | | 3.5 | | pF |
| $C_{io}$ | | $V_{CC}$ = 3.3 V, | $V_O$ = 3.3 V or 0 | | 8 | | | 8 | | pF |



† All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
‡ The bus-hold circuit can sink at least the minimum low sustaining current at $V_{IL}$ max. $I_{BHL}$ should be measured after lowering $V_{IN}$ to GND and then raising it to $V_{IL}$ max.
§ The bus-hold circuit can source at least the minimum high sustaining current at $V_{IH}$ min. $I_{BHH}$ should be measured after raising $V_{IN}$ to $V_{CC}$ and then lowering it to $V_{IH}$ min.
¶ An external driver must source at least $I_{BHLO}$ to switch this node from low to high.
# An external driver must sink at least $I_{BHHO}$ to switch this node from high to low.
‖ Current into an output in the high state when $V_O$ > $V_{CC}$
☆ High-impedance state during power up or power down
□ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

**switching characteristics over recommended operating free-air temperature range, $C_L$ = 30 pF, $V_{CC}$ = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54ALVTH16245 | | SN74ALVTH16245 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | B or A | 0.5 | 3.6 | 0.5 | 3.6 | ns |
| $t_{PHL}$ | | | 0.5 | 3.4 | 0.5 | 3.4 | |
| $t_{PZH}$ | $\overline{OE}$ | A or B | 1.5 | 4.9 | 1.5 | 4.9 | ns |
| $t_{PZL}$ | | | 1 | 4 | 1 | 4 | |
| $t_{PHZ}$ | $\overline{OE}$ | A or B | 1.5 | 4.9 | 1.5 | 4.9 | ns |
| $t_{PLZ}$ | | | 1 | 4.2 | 1 | 4.2 | |



**switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54ALVTH16245 | | SN74ALVTH16245 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | B or A | 0.5 | 3.1 | 0.5 | 3.1 | ns |
| $t_{PHL}$ | | | 0.5 | 2.9 | 0.5 | 2.9 | |
| $t_{PZH}$ | $\overline{OE}$ | A or B | 1 | 4.2 | 1 | 4.2 | ns |
| $t_{PZL}$ | | | 1 | 3.5 | 1 | 3.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | A or B | 1.5 | 5.3 | 1.5 | 5.3 | ns |
| $t_{PLZ}$ | | | 1.5 | 5 | 1.5 | 5 | |



## skew

**$t_{ps}$ (pin or transition skew), $t_{ps} = |t_{PHL} - t_{PHL}|$**

| | $V_{CC}$ = 2.5 V | $V_{CC}$ = 3.3 V | UNIT |
|---|---|---|---|
| | TYP | TYP | |
| $t_{ps}$max | 438 | 118 | ps |

**$t_{OST} = |t_{p\Phi m} - t_{p\Phi n}|$, where $\Phi$ is any edge transition (high to low or low to high) measured between any two outputs (m or n) within any given device (see Note 4)**

| | | $V_{CC}$ = 2.5 V | $V_{CC}$ = 3.3 V | UNIT |
|---|---|---|---|---|
| | | TYP | TYP | |
| $t_{OST}$ | A–B | 227 | 248 | ps |
| | B–A | 223 | 243 | |

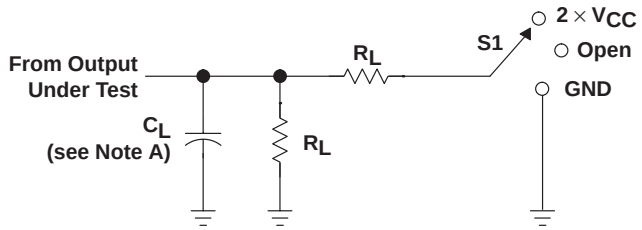
NOTE 4: One output switching, $T_A$ = 25°C

**$t_{OSHL}/t_{OSLH}$ (common edge skew), $t_{OSHL} = |t_{PHL}$max $- t_{PHL}$min$|$ (output skew for low-to-high transitions), and $t_{OSLH} = |t_{PLH}$max $- t_{PLH}$min$|$ (output skew for high-to-low transitions) (see Note 4)**

| | | $V_{CC}$ = 2.5 V | $V_{CC}$ = 3.3 V | UNIT |
|---|---|---|---|---|
| | | TYP | TYP | |
| $t_{OSLH}$ | A–B | 210 | 145 | ps |
| $t_{OSHL}$ | | 243 | 351 | |
| $t_{OSLH}$ | B–A | 207 | 136 | ps |
| $t_{OSHL}$ | | 238 | 350 | |

NOTE 4: One output switching, $T_A$ = 25°C

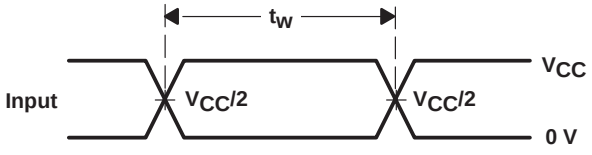
## PARAMETER MEASUREMENT INFORMATION



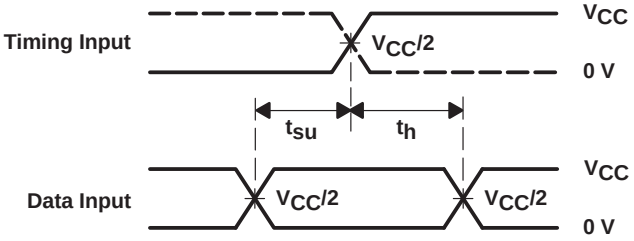

LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $2 \times V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

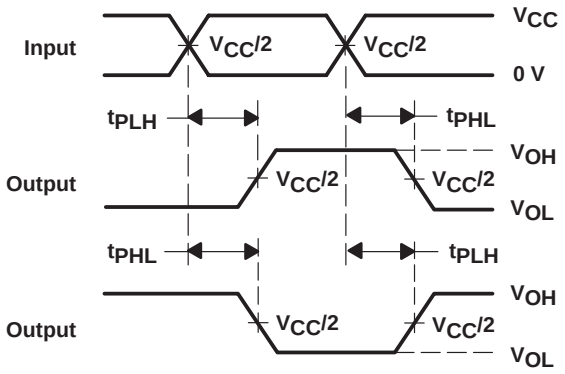
| $V_{CC}$ | $C_L$ | $R_L$ | $V_\Delta$ |
|---|---|---|---|
| 2.5 V ±0.2 V | 30 pF | 500 Ω | 0.15 V |
| 3.3 V ±0.3 V | 50 pF | 500 Ω | 0.3 V |



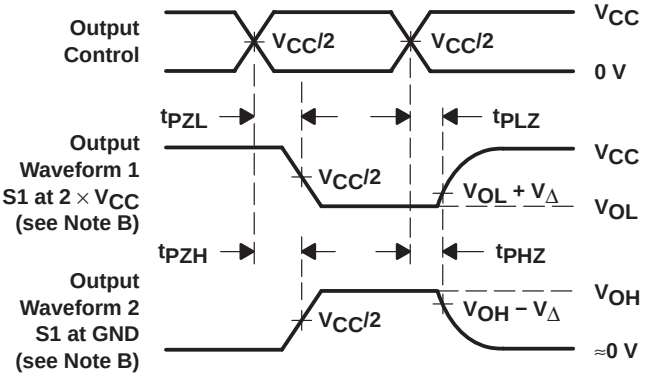

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2 ns, $t_f$ ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
H. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

# PACKAGE OPTION ADDENDUM

15-Jan-2021

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 74ALVTH16245GRE4 | ACTIVE | TSSOP | DGG | 48 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ALVTH16245 | Samples |
| 74ALVTH16245VRG4 | ACTIVE | TVSOP | DGV | 48 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | VT245 | Samples |
| SN74ALVTH16245DL | ACTIVE | SSOP | DL | 48 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ALVTH16245 | Samples |
| SN74ALVTH16245DLR | ACTIVE | SSOP | DL | 48 | 1000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ALVTH16245 | Samples |
| SN74ALVTH16245GR | ACTIVE | TSSOP | DGG | 48 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ALVTH16245 | Samples |
| SN74ALVTH16245VR | ACTIVE | TVSOP | DGV | 48 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | VT245 | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

# PACKAGE OPTION ADDENDUM

15-Jan-2021

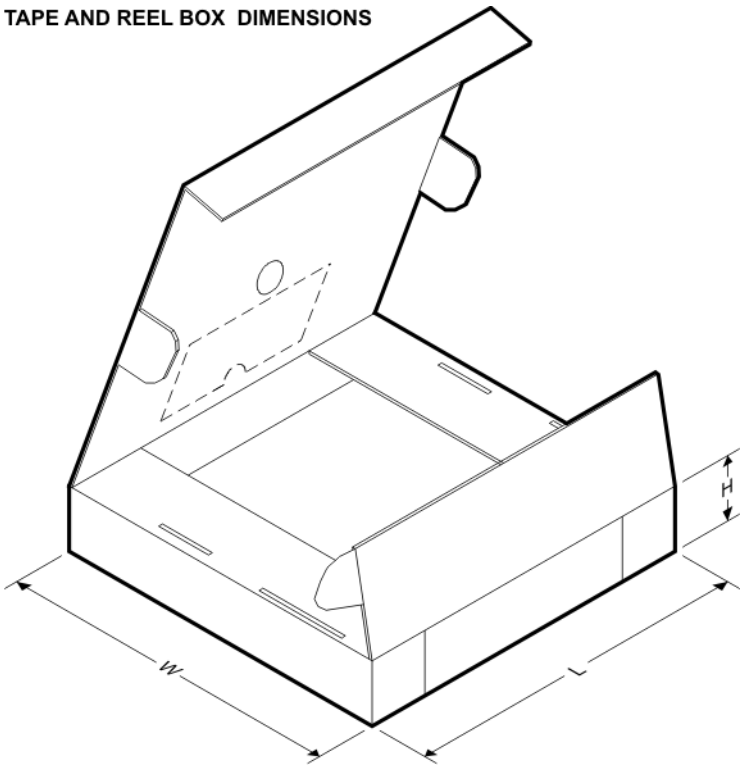
**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

# PACKAGE MATERIALS INFORMATION

13-Jan-2021

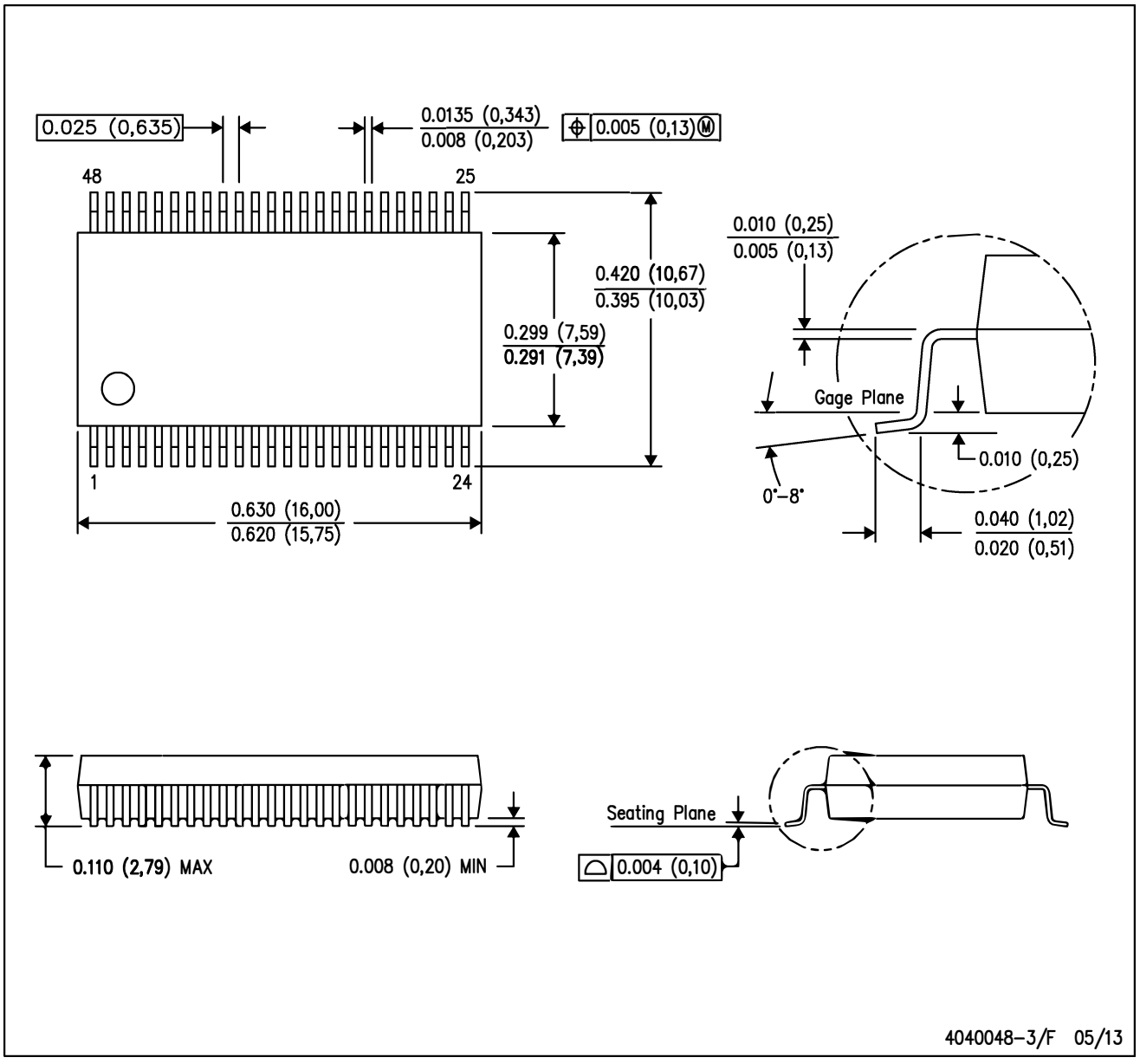
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74ALVTH16245DLR | SSOP | DL | 48 | 1000 | 367.0 | 367.0 | 55.0 |
| SN74ALVTH16245GR | TSSOP | DGG | 48 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74ALVTH16245VR | TVSOP | DGV | 48 | 2000 | 853.0 | 449.0 | 35.0 |

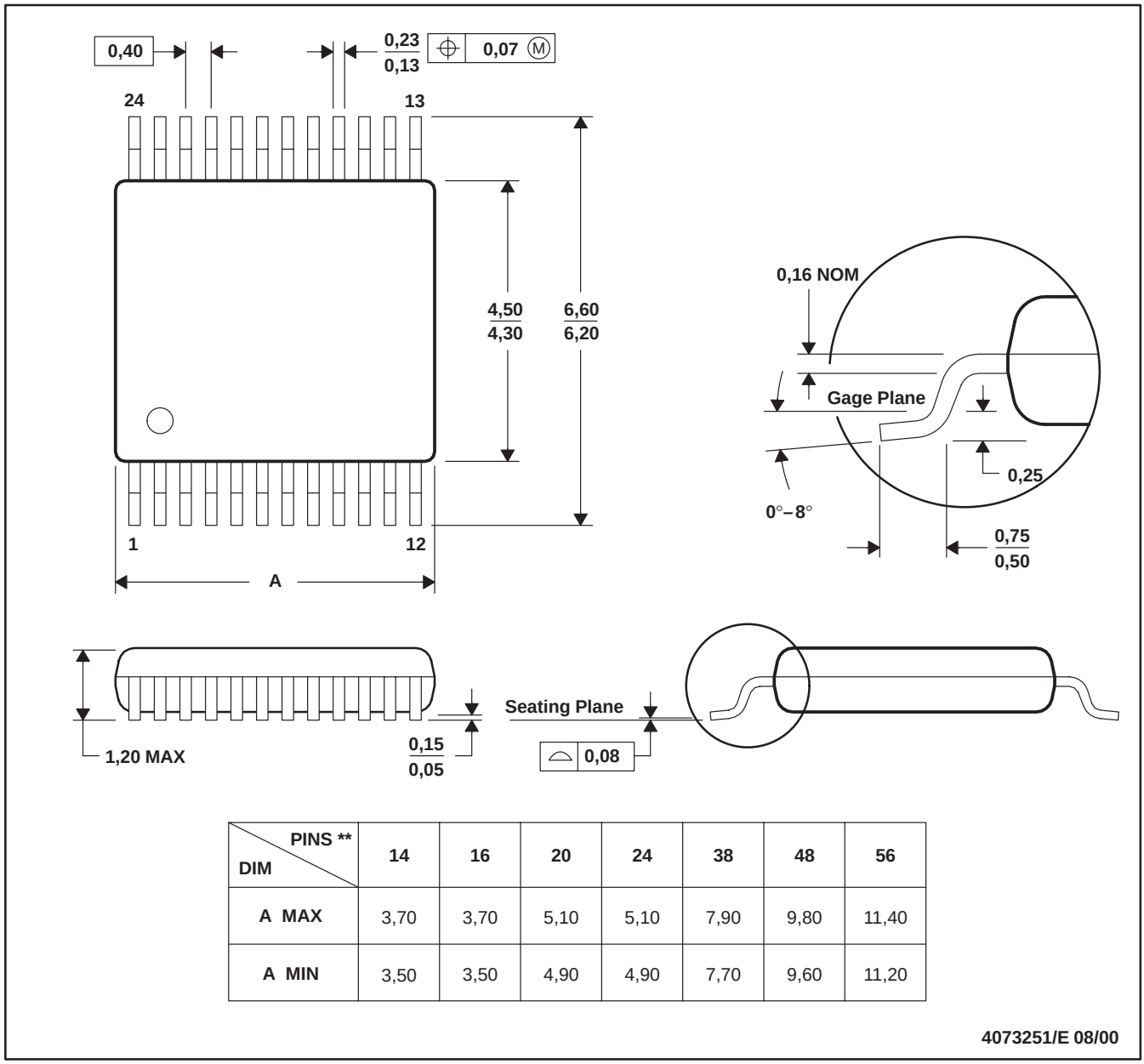
DL (R–PDSO–G48) PLASTIC SMALL–OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO–118

**DGV (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**24 PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 | 38 | 48 | 56 |
|---|---|---|---|---|---|---|---|
| A MAX | 3,70 | 3,70 | 5,10 | 5,10 | 7,90 | 9,80 | 11,40 |
| A MIN | 3,50 | 3,50 | 4,90 | 4,90 | 7,70 | 9,60 | 11,20 |

**4073251/E 08/00**

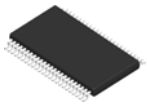
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

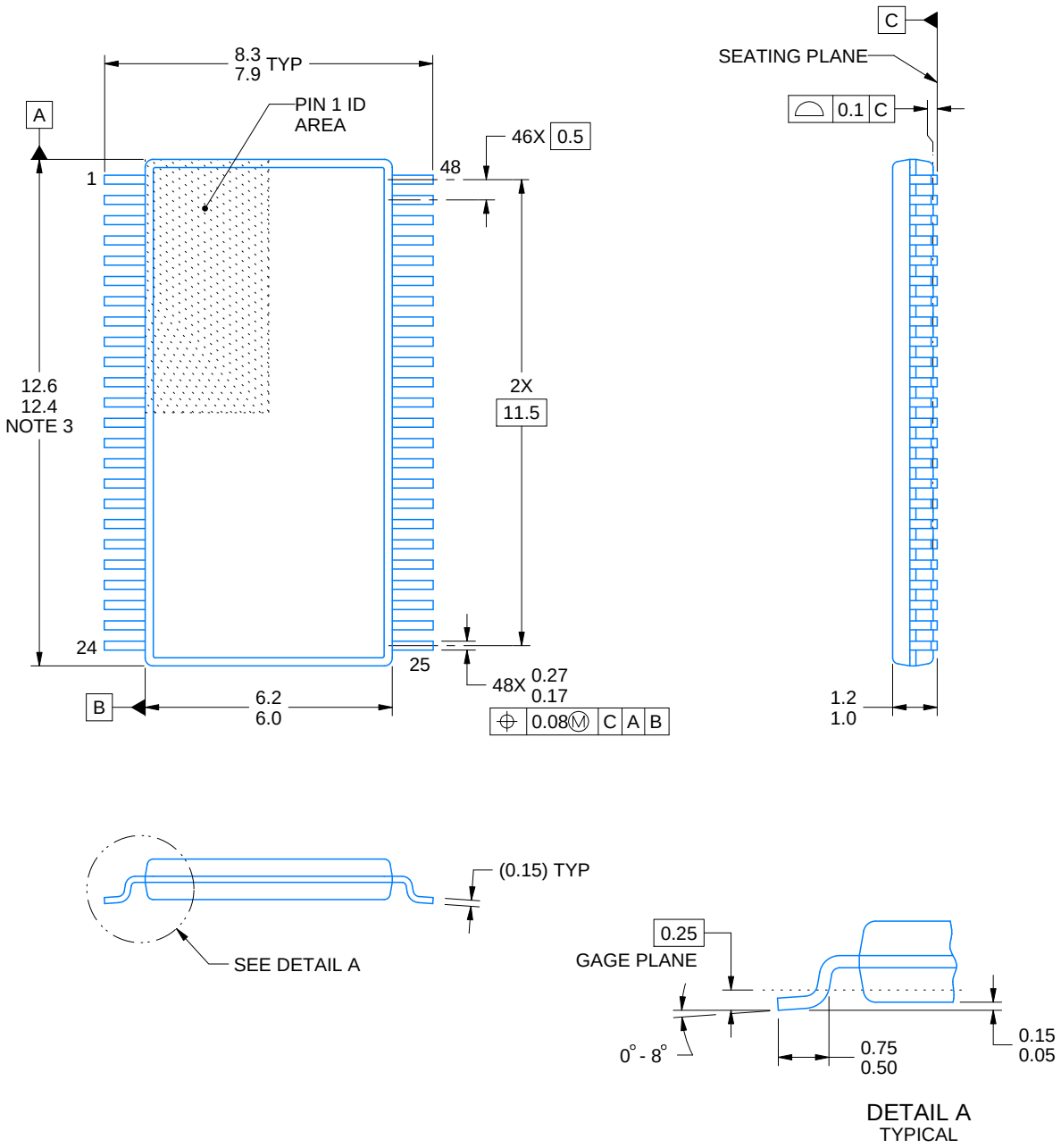
# PACKAGE OUTLINE

## DGG0048A

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



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NOTES:

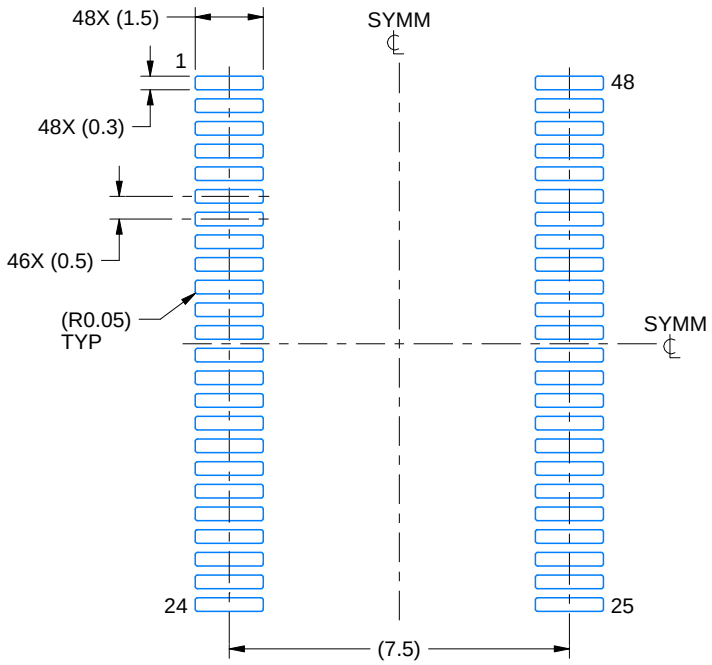
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

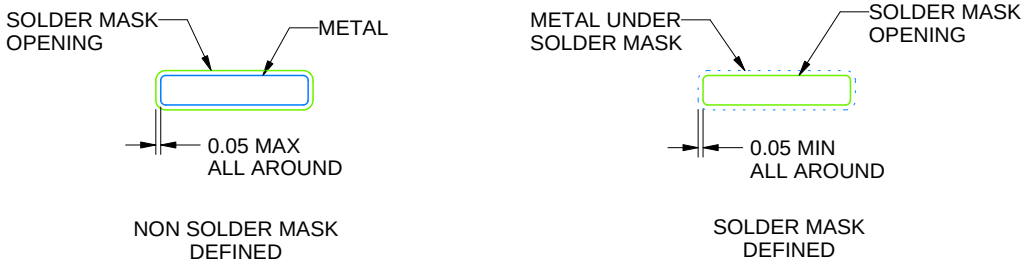
## DGG0048A

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE




LAND PATTERN EXAMPLE
SCALE:6X




SOLDER MASK DETAILS

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NOTES: (continued)

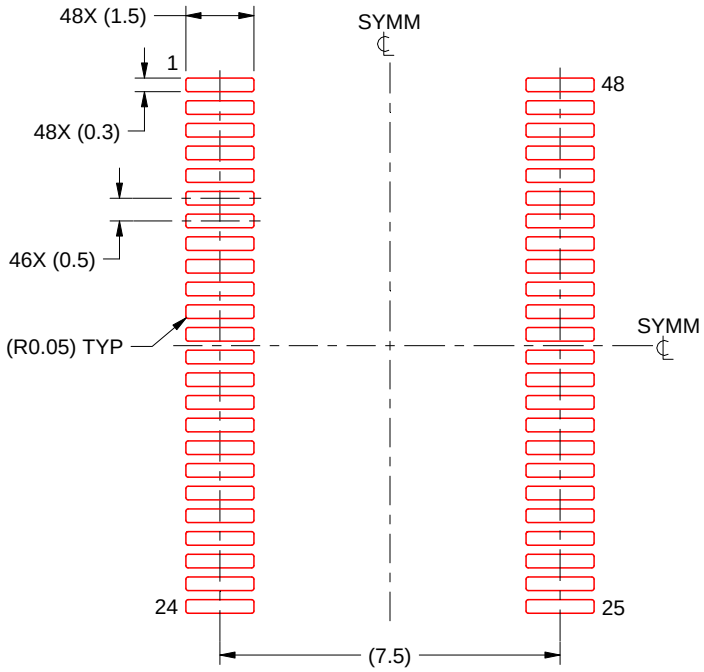
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## DGG0048A

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

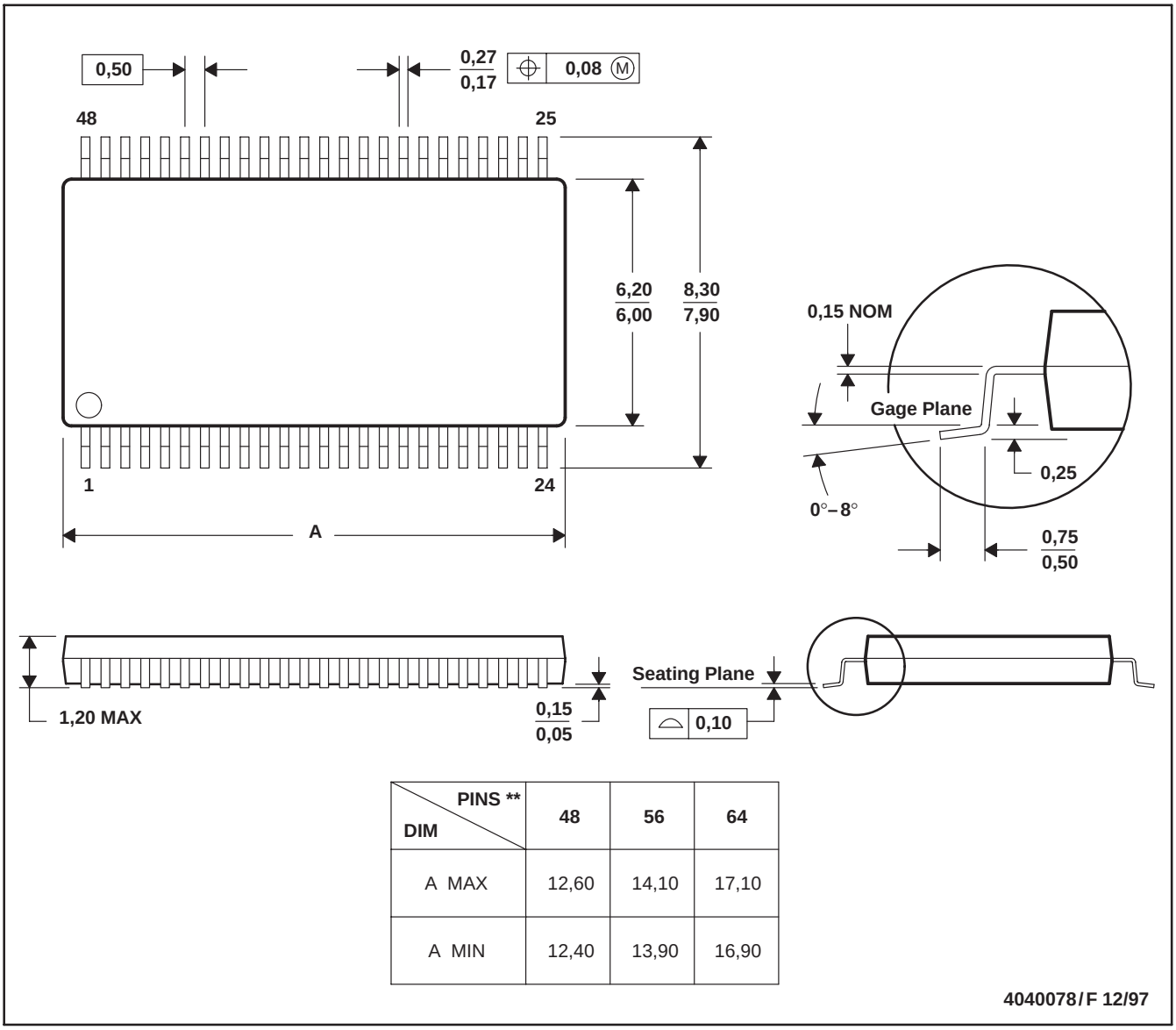
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

MTSS003D – JANUARY 1995 – REVISED JANUARY 1998

## DGG (R-PDSO-G**)

## PLASTIC SMALL-OUTLINE PACKAGE

**48 PINS SHOWN**




| DIM \ PINS ** | 48 | 56 | 64 |
|---|---|---|---|
| A MAX | 12,60 | 14,10 | 17,10 |
| A MIN | 12,40 | 13,90 | 16,90 |

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153