LM34940 Wide-Input-Voltage 100-V Buck Converter

1 Features

- Operates up to 100-V Input Voltage Range
- 1-A Maximum DC Load Current
  - 3-A Limited Load Transient Capability
- Constant ON-Time Control
  - No External Loop Compensation
  - Fast Transient Response
- Nearly Constant Switching Frequency
- Frequency Adjustable Up to 1 MHz
- Programmable Soft-Start Time
- Peak Current Limiting Protection
- Adjustable Input UVLO and Hysteresis
- ±1% Feedback Voltage Reference
- Thermal Shutdown Protection

2 Applications

- GSM/GPRS Tracker
- Telecom DC-DC Bias
- E-Meter Power Line Communication

3 Description

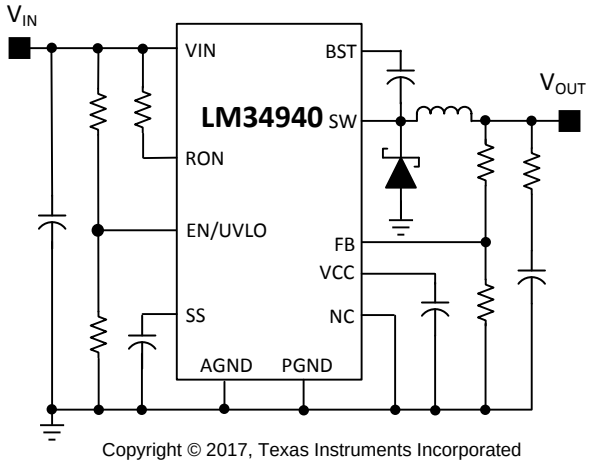
The LM34940 is a 100-V step-down buck converter with an integrated high-side MOSFET, capable of handling time limited 3-A DC load transients. The constant-ON-time control scheme requires no loop compensation and supports high step-down ratios with fast transient response. An internal feedback amplifier maintains ±1% output voltage regulation over the entire operating temperature range. The ON time varies inversely with input voltage resulting in nearly constant switching frequency. The peak current limit protection scheme along with an intelligent OFF-timer circuit protects the part against overload conditions. The undervoltage lockout (EN/UVLO) circuit provides independently adjustable input undervoltage threshold and hysteresis. When handling a DC load current of 3 A or higher over an extended time period, especially at input voltages close to the set output voltage in an application, the LM34940 is further protected from overheating by the internal thermal shutdown feature.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM34940	HTSSOP (14)	4.40 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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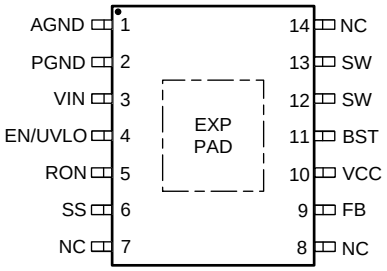
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
April 2017	*	Initial release

5 Pin Configuration and Functions

PWP Package
14-Pin HTSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	AGND	-	Analog ground. Ground connection of internal control circuits.
2	PGND	-	Power ground
3	VIN	I	Input supply connection. Operating input range is 4.5 V to 100 V.
4	EN/UVLO	I	Precision enable. Input pin of undervoltage lockout (UVLO) comparator.
5	RON	I	On-time programming pin. A resistor between this pin and VIN sets the switch ON time as a function of input voltage.
6	SS	I	Soft start. Connect a capacitor from SS to AGND to control output rise time and limit overshoot.
7,14	NC		No connection. PIN 14 can be connected to PIN 12,13 if needed for the SW node.
8	NC	I	Connect to AGND for all operation.
9	FB	I	Feedback input of voltage regulation comparator.
10	VCC	O	Internal high voltage start-up regulator bypass capacitor pin.
11	BST	I	Bootstrap capacitor pin. Connect a capacitor between BST and SW to bias gate driver of high-side buck FET.
12,13	SW	O	Switch node. Source connection of the internal high-side buck FET.
—	EP		Exposed pad. Connect to AGND and printed-circuit board ground plane to improve power dissipation.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
Input voltage	VIN to AGND	–0.3	100	V
	EN/UVLO to AGND	–0.3	100	
	RON to AGND	–0.3	100	
	BST to AGND	–0.3	114	
	VCC to AGND	–0.3	14	
	SS to AGND	–0.3	7	
	FB to AGND	–0.3	7	
Output voltage	BST to SW	–0.3	14	V
	BST to VCC		100	
	SW to AGND	–1.5	100	
Maximum junction temperature(3)		–40	150	°C
Storage temperature T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions(1)

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN} input voltage		9		95	V
I_O output current	Average load current rating			1	A
	Peak DC load current rating during load transient (limited to maximum 5ms time duration; never exceeding 25% total load duty cycle)			3	
External V_{CC} bias voltage		9		13	V
Operating junction temperature(2)		–40		125	°C

(1) Operating Ratings are conditions under the device is intended to be functional. For specifications and test conditions, see *Electrical Characteristics*.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.4 Thermal Information

THERMAL METRIC[1]		LM34940 PWP (HTSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	39.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	19.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.5	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

6.5 Electrical Characteristics

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over T_J = –40°C to +125°C for LM34940. Unless otherwise stated, V_{IN} = 48 V.[1][2]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{SD}	Input shutdown current	V_{IN} = 48 V, EN/UVLO = 0 V		50	90	µA
I_{OP}	Input operating current	V_{IN} = 48 V, FB = 3 V, Non-switching		2.3	2.5	mA
VCC SUPPLY						
V_{CC}	Bias regulator output	V_{IN} = 48 V, I_{CC} = 20 mA	6.3	7.3	8.5	V
V_{CC}	Bias regulator current limit	V_{IN} = 48 V	30			mA
$V_{CC(UV)}$	VCC undervoltage threshold	V_{CC} rising		3.98	4.1	V
$V_{CC(HYS)}$	VCC undervoltage hysteresis	V_{CC} falling		185		mV
$V_{CC(LDO)}$	VIN - VCC dropout voltage	V_{IN} = 4.5 V, I_{CC} = 20 mA		200	340	mV
HIGH-SIDE FET						
$R_{DS(ON)}$	High-side ON resistance	$V_{(BST - SW)}$ = 7 V, I_{SW} = 0.5 A		0.58	1.1	Ω
$BST_{(UV)}$	Bootstrap gate drive UV	$V_{(BST - SW)}$ rising		2.93	3.6	V
$BST_{(HYS)}$	Gate drive UV hysteresis	$V_{(BST - SW)}$ falling		200		mV
HIGH-SIDE CURRENT LIMIT						
$I_{LIM (HS)}$	High-side current limit threshold	T_J = 25°C		3.77	4.20	A
T_{RES}	Current limit response time	$I_{LIM (HS)}$ threshold detect to FET turnoff		120		ns
T_{OFF}	Current limit forced OFF time	FB = 0 V, V_{IN} = 72 V	13	16.5	21	µs
T_{OFF1}	Current limit forced OFF time	FB = 0.1 V, V_{IN} = 72 V	10	13	17	µs
T_{OFF2}	Current limit forced OFF time	FB = 1 V, V_{IN} = 72 V	2	2.7	4.1	µs
REGULATION COMPARATOR						
V_{REF}	FB regulation level	V_{IN} = 48 V	1.975	2	2.015	V
$I_{(BIAS)}$	FB input bias current	V_{IN} = 48 V			100	nA
ERROR CORRECTION AMPLIFIER AND SOFT START						
G_M	Error amp transconductance	FB = V_{REF} (±) 10 mV		100		µA/V
$I_{EA(SOURCE)}$	Error amp source current	FB = 1 V, SS = 1 V	7.5	10	12.5	µA
$I_{EA(SINK)}$	Error amp sink current	FB = 5 V, SS = 2.25 V	7.5	10	12.5	
$V_{(SS-FB)}$	V_{SS} - V_{FB} clamp voltage	FB = 1.75 V, $C_{(SS)}$= 1 nF		135		mV
I_{SS}	Softstart charging current	SS = 0.5 V	7.5	10	12.5	µA

(1) All minimum and maximum limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) The junction temperature (T_J in °C) is calculated from the ambient temperature (T_A in °C) and power dissipation (P_D in watts) as follows: $T_J = T_A + (P_D \times R_{\theta JA})$ where $R_{\theta JA}$ (in °C/W) is the package thermal impedance provided in *Thermal Information*.

Electrical Characteristics (continued)

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over T_J = –40°C to +125°C for LM34940. Unless otherwise stated, V_{IN} = 48 V.[1][2]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENABLE/UVLO						
$V_{UVLO\ (TH)}$	UVLO threshold	EN/UVLO rising	1.2	1.24	1.27	V
$I_{UVLO(HYS)}$	UVLO hysteresis current	EN/UVLO = 1.4 V	15	20	25	µA
$V_{SD(TH)}$	Shutdown mode threshold	EN/UVLO falling	0.29	0.35		V
$V_{SD(HYS)}$	Shutdown threshold hysteresis	EN/UVLO rising		50		mV
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown threshold			175		°C
$T_{SD(HYS)}$	Thermal shutdown hysteresis			20		°C

6.6 Switching Characteristics

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over T_J = –40°C to +125°C for LM34940. Unless otherwise stated, V_{IN} = 48 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MINIMUM OFF TIME						
$T_{OFF-MIN}$	Minimum OFF time	FB = 0 V		170		ns
ON-TIME GENERATOR						
T_{ON} Test 1	V_{IN} = 24 V, R_{ON} = 100 kΩ		420	520	630	ns
T_{ON} Test 2	V_{IN} = 48 V, R_{ON} = 100 kΩ			290		ns
T_{ON} Test 3	V_{IN} = 8 V, R_{ON} = 100 kΩ		1150	1325	1500	ns
T_{ON} Test 4	V_{IN} = 72 V, R_{ON} = 150 kΩ			290		ns

6.7 Typical Characteristics

At T_A = 25°C and applicable to LM34940 unless otherwise noted.

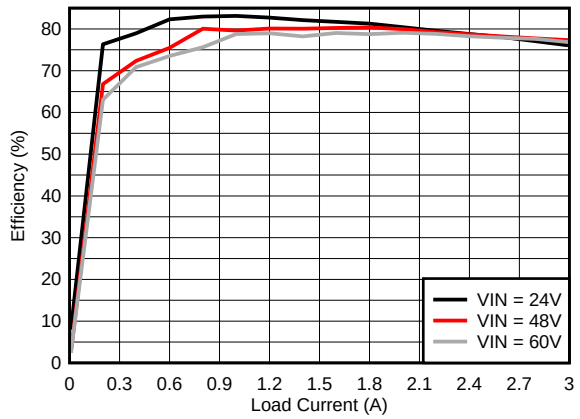


Figure 1. Efficiency at 100 kHz

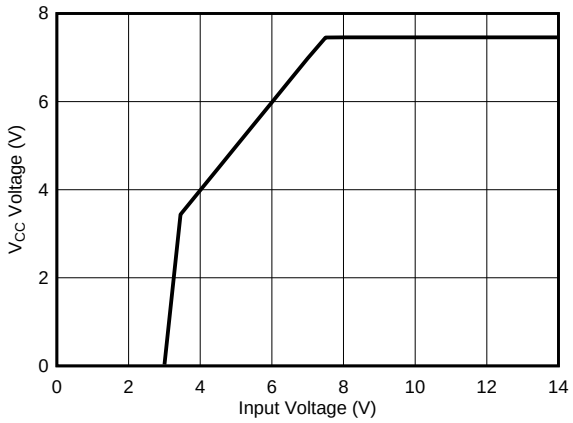


Figure 2. V_{CC} vs V_{IN}

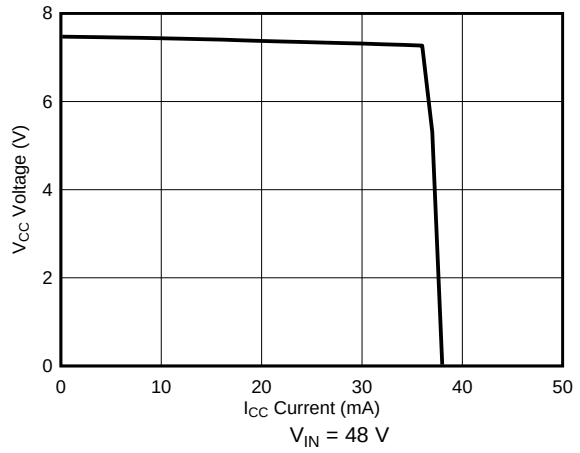


Figure 3. V_{CC} vs I_{CC}

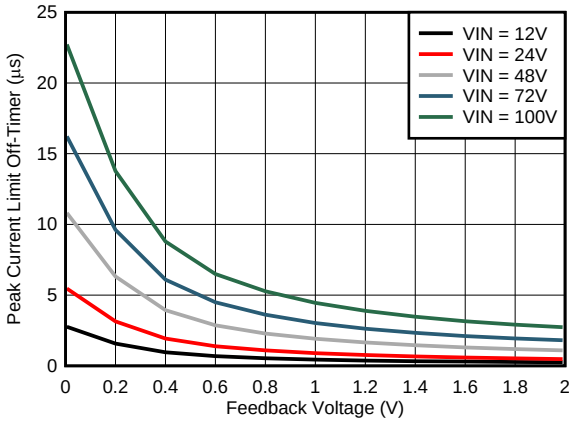


Figure 4. T_{OFF} (I_{LIM}) vs V_{FB}

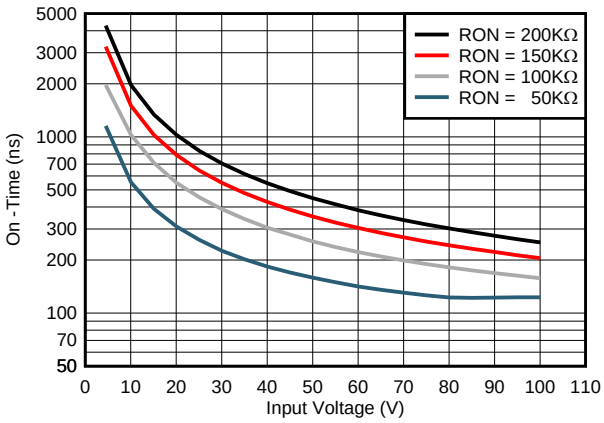


Figure 5. T_{ON} vs V_{IN}

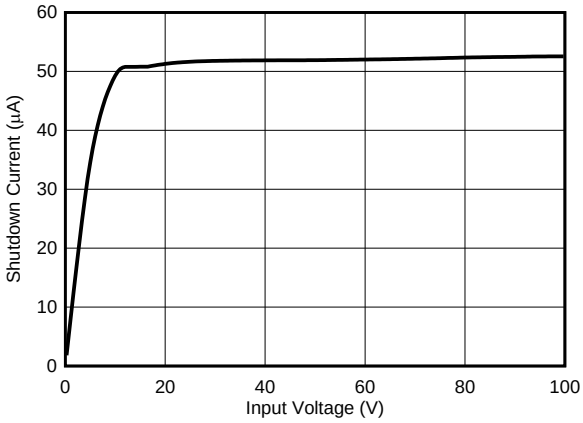


Figure 6. Shutdown Current vs V_{IN}

Typical Characteristics (continued)

At T_A = 25°C and applicable to LM34940 unless otherwise noted.

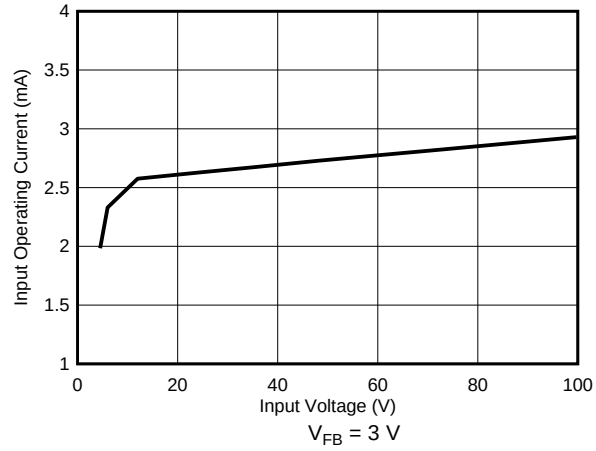


Figure 7. I_{IN} vs V_{IN} (Operating, Non Switching)

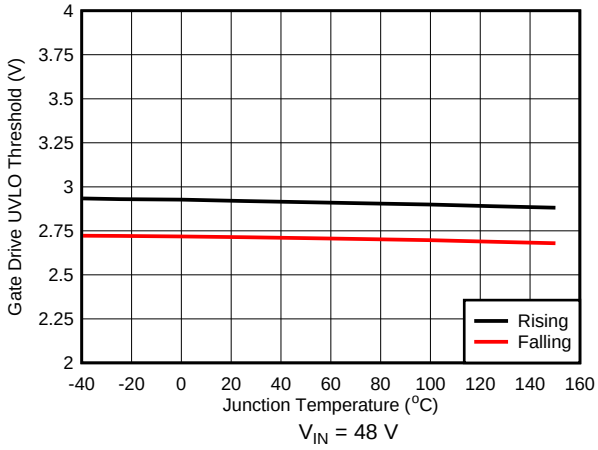


Figure 8. High-Side FET Gate Drive UVLO vs Temperature

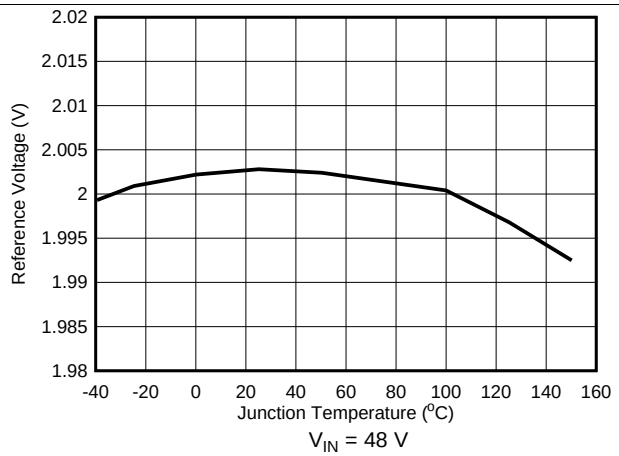


Figure 9. Reference Voltage vs Temperature

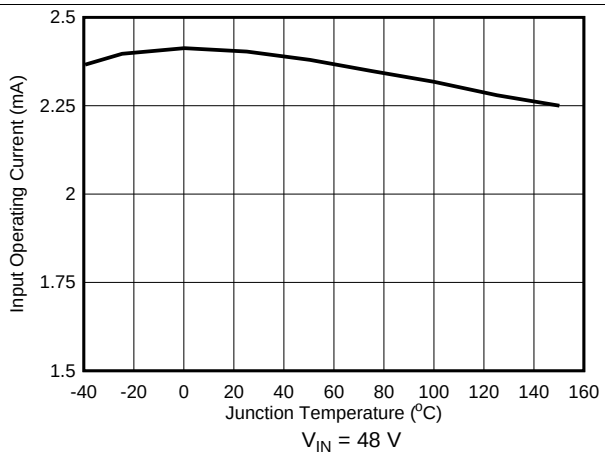


Figure 10. Input Operating Current vs Temperature

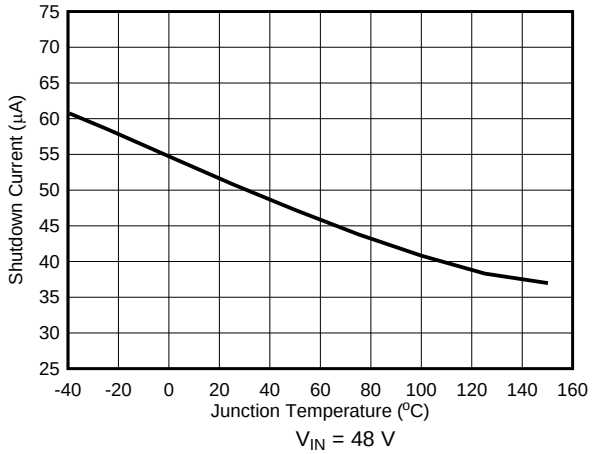


Figure 11. Input Shutdown Current vs Temperature

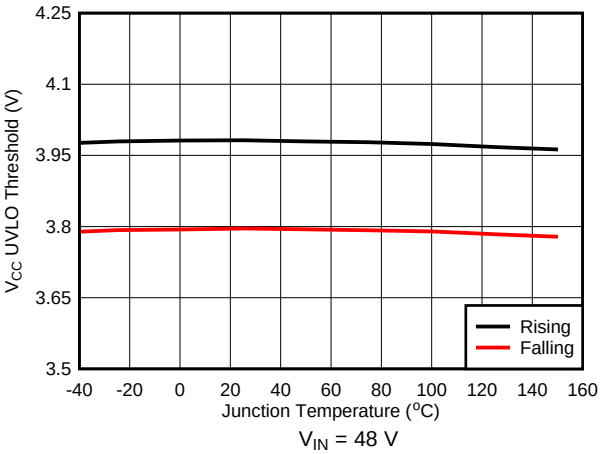


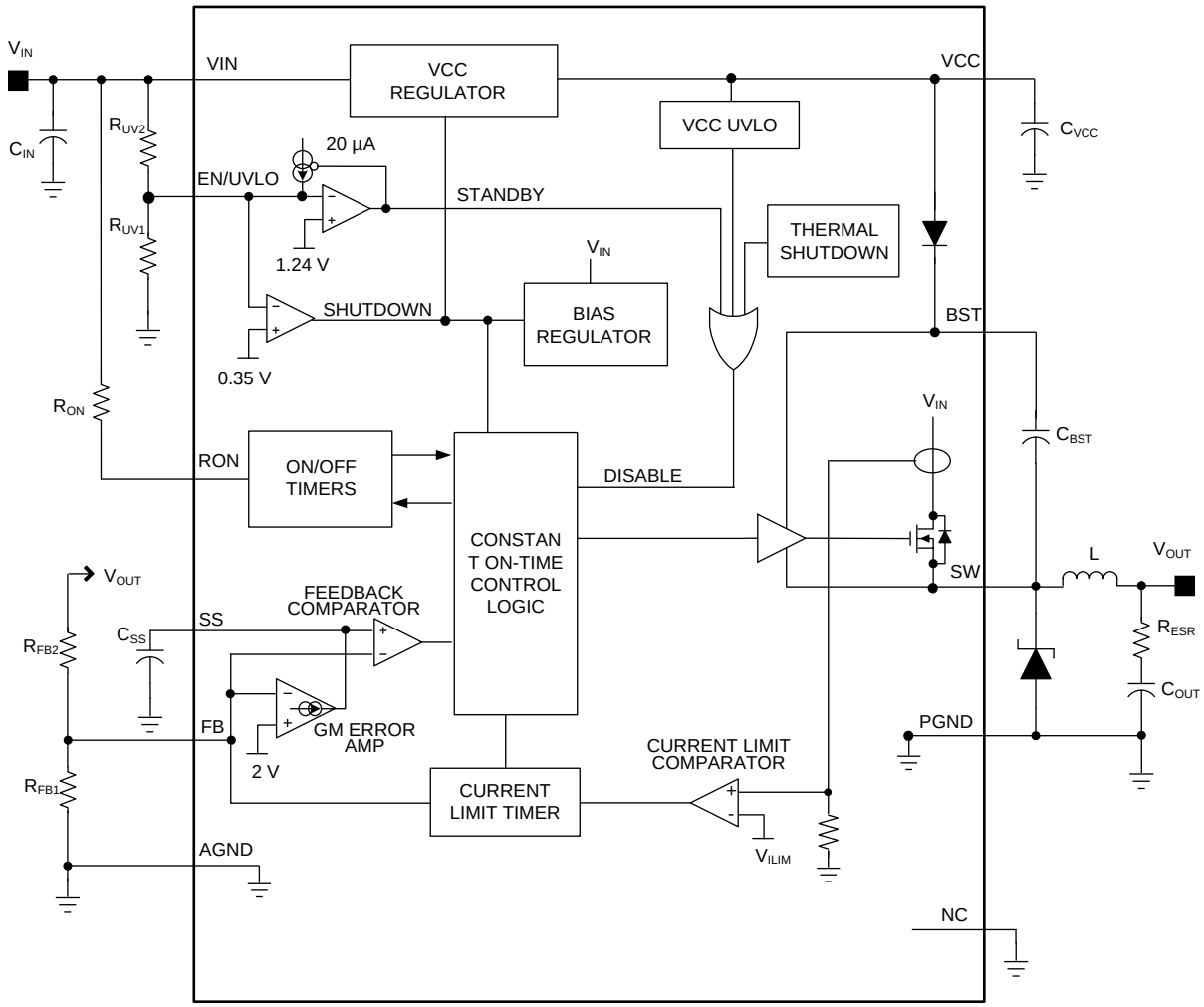
Figure 12. V_{CC} UVLO vs Temperature

7 Detailed Description

7.1 Overview

The LM34940 step-down switching regulator features all the functions needed to implement a low-cost, efficient buck converter. This high-voltage converter contains a 100-V, N-channel buck switch and is available in the 14-pin HTSSOP package. The regulator operation is based on constant ON-time control where the ON time is inversely proportional to input voltage V_{IN}. This feature maintains a relatively constant operating frequency with load and input-voltage variations. A constant ON-time switching regulator requires no loop compensation resulting in fast load-transient response. Peak current limit detection circuit is implemented with a forced OFF time during current limiting which is inversely proportional to voltage at the feedback pin, V_{FB} and directly proportional to V_{IN}. The variation in the current limit OFF time with V_{FB} and V_{IN} ensures short-circuit protection with minimal current limit foldback. The LM34940 can be applied in numerous end equipment systems requiring efficient step-down regulation from higher input voltages. This regulator is well-suited for 24-V industrial systems as well as for 48-V telecom ranges. The LM34940 integrates an undervoltage lockout (EN/UVLO) circuit to prevent faulty operation of the device at low input voltages and features intelligent current limit and thermal shutdown to protect the device during overload or short circuit.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Control Circuit

The LM34940 step-down switching regulator employs a control principle based on a comparator and a one-shot ON timer, with the output voltage feedback (FB) compared to the voltage at the soft-start (SS) pin (V_{SS}). If the FB voltage is below V_{SS}, the internal buck switch is turned on for a time period determined by the input voltage and one-shot programming resistor (R_{ON}). Following the ON time, the buck switch must remain off for the minimum OFF time forced by the minimum OFF-time one-shot. The buck switch remains off until the FB voltage falls below $V_{(SS)}$ again, when it turns on for another ON-time one-shot period.

During a rapid start-up or when the load current increases suddenly, the regulator operates with minimum OFF time per cycle. When regulating the output in steady state operation, the OFF time automatically adjusts to produce the SW pin duty cycle required for output voltage regulation.

When in regulation, the LM34940 operates in discontinuous conduction mode at light load. With sufficient load, the LM34940 operates in continuous conduction mode with the inductor current never reaching zero during the OFF time of the high-side FET. In this mode the operating frequency remains relatively constant with load and line variations. The minimum load current for continuous conduction mode is one-half the inductor's ripple current amplitude. The operating frequency (in Hz) is programmed by the RON pin resistor and can be calculated from Equation 1 with R_{ON} expressed in ohms.

$$F_{SW} \quad \frac{V_{OUT}}{1.008 \times 10^{-10} \times R_{ON}} \text{ Hz} \tag{1}$$

In discontinuous conduction mode (DCM), current through the inductor ramps up from zero to a peak value during the ON time, then ramps back to zero before the end of the OFF time. The next ON-time period starts when the voltage at FB falls below V_{SS}. When the inductor current is zero during the high-side FET OFF time, the load current is supplied by the output capacitor. In this mode, the operating switching frequency is lower than the continuous conduction mode switching frequency and the frequency varies with load. The discontinuous conduction mode maintains higher conversion efficiency at light loads since the switching losses decrease with the decrease in load and frequency.

The output voltage is set by two external resistors (R_{FB1}, R_{FB2}). The regulated output voltage is calculated from Equation 2, where V_{REF} = 2 V (typical) is the feedback reference voltage.

$$V_{OUT} \quad \frac{V_{REF} \times (R_{FB2} + R_{FB1})}{R_{FB1}} \text{ V} \tag{2}$$

7.3.2 VCC Regulator

The LM34940 contains an internal high-voltage linear regulator with a nominal output voltage of 7.3 V (typical). The VCC regulator is internally current limited to 30 mA (minimum). This regulator supplies power to internal circuit blocks including the high-side gate driver and the logic circuits. When the voltage on the VCC pin reaches the undervoltage lockout ($V_{CC(UV)}$) threshold of 3.98 V (typical) normal switching operation begins. An external capacitor at the VCC pin stabilizes the regulator and supplies transient VCC current. An internal diode connected from VCC to the BST pin replenishes the charge in the high-side gate drive bootstrap capacitor when the SW pin is low.

In high input-voltage applications, the power dissipated in the regulator is significant and can limit the efficiency and maximum achievable output power. The LM34940 allows the internal VCC regulator power loss to be reduced by supplying the VCC voltage via a diode from an external voltage source regulated between 9 V and 13 V. The external VCC bias can be supplied from the LM34940 converter output rail if the regulation voltage is within this range. When the VCC pin of the LM34940 is raised above the regulation voltage (7.3 V typical), the internal regulator is disabled and the power dissipation in the device is reduced.

Feature Description (continued)

7.3.3 Regulation Comparator

The feedback voltage at the FB pin is compared to the SS pin voltage $V_{(SS)}$. In normal operation when the output voltage is in regulation, an ON-time period is initiated when the voltage at FB pin falls below $V_{(SS)}$. The high-side buck switch stays on for the ON-time one-shot period causing the FB voltage to rise. After the ON-time period expires, the high-side switch remains off until the FB voltage falls below V_{SS}. During start-up, the FB voltage is below V_{SS} at the end of each ON-time period and the high-side switch turns on again after the minimum forced OFF time of 170 ns (typical). When the output is shorted to ground (FB = 0 V), the high-side peak current limit is triggered, the high-side FET is turned off and remains off for a period determined by the current limit OFF-time one-shot. See *Current Limit* for additional information.

7.3.4 Soft Start

The soft-start feature of the LM34940 allows the converter to gradually reach a steady-state operating point, thereby reducing start-up stresses and current surges. When the EN/UVLO pin is above the EN/UVLO standby threshold $V_{UVLO(TH)}$ = 1.24 V (typical) and VCC exceeds the VCC undervoltage $V_{CC(UV)}$ = 3.98 V (typical) threshold, an internal 10-µA current source charges the external capacitor at the SS pin ($C_{(SS)}$) from 0 V to 2 V. The voltage at the SS pin is connected to the noninverting input of the internal FB comparator. The soft-start interval ends when the SS capacitor is charged to the 2-V reference level. The ramping voltage at the SS pin produces a controlled, monotonic output voltage start-up. Use a minimum 1-nF soft-start capacitor in all applications.

7.3.5 Error Transconductance (G_M) Amplifier

The LM34940 provides a transconductance (G_M) error amplifier that minimizes the difference between the reference voltage (V_{REF}) and the average feedback (FB) voltage. This amplifier reduces the load and line regulation errors that are common in constant-on-time regulators. The soft-start capacitor (C_{SS}) provides compensation for this error correction loop. The soft-start capacitor must be greater than 1 nF to ensure stability.

7.3.6 ON-Time Generator

The ON time of the LM34940 high-side FET is determined by the R_{ON} resistor and is inversely proportional to the input voltage (V_{IN}). The inverse relationship with V_{IN} results in a nearly constant frequency as V_{IN} is varied. The ON time can be calculated from Equation 3 with R_{ON} expressed in ohms.

$$T_{ON} \quad \frac{1.008 \times 10^{-10} \times R_{ON}}{V_{IN}} \text{ s} \tag{3}$$

To set a specific continuous conduction mode (CCM) switching frequency (F_{SW} expressed in Hz), the R_{ON} resistor is determined from Equation 4:

$$R_{ON} \quad \frac{V_{OUT}}{1.008 \times 10^{-10} \times F_{SW}} \ \Omega \tag{4}$$

R_{ON} must be selected for a minimum on-time (at maximum V_{IN}) greater than 150 ns for proper operation. This minimum ON-time requirement limits the maximum switching frequency of applications with relatively high V_{IN} and low V_{OUT}.

7.3.7 Current Limit

The LM34940 provides an intelligent current limit OFF timer that adjusts the OFF time to reduce foldback of the current limit. If the peak value of the current in the buck switch exceeds 4.2 A (maximum) the present ON-time period is immediately terminated, and a non-resettable OFF timer is initiated. The length of the OFF time is controlled by the FB voltage and the input voltage V_{IN}. For example, when V_{FB} = 0.1 V and V_{IN} = 72 V, the OFF time is set to 13 µs (typical). This condition occurs if the output is shorted or during the initial phase of start-up. In cases of output overload where the FB voltage is greater than zero volts (a soft short), the current limit OFF time is reduced. Reducing the OFF time during less severe overloads reduces the current limit foldback, overload recovery time, and start-up time. The current limit off time, $T_{OFF(CL)}$ is calculated from Equation 5:

$$T_{OFF(CL)} \quad \frac{V_{IN}}{20\,V_{FB} + 4.35} \ \mu\text{s} \tag{5}$$

Feature Description (continued)

7.3.8 N-Channel Buck Switch and Driver

The LM34940 integrates an N-channel buck switch and associated floating high-side gate driver. The gate-driver circuit works in conjunction with an external bootstrap capacitor and an internal high-voltage bootstrap diode. A 10-nF or larger ceramic capacitor connected between the BST pin and the SW pin provides the voltage to the high-side driver during the buck switch ON time. During the OFF time as the SW node is pulled down, and the bootstrap capacitor charges from VCC through the internal bootstrap diode. The minimum OFF time of 170 ns (typical) provides a minimum time each cycle to recharge the bootstrap capacitor.

7.3.9 Enable/Undervoltage Lockout (EN/UVLO)

The LM34940 contains a dual-level undervoltage lockout (EN/UVLO) circuit. When the EN/UVLO pin voltage is below 0.35 V (typical), the regulator is in a low-current shutdown mode. When the EN/UVLO pin voltage is greater than 0.35 V (typical) but less than 1.24 V (typical), the converter is in standby mode. In standby mode, the VCC bias regulator is active, but converter switching remains disabled. When the voltage at the VCC pin exceeds the VCC rising threshold $V_{CC(UV)}$ = 3.98 V (typical) and the EN/UVLO pin voltage is greater than 1.24 V, normal switching operation begins. An external resistor voltage divider from VIN to GND can be used to set the minimum operating voltage of the regulator.

EN/UVLO hysteresis is accomplished with an internal 20-µA (typical) current source ($I_{UVLO(HYS)}$) that is switched on or off into the impedance of the EN/UVLO pin resistor divider. When the EN/UVLO threshold is exceeded, the current source is activated to effectively raise the voltage at the EN/UVLO pin. The hysteresis is equal to the value of this current times the upper resistance of the resistor divider, (R_{UV2}) (see *Functional Block Diagram* .

7.3.10 Thermal Protection

The LM34940 must be operated such that the junction temperature does not exceed 150°C during normal operation. An internal thermal shutdown circuit is provided to protect the LM34940 in the event of a higher than normal junction temperature. When activated, typically at 175°C, the converter is forced into a low power-reset state, disabling the high-side buck switch and the VCC regulator. Also, when the LM34940 detects a 3-A load transient operation over a prolonged period of time (typically the 3-A load transient must be limited to less than 5-ms time duration; not exceeding 25% total load duty cycle) at input voltages close to the regulated output voltage, the device can be pushed into thermal shutdown during normal operation. This feature prevents catastrophic failures due to device overheating. When the junction temperature falls below 155°C (typical hysteresis = 20°C), the VCC regulator is enabled, and normal operation resumes.

7.4 Device Functional Modes

7.4.1 Undervoltage Detector

Table 1 summarizes the dual threshold levels of the undervoltage lockout (EN/UVLO) circuit explained in *Enable/Undervoltage Lockout (EN/UVLO)* .

Table 1. UVLO Pin Mode Summary

EN/UVLO PIN VOLTAGE	VCC REGULATOR	MODE	DESCRIPTION
< 0.35 V	Off	Shutdown	V_{CC} regulator disabled. High side FET disabled.
0.35 V to 1.24 V	On	Standby	V_{CC} regulator active. High side FET disabled.
> 1.24 V	$V_{CC} < V_{CC(UV)}$	Standby	V_{CC} regulator active. High side FET disabled.
	$V_{CC} > V_{CC(UV)}$	Operating	V_{CC} regulator active. Converter switching enabled.

If an EN/UVLO setpoint is not required, the EN/UVLO pin can be driven by a logic signal as an enable input or connected directly to the VIN pin. If the EN/UVLO is directly connected to the VIN pin, the regulator begins switching when the V_{CC} UVLO is satisfied.

8 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM34940 is a buck converter designed to operate over a wide input voltage and output current range. The *Typical Application* describes a typical buck application circuit using the LM34940 with detailed, step-by-step design procedures.

8.2 Typical Application

8.2.1 LM34940 Buck (15-V to 80-V Input)

A typical application example is a non-synchronous buck converter operating from a wide input voltage range of 15 V to 80 V, which provides a stable 5-V output voltage with a maximum output current capability of 1 A and limited 3-A load transient handling capability. The complete schematic for a typical non-synchronous buck application circuit with the LM34940 device is shown in Figure 13. In Figure 13, the components are labeled by their respective descriptive names.

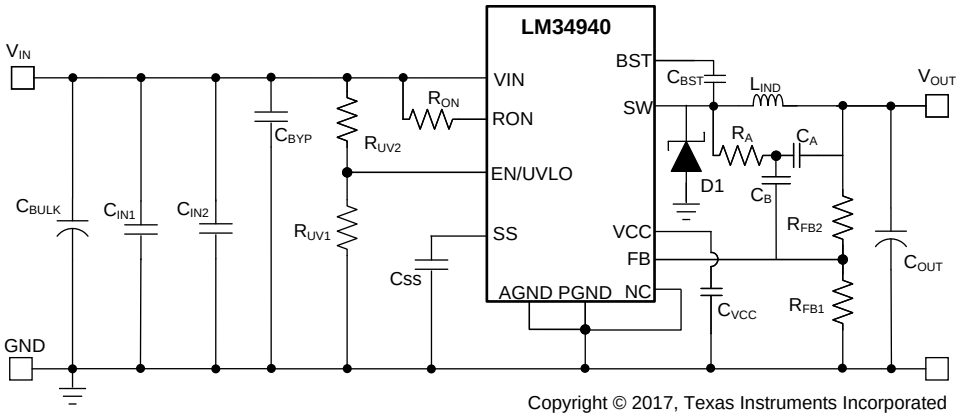


Figure 13. Non-Synchronous Buck Application Circuit with LM34940

8.2.1.1 Design Requirements

A typical buck application introduced in *LM34940 Buck (15-V to 80-V Input)* , Table 2 summarizes the operating parameters:

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	15 V to 80 V
output	5 V
Full load current	1 A
Maximum Load transient capability	3 A (Limited to 5-ms transient operation)
Nominal switching frequency	100 kHz

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Output Resistor Divider Selection

With the required output voltage set point at 5 V and V_{FB} = 2 V (typical), the ratio of (R_{FB1}) to (R_{FB2}) can be calculated using Equation 6:

$$\frac{R_{FB2}}{R_{FB1}} \quad \frac{V_{OUT}}{V_{REF}} - 1 \tag{6}$$

The resistor ratio calculates to be 3:2. Standard values of R_{FB1} = 2 kΩ and R_{FB2} =3.01 kΩ are chosen.

8.2.1.2.2 Frequency Selection

The duty cycle required to maintain output regulation at the minimum input voltage restricts the maximum switching frequency of LM34940. The maximum value of the minimum forced OFF time $T_{OFF,\ min}$ (maximum), limits the duty cycle and therefore the switching frequency. The maximum frequency that avoids output dropout at minimum input voltage can be calculated from Equation 7.

$$F_{SW,\,max\,(@\,V_{IN,\,min})} \quad \frac{V_{IN,\,min} - V_{OUT}}{V_{IN,\,min} \times T_{OFF,\,min}(ns)} \tag{7}$$

For this design example, the maximum frequency based on the minimum OFF-time limitation for $T_{OFF,min}$ (typical) = 170 ns is calculated to be $F_{SW,max(@VIN,min)}$ = 3.9 MHz. This value is above 1 MHz, the maximum possible operating frequency of the LM34940. Therefore, the minimum OFF-time parameter restricts the maximum achievable switching frequency calculation in this application.

At the maximum input voltage, the maximum switching frequency of LM34940 is restricted by the minimum ON-time, $T_{ON,min}$, which limits the minimum duty cycle of the converter. The maximum frequency at maximum input voltage can be calculated using Equation 8.

$$F_{SW,\,max\,(@\,V_{IN,\,max})} \quad \frac{V_{OUT}}{V_{IN,\,max} \times T_{ON,\,min}(ns)} \tag{8}$$

Using Equation 8 and $T_{ON,min}$ (typical) = 150 ns, the maximum achievable switching frequency is $F_{SW,max(@VIN,max)}$= 417.5 kHz. Taking this value as the maximum possible operational switching frequency over the input voltage range in this application, a nominal switching frequency of F_{SW} = 100 kHz is chosen for this design.

The value of the resistor, R_{ON} sets the nominal switching frequency based on Equation 9.

$$R_{ON} \quad \frac{V_{OUT}}{1.008 \times 10^{-10} \times F_{SW}}\ \Omega \tag{9}$$

For this particular application with F_{SW} = 100 kHz, R_{ON} calculates to be 497 kΩ . Selecting a standard value for R_{ON} = 499 kΩ (±1%) results in a nominal frequency of 100 kHz. The resistor value may need to adjusted further in order to achieve the required switching frequency as the switching frequency in constant ON-time converters varies slightly(±10%) with input voltage and/or output current. Operation at a lower nominal switching frequency results in higher efficiency but increase in the inductor and capacitor values leading to a larger total solution size.

8.2.1.2.3 Inductor Selection

Select the inductor to limit the inductor ripple current to a value between 20 and 40 percent of the maximum load current. The minimum value of the inductor required in this application can be calculated from Equation 10:

$$L_{min} \quad \frac{V_O \times (V_{IN,\,max} - V_O)}{V_{IN,\,max} \times F_{SW} \times I_{O,\,max} \times 0.4} \tag{10}$$

Based on Equation 10, the minimum value of the inductor is calculated to be 117 µH for V_{IN} = 80 V (maximum), and inductor current ripple is 40 percent of the maximum load current. Allowing margin for inductance variation and inductor saturation, a standard value of L1 (L) = 47 µH is selected for this design, in order to keep the inductor size small compared to the entire solution size.

The peak inductor current at maximum load must be smaller than the minimum current limit threshold of the high-side FET as given in *Electrical Characteristics* . The inductor current ripple at any input voltage is given by:

$$\Delta I_L \quad \frac{V_O \times (V_{IN} - V_O)}{V_{IN} \times F_{SW} \times L} \tag{11}$$

The peak-to-peak inductor current ripple is calculated to be 712 mA and 1 A at the minimum and maximum input voltages, respectively. The maximum peak inductor current in the buck FET is given by Equation 12:

$$I_{L(peak)} \quad I_{O,max} + \frac{\Delta I_{L,max}}{2} \tag{12}$$

In this design with maximum DC steady-state-output current of 1-A, the maximum peak-inductor current is calculated to be approximately 1.5 A at $V_{IN,\ max}$ = 80 V, which is less than the high-side FET-current-limit threshold. Even at 3-A load transient operation, the inductor peak current at $V_{IN,\ max}$ = 80 V measures 3.5 A.

The saturation current of the inductor must also be carefully considered. The peak value of the inductor current is bound by the high-side FET current limit during overload or short circuit conditions. Based on the high side FET current limit specification in the *Electrical Characteristics*, select an inductor with saturation current rating above 4.7A (maximum).

8.2.1.2.4 Output Capacitor Selection

The output capacitor is selected to limit the capacitive ripple at the output of the regulator. Maximum capacitive ripple is observed at maximum input voltage. The output capacitance required for a ripple voltage ΔV_O across the capacitor is given by Equation 13.

$$C_{OUT} \quad \frac{\Delta I_{L,max}}{8 \times F_{SW} \times \Delta V_{O,ripple}} \tag{13}$$

Substituting $\Delta V_{O,\ ripple}$ = 10 mV gives C_{OUT} = 125 µF. One standard 100-µF polymer capacitor C_{OUT} is selected in this case.

8.2.1.2.5 Diode Selection

TI recommends a Schottky diode. Ultra-fast recovery diodes are not recommended as the high speed transitions at the SW pin may inadvertently affect operation of the device through external or internal EMI. The diode must be rated for the maximum input voltage, the maximum load current, and the peak current which occurs in current limiting. A 100-V schottky diode has been selected for D1 in the application schematic.

8.2.1.2.6 VCC and Bootstrap Capacitor

The VCC capacitor charges the bootstrap capacitor during the OFF time of the high-side switch and powers internal logic circuits. The bootstrap capacitor biases the high-side gate driver during the high-side FET ON time. A good value for C_{VCC} is 1 µF. A good choice for C_{BST} is 220 nF. Both must be high-quality X7R ceramic capacitors.

8.2.1.2.7 Input Capacitor Selection

The input capacitor must be large enough to limit the input voltage ripple to an acceptable level. Equation 14 provides the input capacitance C_{IN} required for a worst case input ripple of $\Delta V_{IN,\ ripple}$.

$$C_{IN} \quad \frac{I_{O,max} \times D \times (1-D)}{\Delta V_{IN,ripple} \times F_{SW}} \tag{14}$$

C_{IN} supplies most of the switch current during the ON time to limit the voltage ripple at the VIN pin. At maximum load current, when the buck switch turns on, the current into the VIN pin quickly increases to the valley current of the inductor ripple and then ramps up to the peak of the inductor ripple during the ON time of the high-side FET. The average current during the ON time is the output load current. For a worst-case calculation, C_{IN} must supply this average load current during the maximum ON time, without letting the voltage at VIN drop more than the desired input ripple. For this design, the input voltage drop is limited to 0.5 V and the value of C_{IN} is calculated using Equation 14.

Based on Equation 14, the value of the input capacitor is calculated to be approximately 15.06 µF at D = 0.5 for 3 A of transient load. Taking into account the decrease in capacitance over an applied voltage, two standard value ceramic capacitors of 2.2 µF are selected for C_{IN1} and C_{IN2} and an electrolytic capacitor of 22 µF for C_{BULK}. The input capacitors must be rated for the maximum input voltage under all operating and transient conditions. A 100-V, X7R dielectric was selected for this design.

Use a third input capacitor C_{BYP} in this design as a bypass path for the high frequency noise component of the input switching current. The value of 0.1 µF for this bypass capacitor must be placed directly across VIN and PGND (pin 3 and 2) near the device. The C_{IN} values and location are critical to reducing switching noise and transients.

8.2.1.2.8 Soft-Start Capacitor Selection

The capacitor at the SS pin determines the soft-start time, that is the time for the output voltage to reach its final steady-state value. The capacitor value is determined from Equation 15:

$$C_{SS} \quad \frac{I_{SS} \times T_{Startup}}{V_{SS}} \tag{15}$$

With $C_{(SS)}$ set at 22 nF and the V(SS) = 2 V, $I_{(SS)}$ = 10 µA, the $T_{Startup}$ should measure approximately 4 ms.

8.2.1.2.9 EN/UVLO Resistor Selection

The UVLO resistors R3 (R_{UV2}) and R9 (R_{UV1}) set the input undervoltage lockout threshold and hysteresis according to Equation 16 and Equation 17:

$$V_{IN(HYS)} = I_{UVLO(HYS)} \times R_{UV2} \tag{16}$$

and,

$$V_{IN,\,UVLO(rising)} \quad V_{UVLO(TH)} \left(1 + \frac{R_{UV2}}{R_{UV1}}\right) \tag{17}$$

From the *Electrical Characteristics*, $I_{UVLO(HYS)}$ = 20 µA (typical). To design for V_{IN} rising threshold ($V_{IN,\,UVLO(rising)}$) at 15 V and EN/UVLO hysteresis of 1.5 V, Equation 16 and Equation 17 yield R_{UV1} = 6.81 kΩ and R_{UV2} = 75 kΩ. Selecting 1% standard value of R_{UV1} = 6.81 kΩ and R_{UV2} = 75 kΩ results in UVLO threshold (rising) and hysteresis of 14.9 V and 1.5 V respectively.

8.2.1.3 Application Curves

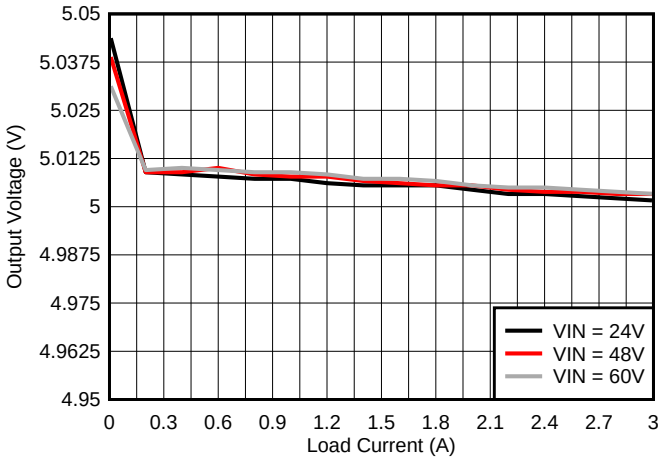


Figure 14. Load Regulation

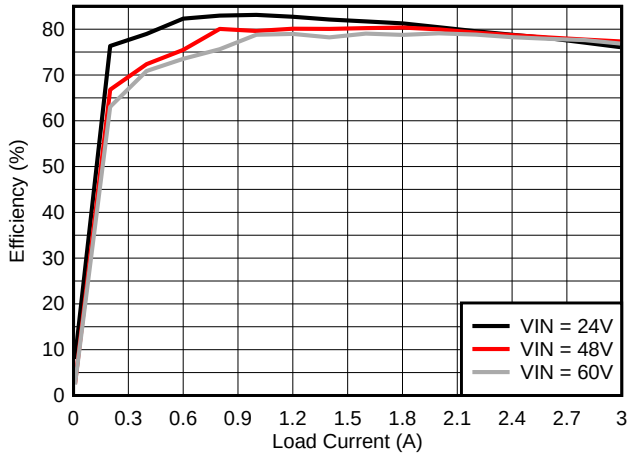


Figure 15. Efficiency vs I_{OUT}

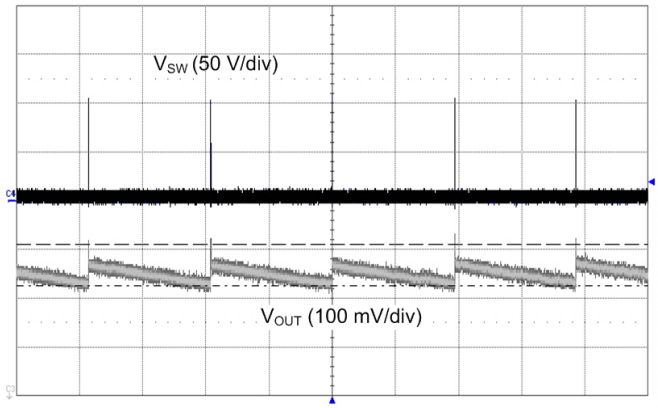


Figure 16. Steady State

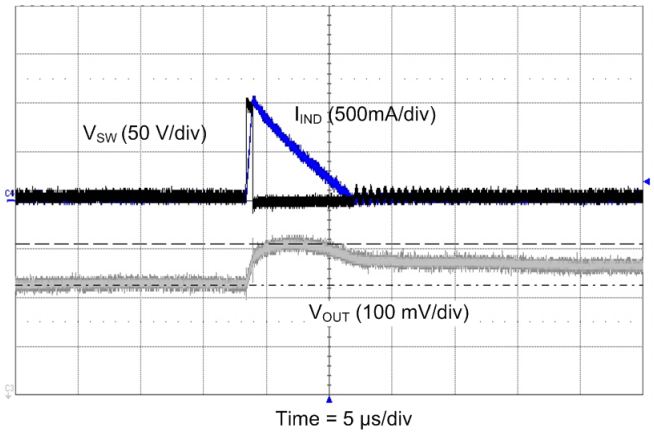


Figure 17. Steady State (Zoomed-In)

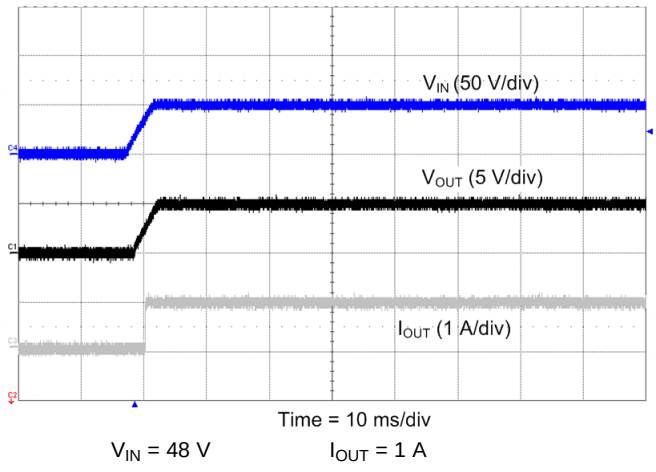


Figure 18. Start-up

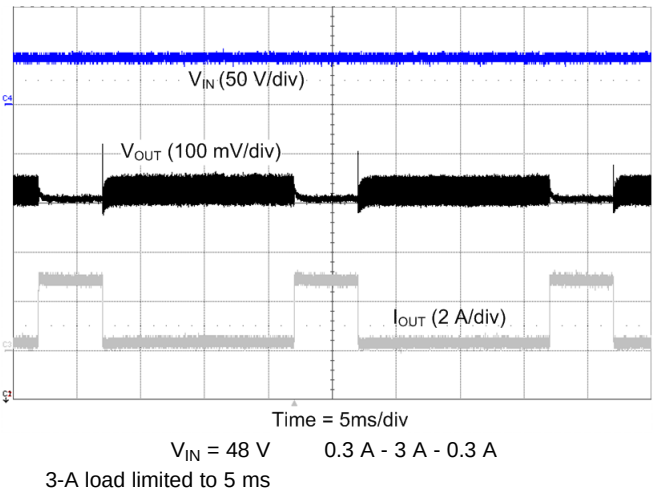


Figure 19. Load Transient

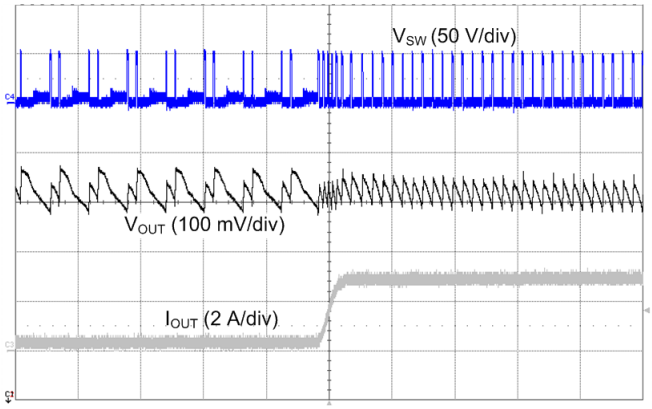


Figure 20. Load Transient

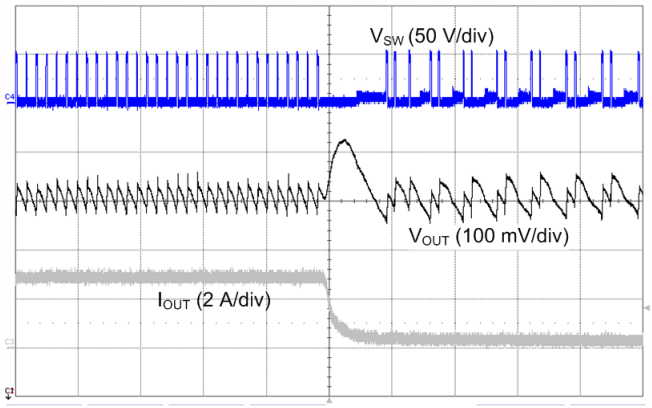


Figure 21. Load Transient

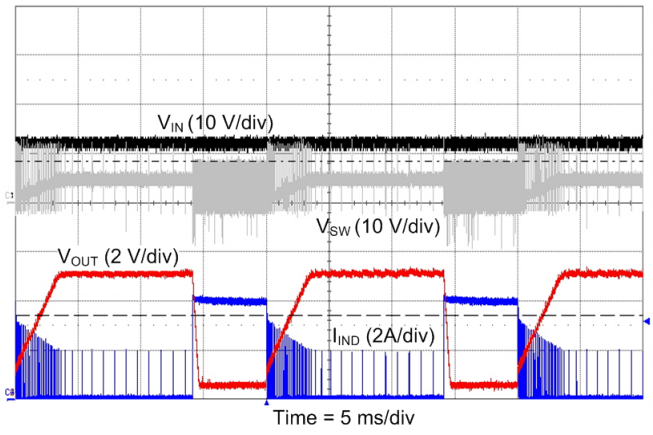


Figure 22. Output Overload

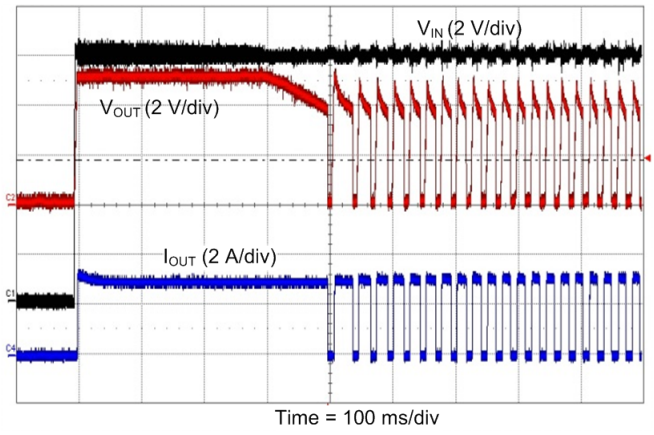


Figure 23. Overtemperature Thermal Shutdown Protection

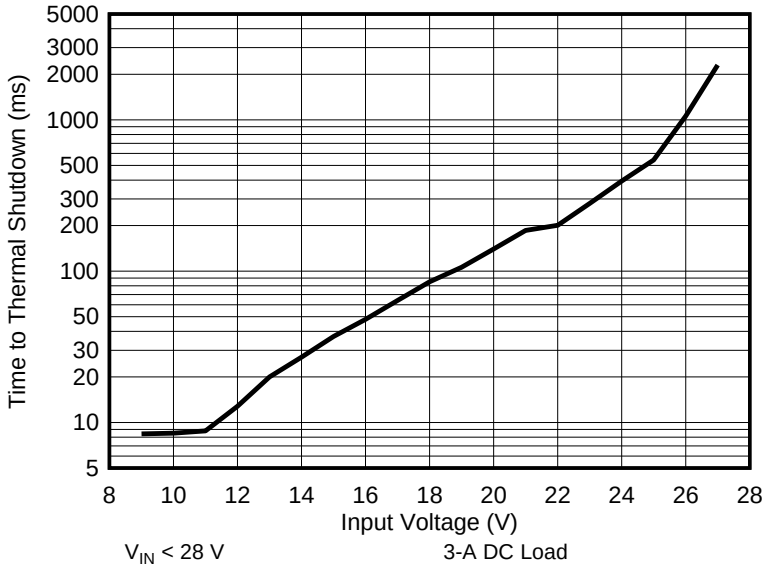


Figure 24. Time to Trigger Thermal Shutdown

8.2.2 Ripple Configuration

LM34940 uses a constant-on-time (COT) control scheme, in which the ON time is terminated by a one-shot, and the OFF time is terminated by the feedback voltage (V_{FB}) falling below the reference voltage. Therefore, for stable operation, the feedback voltage must decrease monotonically and in phase with the inductor current during the OFF time. Furthermore, this change in feedback voltage (V_{FB}) during OFF time must be large enough to dominate any noise present at the feedback node.

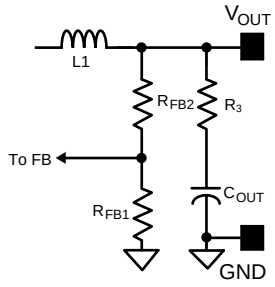
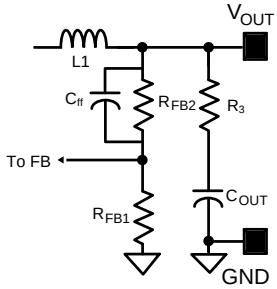
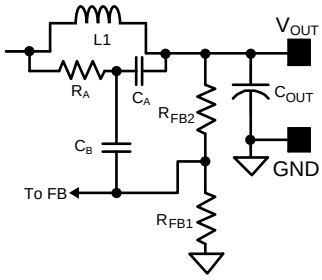
Table 3 presents three different methods for generating appropriate voltage ripple at the feedback node. Type 1 and Type 2 ripple circuits couple the ripple from the output of the converter to the feedback node (FB). The output voltage ripple has two components:

1. Capacitive ripple caused by the inductor current ripple charging or discharging the output capacitor.
2. Resistive ripple caused by the inductor current ripple flowing through the ESR of the output capacitor and R3.

The capacitive ripple is out-of-phase with the inductor current. As a result, the capacitive ripple does not decrease monotonically during the OFF time. The resistive ripple is in phase with the inductor current and decreases monotonically during the OFF time. The resistive ripple must exceed the capacitive ripple at output (V_{OUT}) for stable operation. If this condition is not satisfied unstable switching behavior is observed in COT converters, with multiple ON time bursts in close succession followed by a long OFF time.

Type 3 ripple method, as used in the application example given in *Typical Application*, uses a ripple injection circuit with R_A, C_A and the switch node (SW) voltage to generate a triangular ramp. This triangular ramp is then AC-coupled into the feedback node (FB) using the capacitor C_B. Because this circuit does not use the output voltage ripple, it is suited for applications where low output voltage ripple is imperative. See *Controlling Output Ripple and Achieving ESR Independence in Constant On-Time (COT) Regulator Designs* for more details for each ripple generation method.

Table 3. Ripple Configuration

TYPE 1	TYPE 2	TYPE 3
Lowest Cost	Reduced Ripple	Minimum Ripple
 Copyright © 2016, Texas Instruments Incorporated	 Copyright © 2016, Texas Instruments Incorporated	 Copyright © 2016, Texas Instruments Incorporated
$R_3 \geq \frac{25\ mV \times V_O}{V_{REF} \times \Delta I_{L1,min}}$ (18)	$C_{ff} \geq \frac{5}{F_{SW} \times (R_{FB2} \text{ IIR}_{FB1})}$ $R_3 \geq \frac{25\ mV}{\Delta I_{L1,min}}$ (19)	$R_A C_A \leq \frac{(V_{IN,min} - V_O) \times T_{ON(@\,V_{IN,min})}}{25mV}$ (20)

8.3 Dos and Don'ts

As mentioned earlier in *Soft Start*, the SS capacitor $C_{(SS)}$, must be more than 1 nF. Apart from determining the startup time, this capacitor serves for the external compensation of the internal G_M error amplifier. A minimum value of 1 nF is necessary to maintain stability. The SS pin must not be left floating.

A minimum load current of 1 mA is required to maintain proper operation. If the load current falls below that level, the bootstrap capacitor can discharge during the long off-time and the circuit either shuts down or cycles on and off at a low frequency. If the load current is expected to drop below 1 mA in the application, choose the feedback resistors to be low enough in value to provide the minimum required current at nominal V_{OUT}. Also, the designer can increase the boot capacitor value so that during no load boot capacitor is not discharged below the gate threshold of high-side switch before V_{OUT}, and hence V_{FB}, falls below the reference. The hiccup-free operation should be verified for whole input voltage range. Extending this requirement, a 220-nF BST capacitor is used in the *Typical Application*.

9 Power Supply Recommendations

The LM34940 is designed to operate with an input power supply capable of supplying up to 100 V. The power supply must be well regulated and capable of supplying sufficient current to the regulator during the buck mode. As in all DC-DC applications, the power supply source impedance must be small compared to the converter input impedance in order to maintain the stability of the converter.

If the LM34940 is used in a buck topology with low input supply voltage (4.5 V) and large load current, it is prudent to add a large electrolytic capacitor, in parallel the C_{IN} capacitors. The electrolytic capacitor stabilizes the input voltage to the device and prevents droop or oscillation over the entire load range. Also, add an electrolytic capacitor, or a ceramic capacitor in series with appropriate ESR, parallel to the input capacitors C_{IN}, in order to dampen the input voltage spikes detected by the LM34940 when connected to a power supply with long power leads. These input voltage spikes can easily be twice the input voltage step amplitude, and a damping capacitor is necessary to contain the input voltage to less than 100 V in order to protect the LM34940.

10 Layout

10.1 Layout Guidelines

A proper layout is essential for optimum performance of the circuit. In particular, observe the following layout guidelines:

- C_{IN}: The loop consisting of input capacitor (C_{IN}), VIN pin, and PGND pin carries the switching current. Therefore, in the LM34940, the input capacitor must be placed close to the LM34940 device, directly across VIN and PGND pins, and the connections to these two pins must be direct to minimize the loop area. In general it is not possible to place all of input capacitances near the device. However, a good layout practice includes placing the bulk capacitor as close as possible to the VIN pin (see Figure 25). When using the LM34940 14-pin HTSSOP package, a bypass capacitor (C_{byp}) measuring approximately 0.1 µF must be placed directly across VIN and PGND (pin 3 and 2), as close as possible to the LM34940 device while complying with all layout design rules.
- Place the R_{ON} resistor between the VIN and the RON pin and the SS capacitor as close as possible to their respective pins.
- C_{VCC} and C_{BST}: The bootstrap (BST) bypass capacitor supplies switching current to the high-side gate driver. This capacitor should be placed as close as possible to the LM34940 device, and the connecting trace lengths and the loop area must be kept at minimum (see Figure 25).
- The feedback trace carries the output voltage information and a small ripple component that is necessary for proper operation of the LM34940. Therefore, care must be taken while routing the feedback trace to avoid coupling any noise into this pin. In particular, the feedback trace must be short and not run close to magnetic components, or parallel to any other switching trace.
- If a ripple injection circuit is being used for ripple generation at the FB pin, it is considered a good layout practice to lay out the feedback ripple injection DC trace and the V_{OUT} trace differentially. This scheme helps in reducing the scope for any noise injection at the FB pin.
- SW trace: The SW node switches rapidly between VIN and GND every cycle and is therefore a source of noise. The SW node area must be kept at minimum. In particular, the SW node must not be inadvertently connected to a copper plane or pour.

10.2 Layout Example

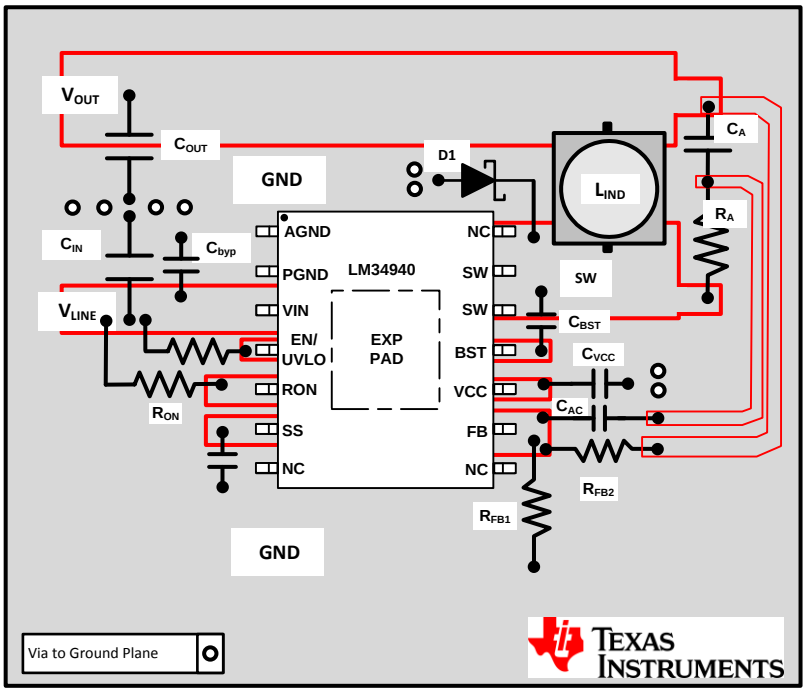


Figure 25. Typical Buck Layout Example With the LM34940

11 Device and Documentation Support

11.1 Trademarks

All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Package Option Addendum

12.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (3)	MSL Peak Temp (4)	Op Temp (°C)	Device Marking (5) (6)
LM34940PWPR	ACTIVE	HTSSOP	PWP	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	LM 34940
LM34940PWPT	ACTIVE	HTSSOP	PWP	14	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	LM 34940

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check or the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

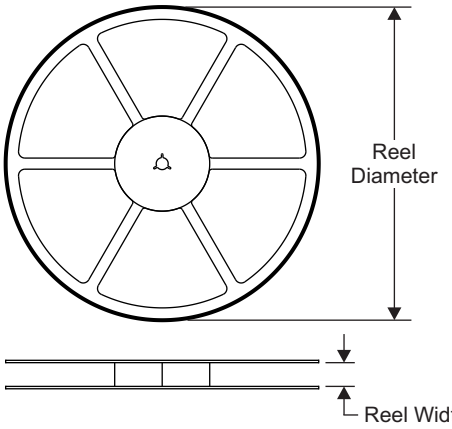
(4) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

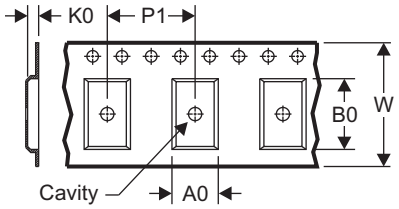
(6) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

12.1.2 Tape and Reel Information

REEL DIMENSIONS

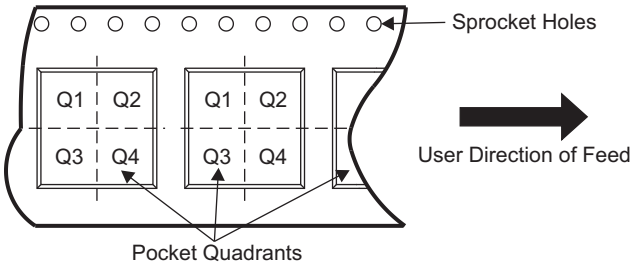


TAPE DIMENSIONS



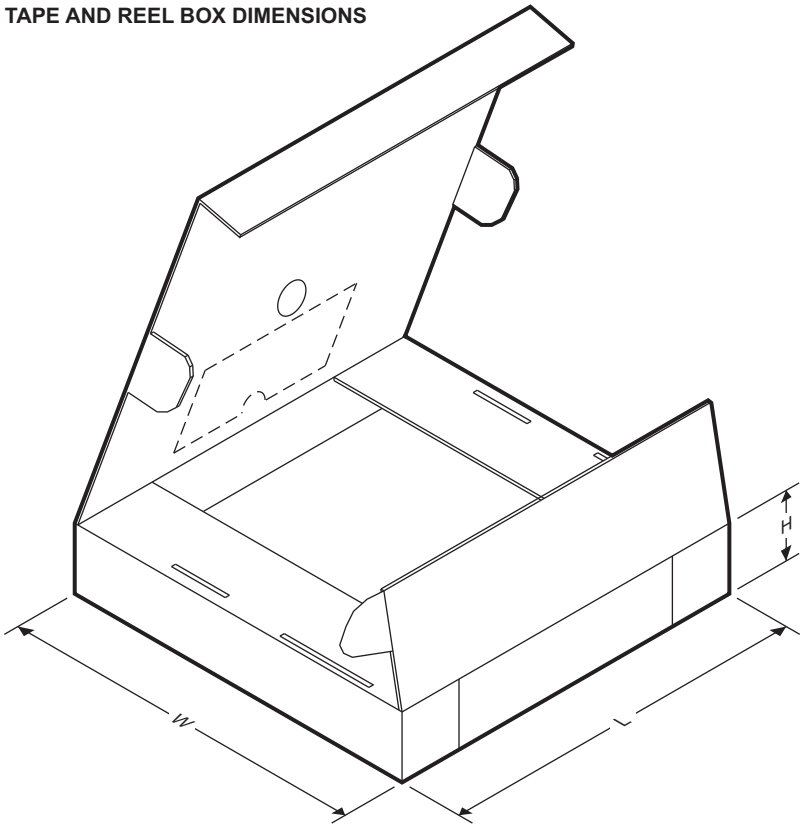
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



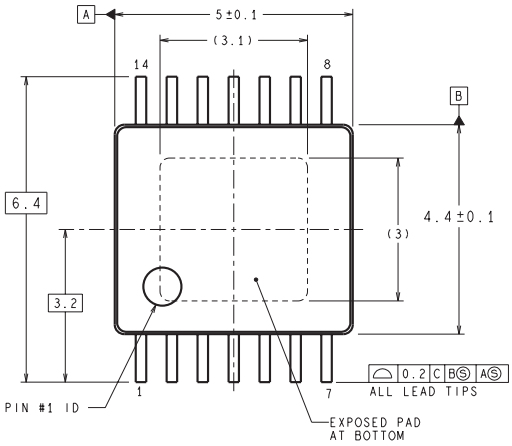
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM34940PWPR	HTSSOP	PWP	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LM34940PWPT	HTSSOP	PWP	14	250	178.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

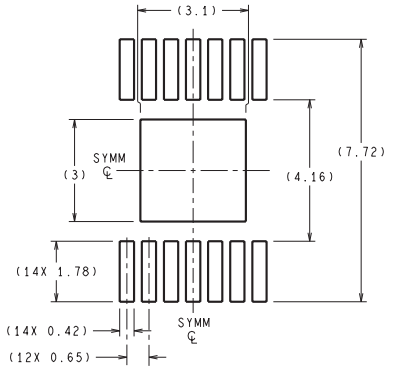
TAPE AND REEL BOX DIMENSIONS



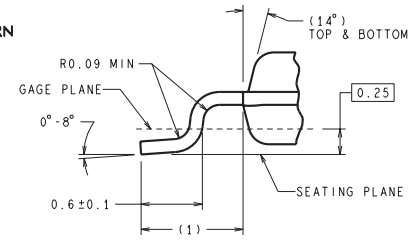
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM34940PWPR	HTSSOP	PWP	14	2500	367.0	367.0	35.0
LM34940PWPT	HTSSOP	PWP	14	250	210.0	185.0	35.0

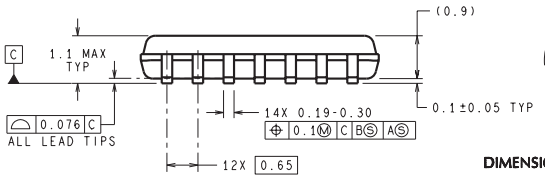
PWP0014A

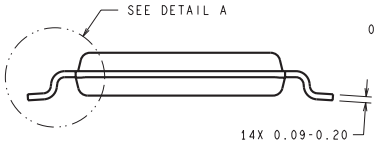




RECOMMENDED LAND PATTERN







DIMENSIONS ARE IN MILLIMETERS

MXA14A (Rev A)

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