

APL3518 / 9

USB Power-Distribution Switches

Features

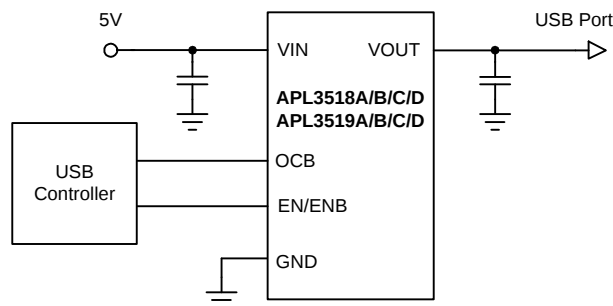
- **62mW High Side MOSFET**
- **Wide Supply Voltage Range: 2.7V to 5.5V**
- **Current-Limit and Short-Circuit Protections**
- **Over-Temperature Protection**
- **Fault Indication Output**
- **Enable Input**
- **UL Approved-File No. E328191**
- **Nemko IEC 60950-1:2005(2nd Edition); Am 1:2009 CB Scheme Certified, No.62377**
- **TUV IEC 60950-1:2005+A1:2009 and EN 60950-1:2006+A11:2009+A1:2010 Certified, No.44 780 11 393954**
- **Lead Free and Green Devices Available (RoHS Compliant)**

General Description

The APL3518/9 series of power switches are designed for USB applications. The 62mΩ N-channel MOSFET power switch satisfies the voltage drop requirements of USB specification.

The protection features include current-limit protection, short-circuit protection, and over-temperature protection. The device limits the output current at current limit threshold level. When V_{OUT} drops below 1.5V, the devices limit the current to a lower and safe level. The over-temperature protection limits the junction temperature below 140°C in case of short circuit or over load conditions. Other features include a deglitched OCB output to indicate the fault condition and an enable input to enable or disable the device.

Simplified Application Circuit

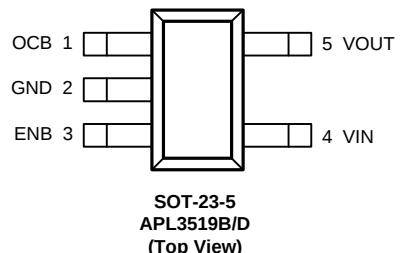
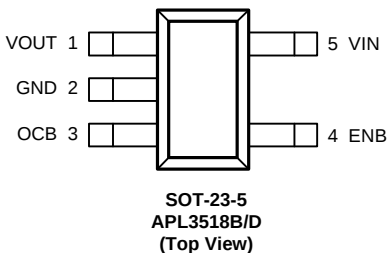
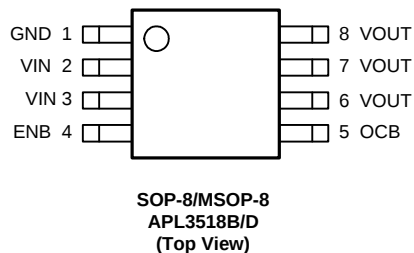
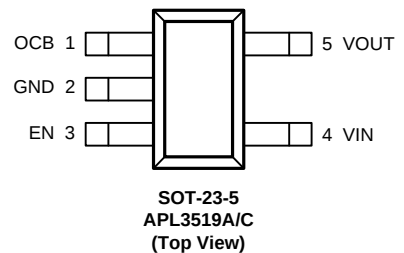
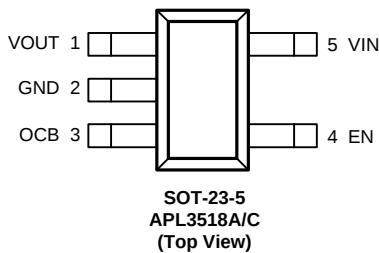
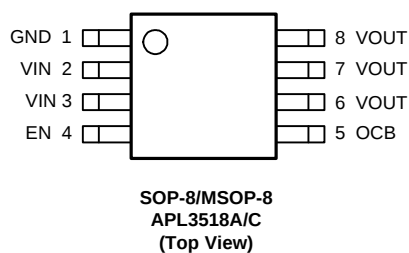


Applications

- **Notebook and Desktop Computers**
- **USB Ports**
- **High-Side Power Protection Switches**

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Pin Configurations



Ordering and Marking Information

APL3518 □□□-□□□ APL3519 Assembly Material Handling Code Temperature Range Package Code Output Current/EN Function	Package Code K : SOP-8 X : MSOP-8 B : SOT-23-5 Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel Output Current/EN Function A : 1.5A/Active High B : 1.5A/Active Low C : 1A/Active High D : 1A/Active Low Assembly Material G : Halogen and Lead Free Device
APL3518A K: APL3518A XXXXX ●	XXXXX - Date Code
APL3518A X: L518A XXX ● XX	XXXXX - Date Code
APL3518A B: L8AX	X - Date Code
APL3519A B: L9AX	X - Date Code

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

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Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{IN}	VIN Input Voltage (VIN to GND)	-0.3 ~ 7	V
V_{IN_PEAK}	VIN Input Peak Voltage (width<10 μ s)	9	V
V_{OUT}	VOUT to GND Voltage	-0.3 ~ 7	V
V_{ENB}, V_{EN}	EN, ENB to GND Voltage	-0.3 ~ 7	V
V_{OCB}	OCB to GND Voltage	-0.3 ~ 7	V
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in Free Air ^(Note 2) SOP-8 MSOP-8 SOT-23-5	160 160 235	°C/W

Note 2 : θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{IN}	VIN Input Voltage	2.7 ~ 5.5	V
I_{OUT}	OUT Output Current (APL3518A/B, APL3519A/B)	0 ~1.5	A
	OUT Output Current (APL3518C/D, APL3519C/D)	0 ~1	
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3 : Refer to the typical application circuit

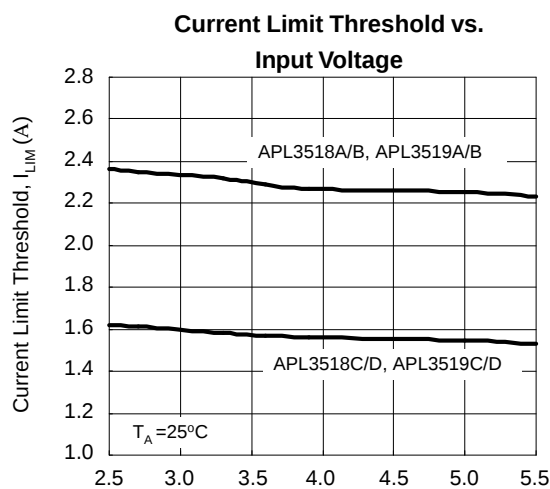
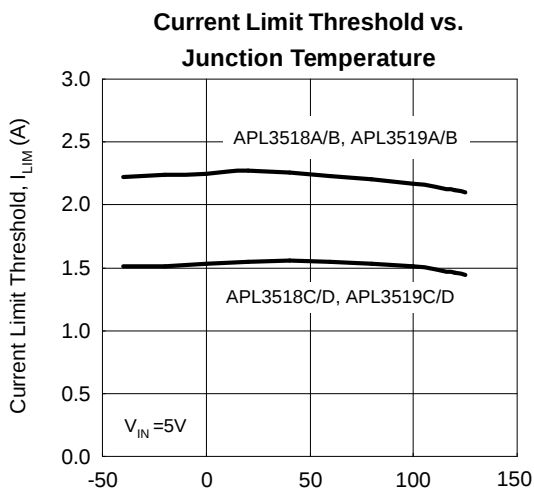
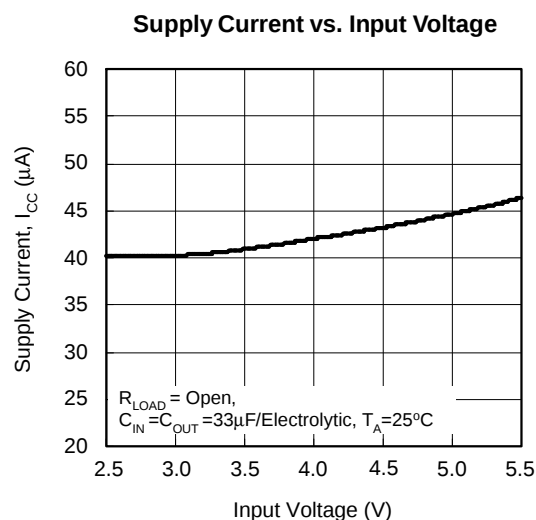
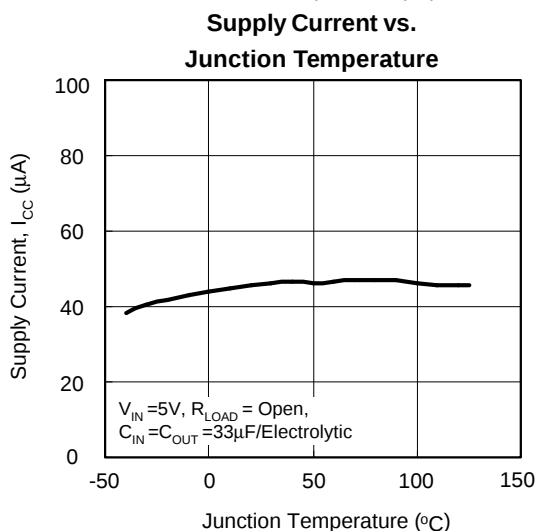
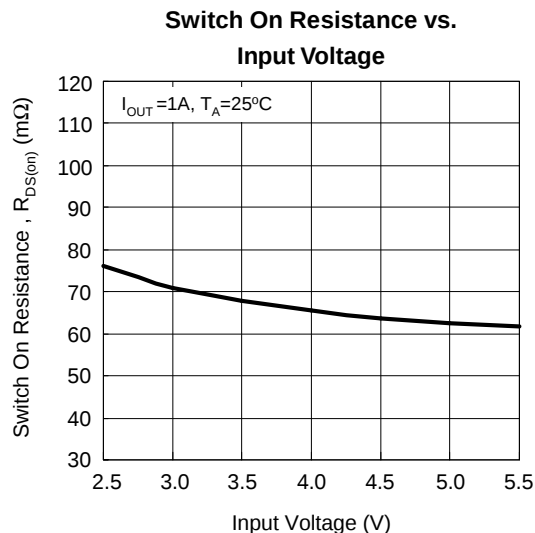
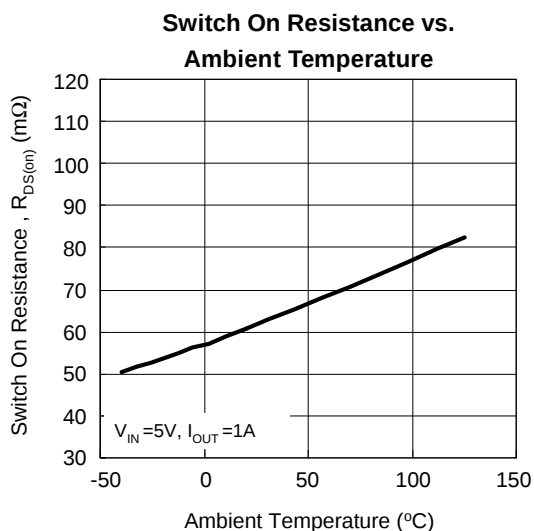
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Electrical Characteristics

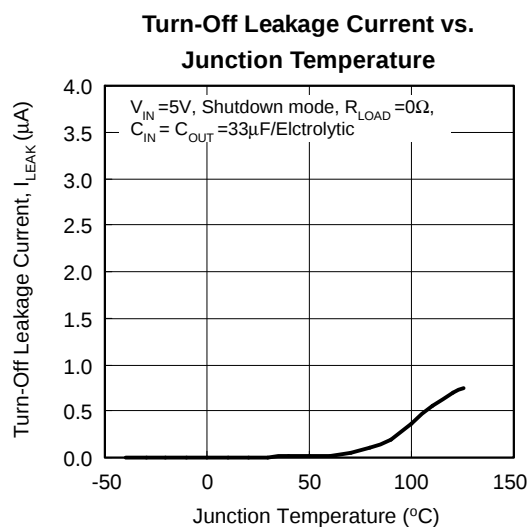
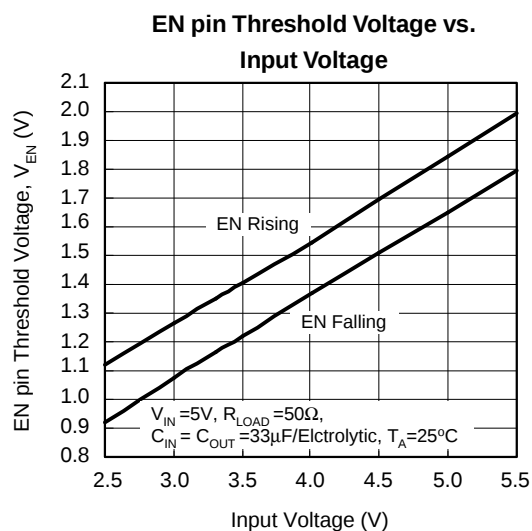
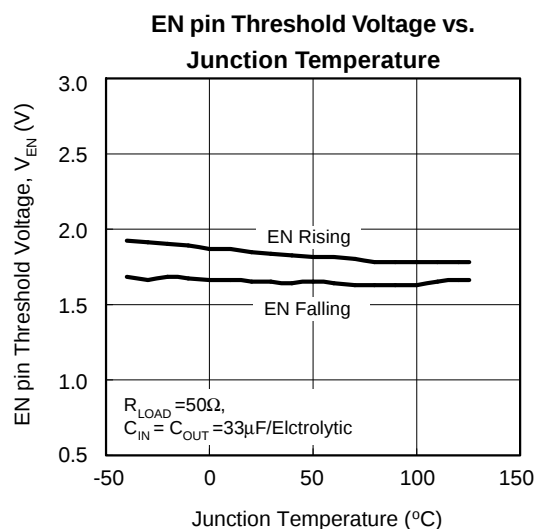
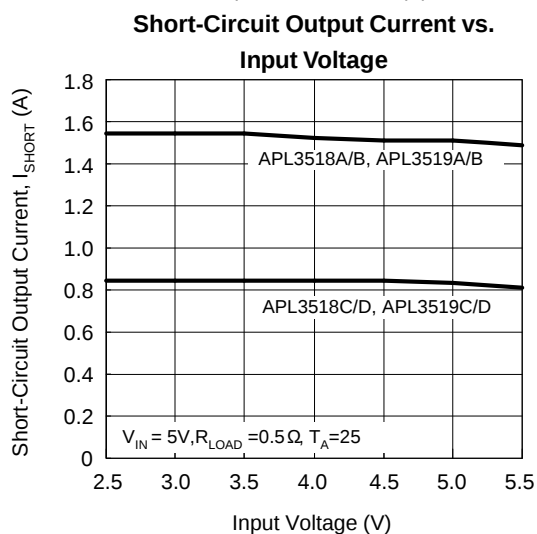
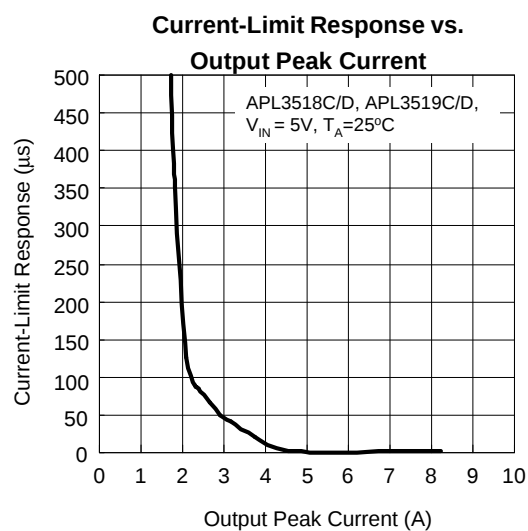
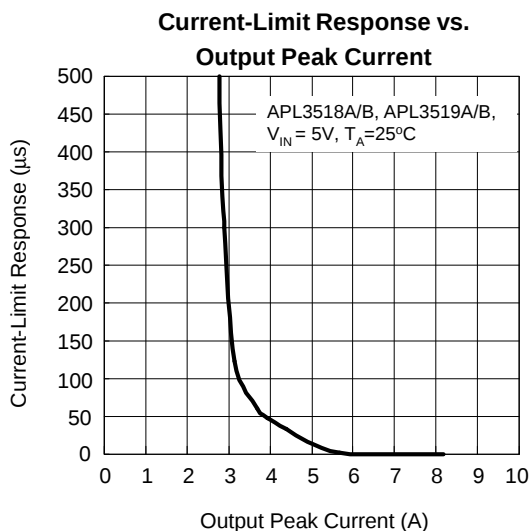
Unless otherwise specified, these specifications apply over $V_{IN}=5V$, $V_{EN}=5V$ or $V_{ENB}=0V$ and $T_A = -40 \sim 85^\circ C$. Typical values are at $T_A=25^\circ C$.

Symbol	Parameter	Test Conditions	APL3518/9			Unit	
			Min.	Typ.	Max.		
SUPPLY CURRENT							
	VIN Supply Current	No load, VEN=0V or VENB=5V	-	-	1	μA	
		No load, VEN=5V or VENB=0V	-	60	100	μA	
	Leakage Current	VOUT=GND, VEN=0V or VENB=5V	-	-	1	μA	
	Reverse Leakage Current	VIN=GND, VOUT=5V, VEN=0V or VENB=5V	-	-	1	μA	
POWER SWITCH							
RDS(ON)	Power Switch On Resistance	APL3518A/B/C/D, APL3519A/B/C/D, TA= 25 °C	IOUT=1A	-	62	72	mΩ
			IOUT=2A	-	62	75	mΩ
UNDER-VOLTAGE LOCKOUT (UVLO)							
	VIN UVLO Threshold Voltage	VIN rising, TA= -40 ~ 85 °C	1.7	-	2.65	V	
	VIN UVLO Hysteresis		-	0.2	-	V	
CURRENT-LIMIT AND SHORT-CIRCUIT PROTECTIONS							
I LIM	Current Limit Threshold	APL3518A/B, APL3519A/B, VIN=2.7V to 5.5V, TA= -40 ~ 85 °C	2.1	2.5	3.6	A	
		APL3518C/D, APL3519C/D, VIN=2.7V to 5.5V, TA= -40 ~ 85 °C	1.1	1.5	2.1	A	
I SHORT	Short-Circuit Output Current	APL3518A/B, APL3519A/B, VIN=2.7V to 5.5V	-	1.5	-	A	
		APL3518C/D, APL3519C/D, VIN=2.7V to 5.5V	-	0.8	-	A	
OCB OUTPUT PIN							
	OCB Output Low Voltage	I OCB=5mA	-	0.2	0.4	V	
	OCB Leakage Current	V OCB=5V	-	-	1	μA	
t D(OCB)	OCB Deglitch Time	OCB assertion, TA= -40 ~ 85 °C	5	12	20	ms	
EN OR ENB INPUT PIN							
V IH	Input Logic HIGH	VIN=2.7V to 5V	2	-	-	V	
V IL	Input Logic LOW	VIN=2.7V to 5V	-	-	0.8	V	
	Input Current		-	-	1	μA	
	VOUT Discharge Resistance	VEN=0V or VENB=5V, VOUT=1V	-	40	-	Ω	
t D(ON)	Turn On Delay Time		-	30	-	μs	
t D(OFF)	Turn Off Delay Time		-	30	-	μs	
t SS	Soft-Start Time	No load, COUT=1μF, VIN=5V	-	400	-	μs	
OVER-TEMPERATURE PROTECTION (OTP)							
T OTP	Over-Temperature Threshold	TJ rising	-	140	-	°C	
	Over-Temperature Hysteresis		-	20	-	°C	

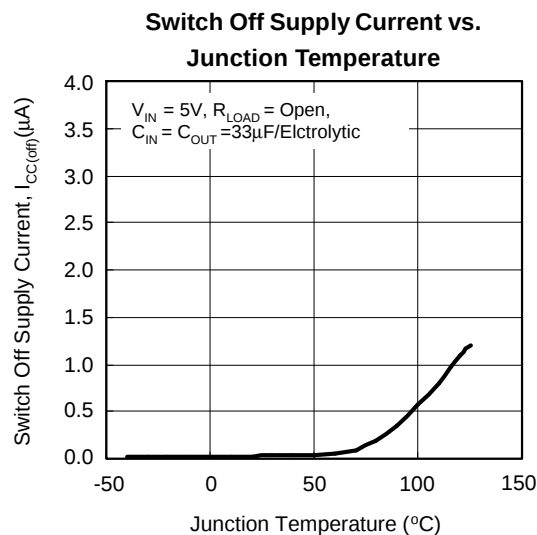
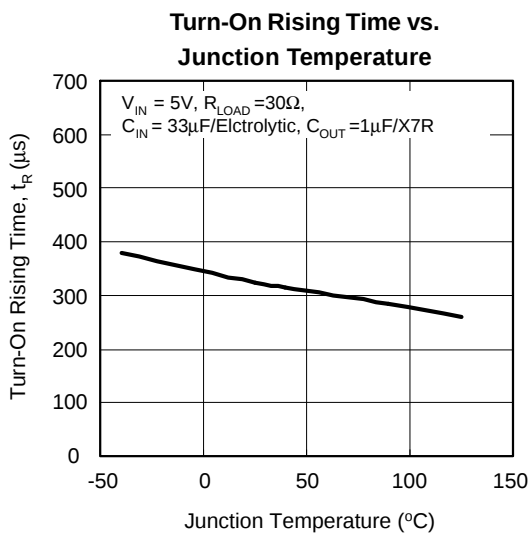
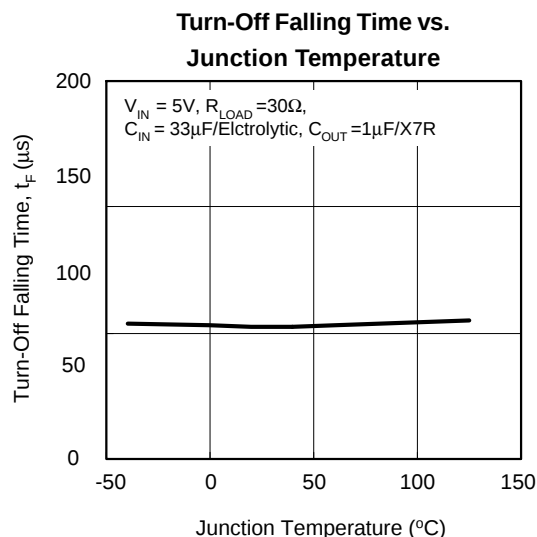
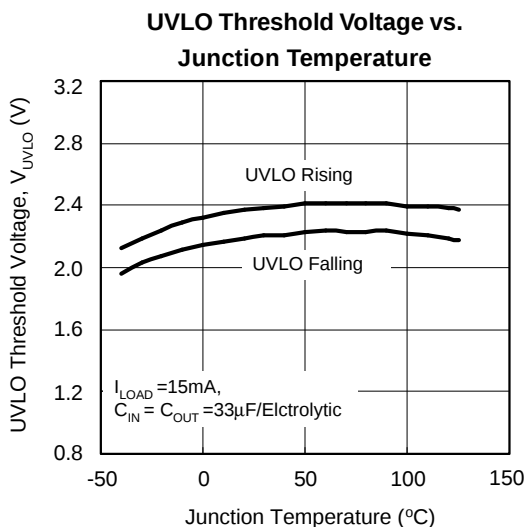
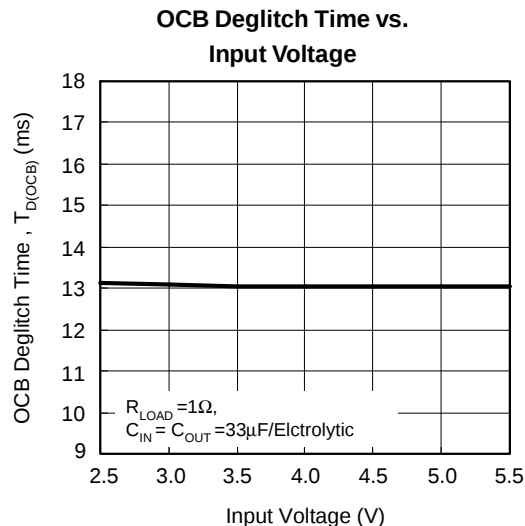
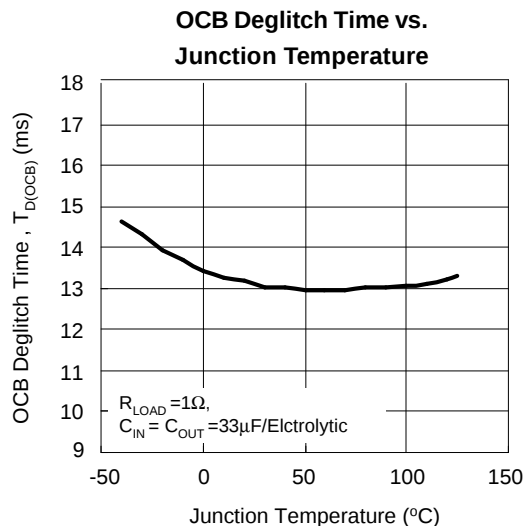
Typical Operating Characteristics



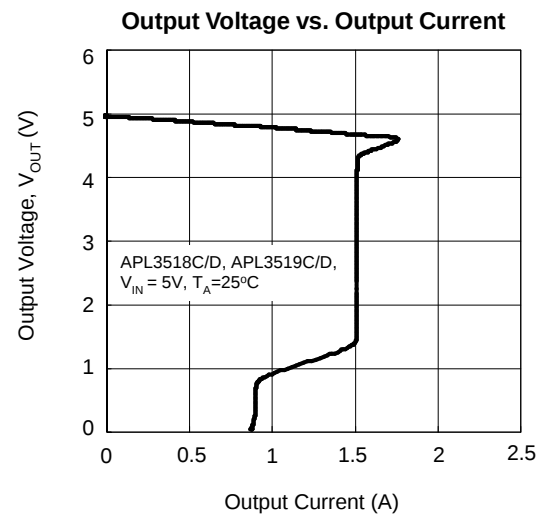
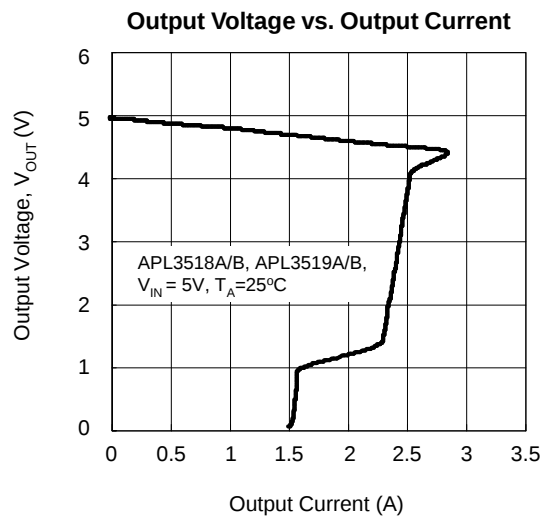
Typical Operating Characteristics (Cont.)



Typical Operating Characteristics (Cont.)



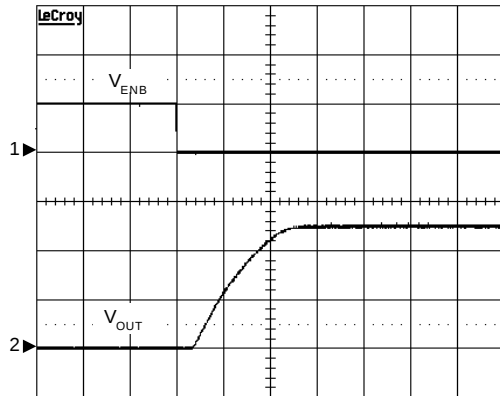
Typical Operating Characteristics (Cont.)



Operating Waveforms

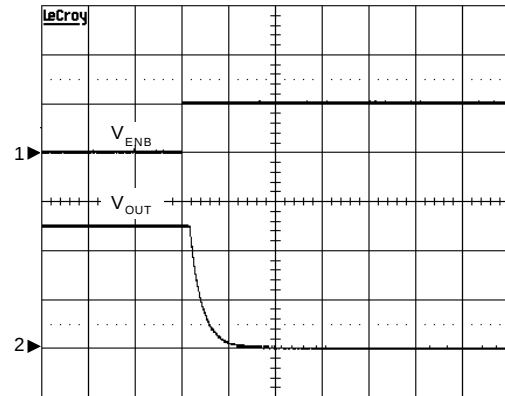
The test condition is $V_{IN}=5V$, $T_A=25^{\circ}C$ unless otherwise specified.

Turn On Response



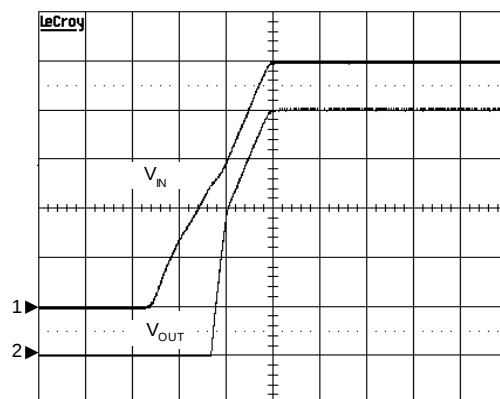
$V_{IN}=5V$, $R_{LOAD}=30\Omega$, $C_{IN}=33\mu F$ /Electrolytic,
 $C_{OUT}=1\mu F$ /Electrolytic
 CH1: V_{ENB} , 5V/Div, DC
 CH2: V_{OUT} , 2V/Div, DC
 TIME: 200 μs /Div

Turn Off Response



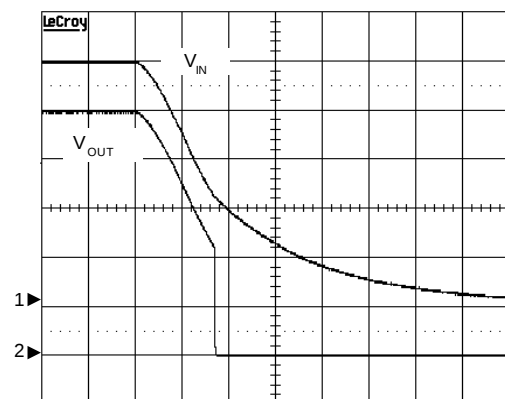
$V_{IN}=5V$, $R_{LOAD}=30\Omega$, $C_{IN}=33\mu F$ /Electrolytic,
 $C_{OUT}=1\mu F$ /Electrolytic
 CH1: V_{ENB} , 5V/Div, DC
 CH2: V_{OUT} , 2V/Div, DC
 TIME: 100 μs /Div

UVLO at Rising



$V_{IN}=5V$, $R_{LOAD}=30\Omega$, $C_{IN}=33\mu F$ /Electrolytic,
 $C_{OUT}=1\mu F$ /Electrolytic
 CH1: V_{IN} , 1V/Div, DC
 CH2: V_{OUT} , 1V/Div, DC
 TIME: 2ms/Div

UVLO at Falling



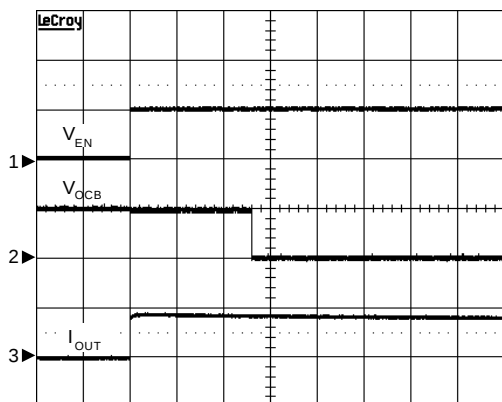
$V_{IN}=5V$, $R_{LOAD}=30\Omega$, $C_{IN}=33\mu F$ /Electrolytic,
 $C_{OUT}=1\mu F$ /Electrolytic
 CH1: V_{IN} , 1V/Div, DC
 CH2: V_{OUT} , 1V/Div, DC
 TIME: 5ms/Div

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Operating Waveforms (Cont.)

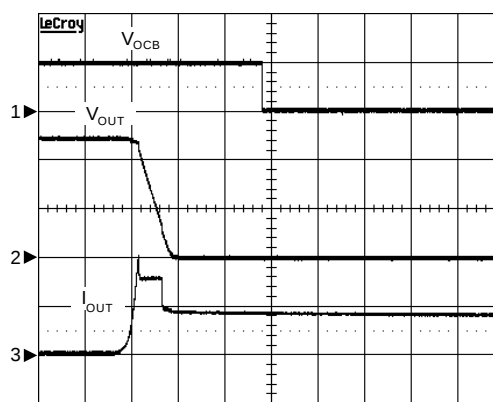
The test condition is $V_{IN}=5V$, $T_A=25^{\circ}C$ unless otherwise specified.

OCB Response during Short Circuit



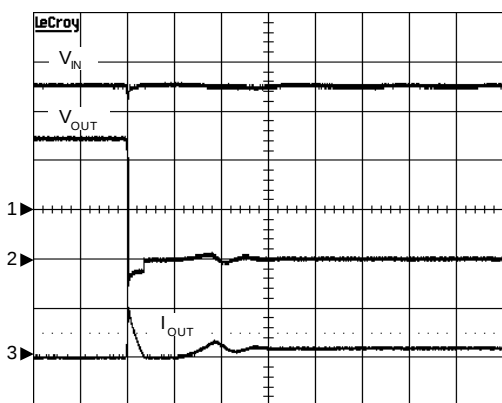
APL3518C, $V_{IN}=5V$, OUT short to GND,
 $C_{IN}=C_{OUT}=33\mu F$ /Electrolytic
 CH1: V_{EN} , 5V/Div, DC
 CH2: V_{OCB} , 5V/Div, DC
 CH3: I_{OUT} , 1A/Div, DC
 TIME: 5ms/Div

OCB Response with Ramped Load



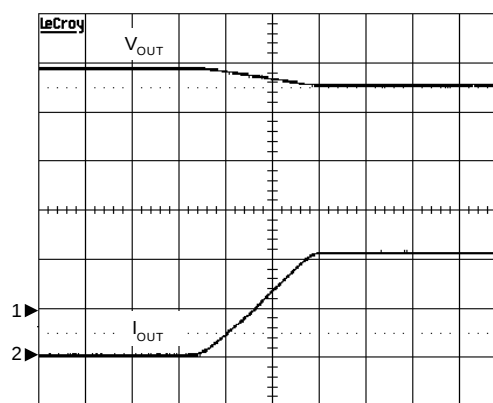
APL3518C, $V_{IN}=5V$, $C_{IN}=C_{OUT}=33\mu F$ /Electrolytic
 CH1: V_{OCB} , 5V/Div, DC
 CH2: V_{OUT} , 2V/Div, DC
 CH3: I_{OUT} , 1A/Div, DC
 TIME: 5ms/Div

Short Circuit Response



APL3518C, $V_{IN}=5V$, OUT Short to GND,
 $C_{IN}=33\mu F$ /Electrolytic, No C_{OUT}
 CH1: V_{IN} , 2V/Div, DC
 CH2: V_{OUT} , 2V/Div, DC
 CH3: I_{OUT} , 5A/Div, DC
 TIME: 50 μs /Div

Load Transient Response



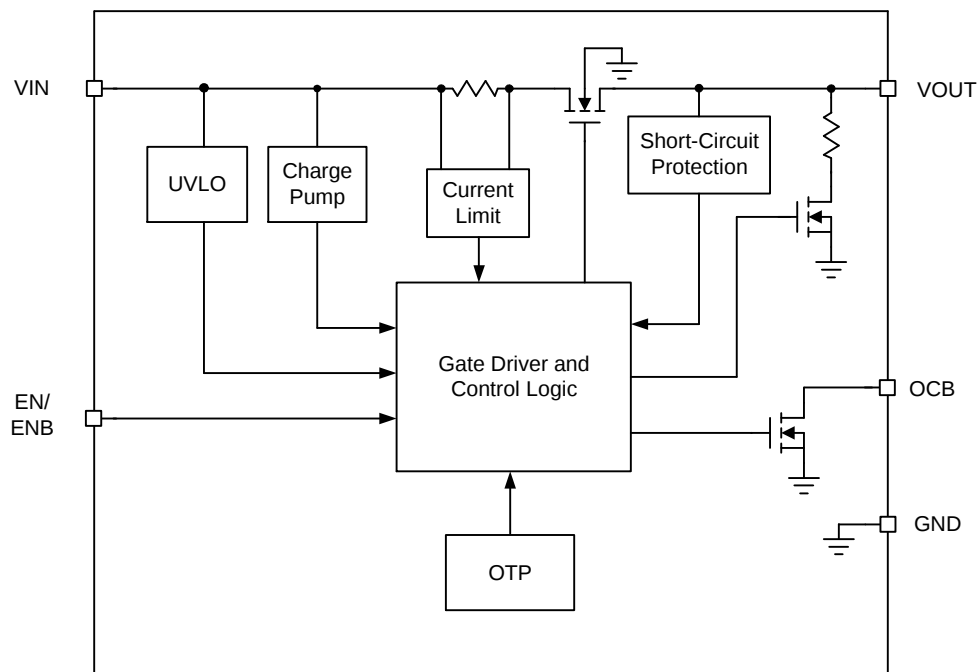
APL3518A, $V_{IN}=5V$, $R_{LOAD}=1k\Omega$ to 2.2Ω ,
 $C_{IN}=C_{OUT}=33\mu F$ /Electrolytic
 CH1: V_{OUT} , 1V/Div, DC
 CH2: I_{OUT} , 1A/Div, DC
 TIME: 1ms/Div

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Pin Description

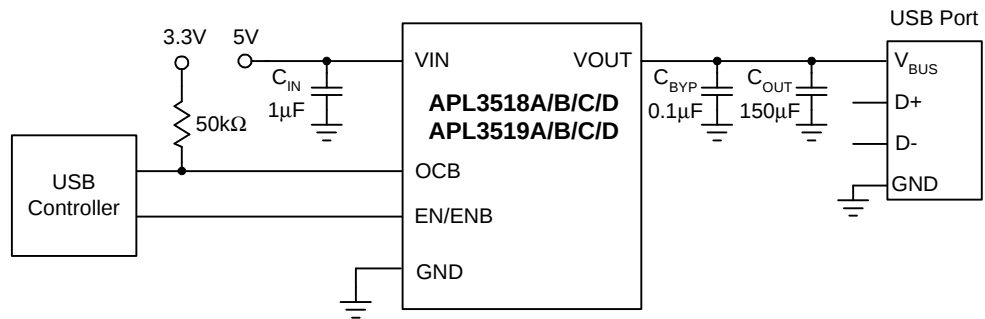
PIN				FUNCTION
NO.			NAME	
SOP-8/ MSOP-8	SOT-23-5			
	APL3518	APL3519		
1	2	2	GND	Ground.
2	5	4	VIN	Power Supply Input. Connect this pin to external DC supply.
3				
4	4	3	EN (A/C)	Enable Input. Pulling this pin to high will enable the device and pulling this pin to low will disable device. The EN pin cannot be left floating.
			ENB (B/D)	Enable Input. Pulling this pin to high will disable the device and pulling this pin to low will enable device. The ENB pin cannot be left floating.
5	3	1	OCB	Fault Indication Pin. This pin goes low when a current limit or an over-temperature condition is detected after a 12ms deglitch time.
6	1	5	VOUT	Output Voltage Pin. The output voltage follows the input voltage. When ENB is high or EN is low, the output voltage is discharged by an internal resistor.
7				
8				

Block Diagram



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Typical Application Circuit



Function Description

VIN Under-Voltage Lockout (UVLO)

The APL3518/9 series of power switches have a built-in under-voltage lockout circuit to keep the output shutting off until internal circuitry is operating properly. The UVLO circuit has hysteresis and a de-glitch feature so that it will typically ignore undershoot transients on the input. When input voltage exceeds the UVLO threshold, the output voltage starts a soft-start to reduce the inrush current.

Power Switch

The power switch is an N-channel MOSFET with a low $R_{DS(ON)}$. The internal power MOSFET does not have the body diode. When IC is off, the MOSFET prevents a current flowing from the VOUT back to VIN and VIN to VOUT.

Current-Limit Protection

The APL3518/9 series of power switches provide the current-limit protection function. During current-limit, the devices limit output current at current limit threshold. For reliable operation, the device should not be operated in current-limit for extended period.

Short-Circuit Protection

When the output voltage drops below 1.5V, which is caused by an over-load or a short-circuit, the devices limit the output current down to a safe level. The short-circuit current limit is used to reduce the power dissipation during short-circuit conditions. If the junction temperature reaches over-temperature threshold, the device will enter the thermal shutdown.

OCB Output

The APL3518/9 series of power switches provide an open-drain output to indicate that a fault has occurred. When any of current-limit or over-temperature protection occurs for a deglitch time of $t_{D(OCB)}$, the OCB goes low. Since the OCB pin is an open-drain output, connecting a resistor to a pull high voltage is necessary.

Enable/Disable

Pull the ENB above 2V or EN below 0.8V will disable the device, and pull ENB pin below 0.8V or EN above 2V will enable the device. When the IC is disabled, the supply current is reduced to less than 1 μ A. The enable input is

compatible with both TTL and CMOS logic levels. The EN/ENB pin cannot be left floating.

Over-Temperature Protection

When the junction temperature exceeds 140°C, the internal thermal sense circuit turns off the power FET and allows the device to cool down. When the device's junction temperature cools by 20°C, the internal thermal sense circuit will enable the device, resulting in a pulsed output during continuous thermal protection. Thermal protection is designed to protect the IC in the event of over temperature conditions. For normal operation, the junction temperature cannot exceed $T_J=+125^{\circ}\text{C}$.

Application Information

Input Capacitor

A 1 μ F ceramic bypass capacitor from V_{IN} to GND, located near the APL3518/9, is strongly recommended to suppress the ringing during short circuit fault event. Without the bypass capacitor, the output short may cause sufficient ringing on the input (from supply lead inductance) to damage internal control circuitry.

Output Capacitor

A low-ESR 150 μ F aluminum electrolytic or tantalum between V_{OUT} and GND is strongly recommended to reduce the voltage drop during hot-attachment of downstream peripheral. (Per USB 2.0, output ports must have a minimum 120 μ F of low-ESR bulk capacitance per hub). Higher-value output capacitor is better when the output load is heavy. Additionally, bypassing the output with a 0.1 μ F ceramic capacitor improves the immunity of the device to short-circuit transients.

Layout Consideration

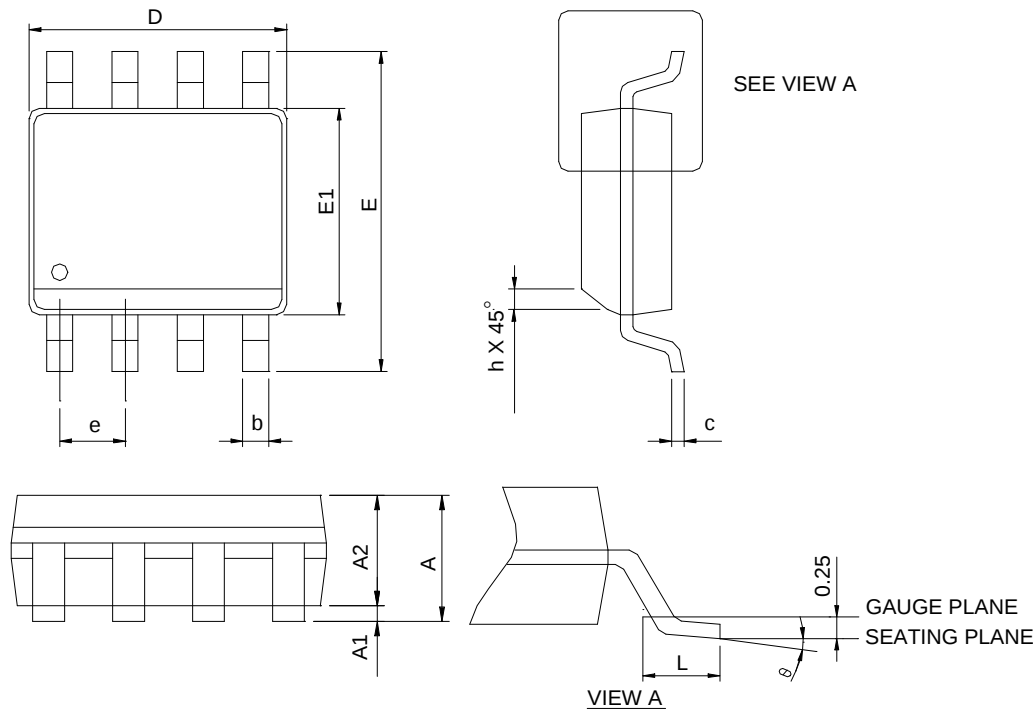
The PCB layout should be carefully performed to maximize thermal dissipation and to minimize voltage drop, droop and EMI. The following guidelines must be considered:

1. Please place the input capacitors near the VIN pin as close as possible.
2. Output decoupling capacitors for load must be placed near the load as close as possible for decoupling high-frequency ripples.
3. Locate APL3518/9 and output capacitors near the load to reduce parasitic resistance and inductance for excellent load transient performance.
4. The negative pins of the input and output capacitors and the GND pin must be connected to the ground plane of the load.
5. Keep V_{IN} and V_{OUT} traces as wide and short as possible.

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Package Information

SOP-8



SYMBOL	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.10	0.25	0.004	0.010
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

Note: 1. Follow JEDEC MS-012 AA.

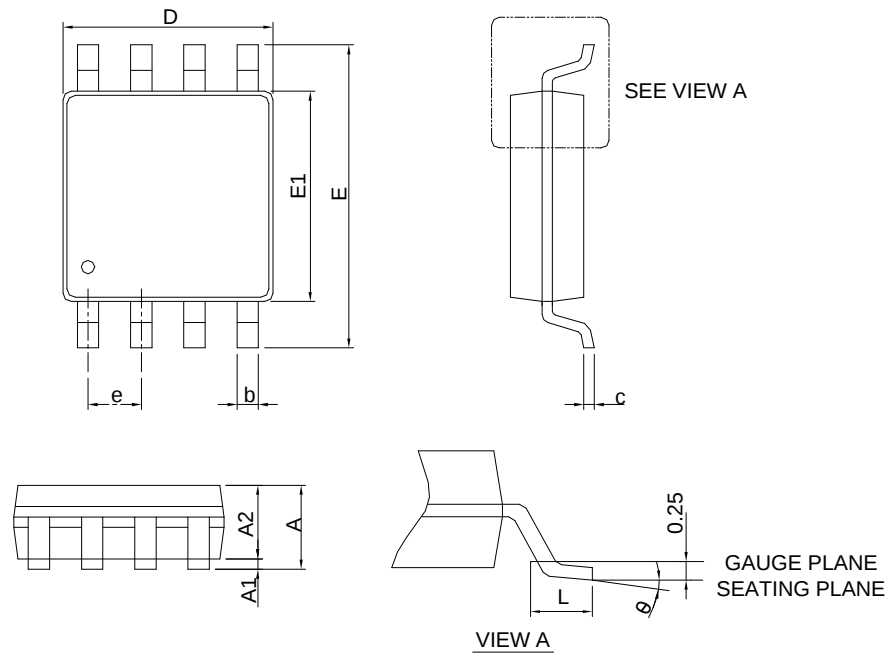
2. Dimension "D" does not include mold flash, protrusions or gate burrs.
Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.

3. Dimension "E" does not include inter-lead flash or protrusions.
Inter-lead flash and protrusions shall not exceed 10 mil per side.

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Package Information

MSOP-8



SYMBOL	MSOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.10		0.043
A1	0.00	0.15	0.000	0.006
A2	0.75	0.95	0.030	0.037
b	0.22	0.38	0.009	0.015
c	0.08	0.23	0.003	0.009
D	2.90	3.10	0.114	0.122
E	4.70	5.10	0.185	0.201
E1	2.90	3.10	0.114	0.122
e	0.65 BSC		0.026 BSC	
L	0.40	0.80	0.016	0.031
θ	0°	8°	0°	8°

Note: 1. Follow JEDEC MO-187 AA.

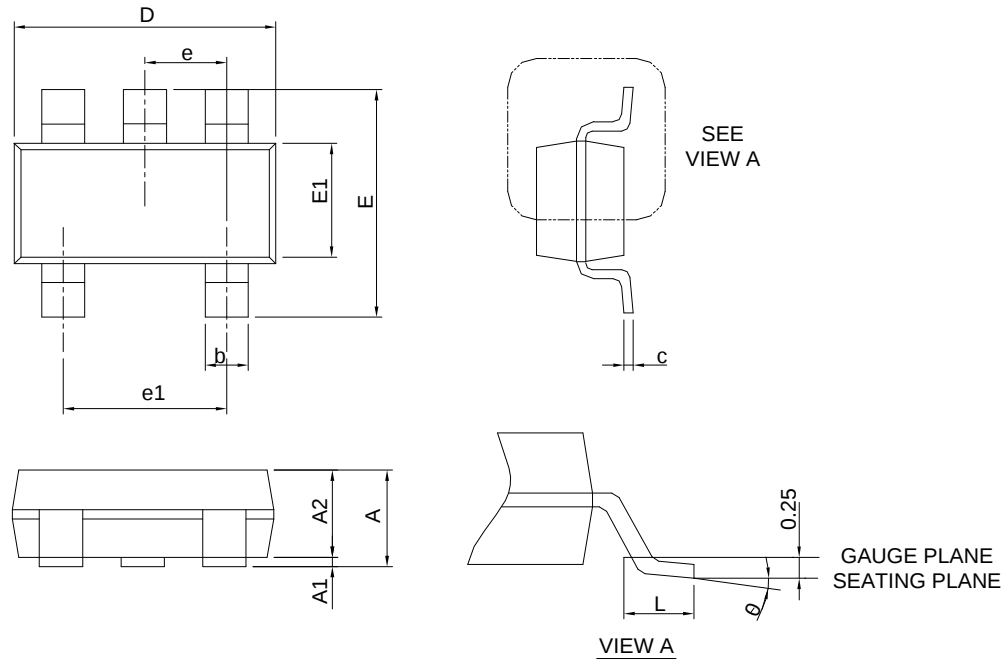
2. Dimension " D " does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.

3. Dimension " E1 " does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 5 mil per side.

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Package Information

SOT-23-5



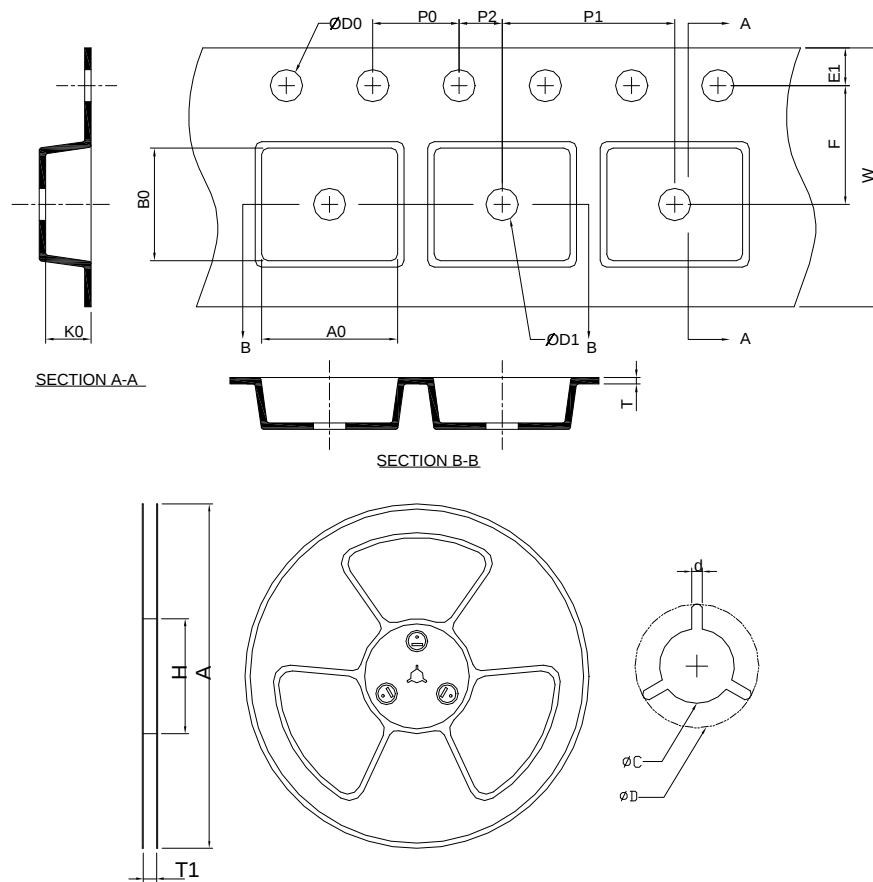
SYMBOL	SOT-23-5			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.45		0.057
A1	0.00	0.15	0.000	0.006
A2	0.90	1.30	0.035	0.051
b	0.30	0.50	0.012	0.020
c	0.08	0.22	0.003	0.009
D	2.70	3.10	0.106	0.122
E	2.60	3.00	0.102	0.118
E1	1.40	1.80	0.055	0.071
e	0.95 BSC		0.037 BSC	
e1	1.90 BSC		0.075 BSC	
L	0.30	0.60	0.012	0.024
θ	0°	8°	0°	8°

Note : 1. Follow JEDEC TO-178 AA.

2. Dimension D and E1 do not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 10 mil per side.

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Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
SOP-8	330.0 ±0.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0 ±0.30	1.75 ±0.10	5.5 ±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0 ±0.10	8.0 ±0.10	2.0 ±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40 ±0.20	5.20 ±0.20	2.10 ±0.20
Application	A	H	T1	C	d	D	W	E1	F
MSOP-8	330.0 ±0.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0 ±0.30	1.75 ±0.10	5.5 ±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.00 ±0.10	8.00 ±0.10	2.00 ±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	5.30 ±0.20	3.30 ±0.20	1.40 ±0.20
Application	A	H	T1	C	d	D	W	E1	F
SOT-23-5	178.0 ±0.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0 ±0.30	1.75 ±0.10	3.5 ±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0 ±0.10	4.0 ±0.10	2.0 ±0.05	1.5+0.10 -0.00	1.0 MIN.	0.6+0.00 -0.40	3.20 ±0.20	3.10 ±0.20	1.50 ±0.20

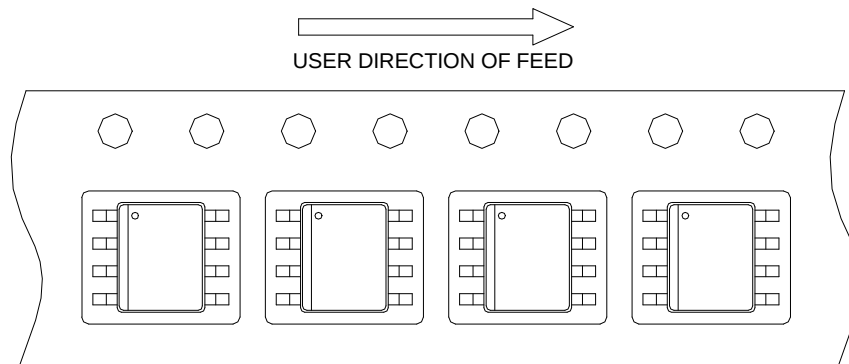
(mm)

Devices Per Unit

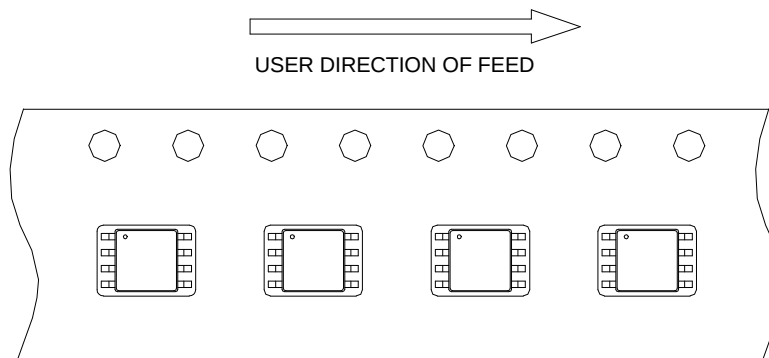
Package Type	Unit	Quantity
SOP-8	Tape & Reel	2500
MSOP-8	Tape & Reel	3000
SOT-23-5	Tape & Reel	3000

Taping Direction Information

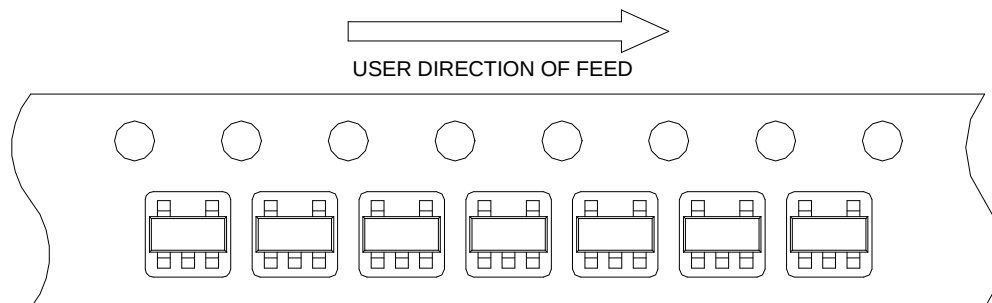
SOP-8



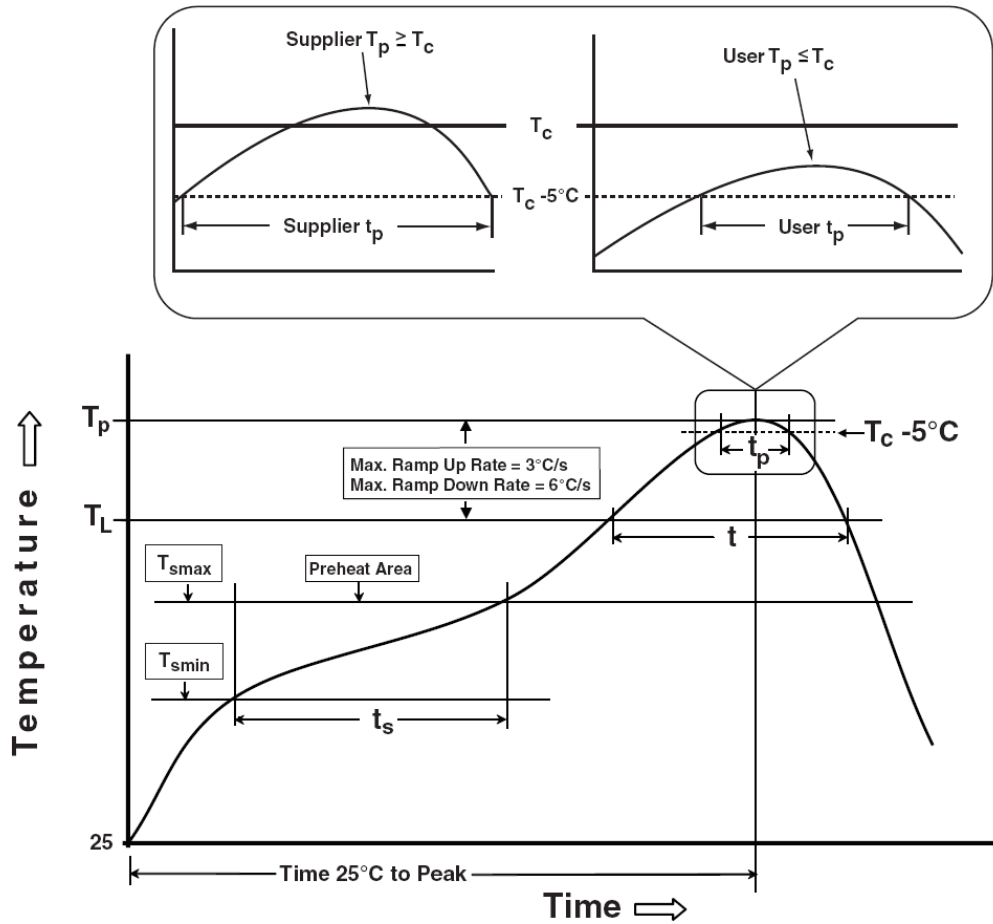
MSOP-8



SOT-23-5



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak		
Temperature min (T_{smin})	100 °C	150 °C
Temperature max (T_{smax})	150 °C	200 °C
Time (T_{smin} to T_{smax}) (t_s)	60-120 seconds	60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L)	183 °C	217 °C
Time at liquidous (t_L)	60-150 seconds	60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_p)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum.		
** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Classification Reflow Profiles (Cont.)

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm ³ <350	Volume mm ³ 350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm ³ <350	Volume mm ³ 350-2000	Volume mm ³ >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ Tj=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM 2KV
MM	JESD-22, A115	VMM 200V
Latch-Up	JESD 78	10ms, 1 _{tr} 100mA

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