SGM41511

I²C Controlled 3A Single-Cell Battery Charger for High Input Voltage and Narrow Voltage DC (NVDC) Power Path Management

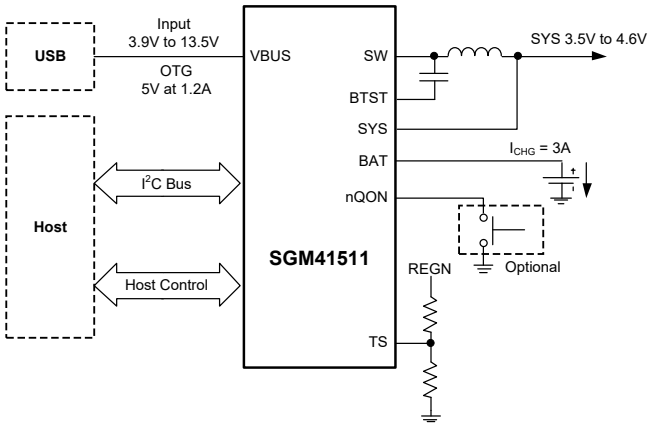
FEATURES

- High Efficiency, 1.6MHz, Synchronous Switch-Mode Buck Charger
  - 93% Charge Efficiency at 1A from 5V Input
  - 91% Charge Efficiency at 2A from 5V Input
  - Optimized for USB Voltage Input (5V)
  - Selectable Low Power Pulse Frequency Modulation (PFM) Mode for Light Load Operations
- Supports USB On-The-Go (OTG)
  - Boost Converter with up to 1.2A Output
  - 93.5% Boost Efficiency at 0.5A Output
  - 92.2% Boost Efficiency at 1A Output
  - Accurate Hiccup Mode Over-Current Protection
  - Soft-Start up to 500μF Capacitive Load
  - Output Short Circuit Protection
  - Selectable Low Power PFM Mode for Light Load Operations
- Single Input to Support USB Input and High Voltage Adapters
  - Support 3.9V to 13.5V Input Voltage Range with 20V Absolute Maximum Input Voltage Rating
  - Programmable Input Current Limit (100mA to 3.2A with 100mA Resolution) to Support USB 2.0, USB 3.0 Standards and High Voltage Adaptors (IINDPM)
  - Maximum Power Tracking by Input Voltage Limit up to 5.4V (VINDPM)
  - VINDPM Threshold Automatically Tracks Battery Voltage
- High Battery Discharge Efficiency with 28mΩ Battery Discharge MOSFET
- NVDC Power Path Management
  - Instant-On Works with No Battery or Deeply Discharged Battery
  - Ideal Diode Operation in Battery Supplement Mode
- BATFET Control to Support Ship Mode, Wake-Up and Full System Reset
- Flexible Autonomous and I²C Mode for Optimal System Performance
- High Integration Includes All MOSFETs, Current Sensing and Loop Compensation
- 9μA Low Battery Leakage Current to Support Ship Mode
- High Accuracy
  - ±0.5% Charge Voltage Regulation
  - ±5% at 1.5A Charge Current Regulation
  - ±10% at 0.9A Input Current Regulation
- Safety
  - Battery Temperature Sensing for Charge and Boost Mode
  - Thermal Regulation and Thermal Shutdown
  - Input Under-Voltage Lockout (UVLO) and Over-Voltage (ACOV) Protections

APPLICATIONS

Smart Phones, EPOS
Portable Internet Devices and Accessory

SIMPLIFIED SCHEMATIC



GENERAL DESCRIPTION

The SGM41511 is a highly-integrated 3A switch-mode battery charge management and system power path management device for single cell Li-Ion and Li-polymer battery. It features fast charging with high input voltage support for a wide range of smart phones, tablets and portable devices. Its low impedance power path optimizes switch-mode operation efficiency, reduces battery charging time and extends battery life during discharging phase. Its input voltage and current regulation deliver maximum charging power to battery. The solution is highly integrated with input reverse blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and battery FET (BATFET, Q4) between system and battery. It also integrates the bootstrap diode for the high-side gate drive for simplified system design. The I^2C serial interface with charging and system settings makes the device a truly flexible solution.

The device supports a wide range of input sources, including standard USB host port, USB charging port, and USB compliant high voltage adapter. The device sets default input current limit based on the built-in USB interface. To set the default input current limit, the device takes the result from detection circuit in the system, such as USB PHY device. The device is compliant with USB 2.0 and USB 3.0 power spec with input current and voltage regulation. The device also meets USB On-the-Go (OTG) operation power rating specification by supplying 5.15V on VBUS with current limit up to 1.2A.

The power path management regulates the system slightly above battery voltage but does not drop below 3.5V minimum system voltage (programmable). With this feature, the system maintains operation even when the battery is completely depleted or removed. When the input current limit or voltage limit is reached, the power path management automatically reduces the charge current to zero. As the system load continues to increase, the power path discharges the battery until the system power requirement is met. This supplement mode prevents overloading the input source.

The device initiates and completes a charging cycle without software control. It senses the battery voltage and charges the battery in three phases: pre-conditioning, constant current and constant voltage. At the end of the charging cycle, the charger automatically terminates when the charge current is below a preset limit and the battery voltage is higher than recharge threshold. If the fully charged battery falls below the recharge threshold, the charger automatically starts another charging cycle.

The charger provides various safety features for battery charging and system operations, including battery negative temperature coefficient thermistor monitoring, charging safety timer and over-voltage and over-current protections. The thermal regulation reduces charge current when the junction temperature exceeds 110℃ (programmable). The STAT output reports the charging status and any fault conditions. Other safety features include battery temperature sensing for charge and boost mode, thermal regulation and thermal shutdown and input UVLO and over-voltage protection. The VBUS_GD bit indicates if a good power source is present. The nINT output immediately notifies host when fault occurs.

The device also provides nQON pin for BATFET enable and reset control to exit low power ship mode or full system reset function.

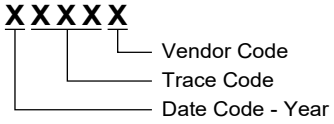
The device is available in a Green TQFN-4×4-24L package.

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM41511	TQFN-4×4-24L	-40℃ to +85℃	SGM41511YTQF24G/TR	SGM41511 YTQF24 XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltage Range (with Respect to PGND)
- VAC, VBUS (Converter not Switching) ..... -2V to 20V
- BTST, PMID (Converter not Switching) ..... -0.3V to 20V
- SW ..... -2V to 16V
- BTST to SW ..... -0.3V to 6V
- PSEL ..... -0.3V to 6V
- REGN, TS, nCE, nPG, BAT, SYS (Converter not Switching) ..... -0.3V to 6V
- SDA, SCL, nINT, nQON, STAT ..... -0.3V to 6V

Output Sink Current
- STAT ..... 6mA (MAX)
- nINT ..... 6mA (MAX)

Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range, V_{VBUS} ..... 3.9V to 13.5V
Input Current (VBUS), I_{IN} ..... 3.25A (MAX)
Output Current (SW), I_{SWOP} ..... 3.25A (MAX)
Battery Voltage, V_{BATOP} ..... 4.624V (MAX)
Fast Charging Current, I_{BATOP} ..... 3A (MAX)
Discharging Current (Continuous), I_{BATOP} ..... 6A (MAX)
Operating Temperature Range ..... -40℃ to +85℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

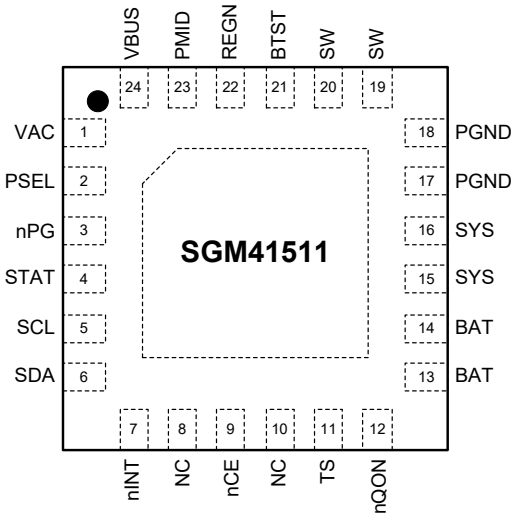
This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TQFN-4×4-24L

PIN DESCRIPTION

PIN	NAME	TYPE (1)	FUNCTION
1	VAC	AI	Charge Input Voltage Sense. This pin must be connected to VBUS pin.
2	PSEL	DI	Power Source Selection Input. Set 500mA input current limit by pulling this pin high and set 2.4A input current limit by pulling this pin low. Once the device gets into host mode, the host can program different input current limits to IINDPM[4:0] register.
3	nPG	DO	Open-Drain Active Low Power Good Indicator. Connect to the pull-up rail through 10kΩ resistor. Low indicates a good input source if the input voltage is between UVLO and ACOV, above sleep mode threshold.
4	STAT	DO	Open-Drain Charge Status Output. Connect STAT pin to a logic rail via 10kΩ resistor. The STAT pin indicates charger status. Connect a current limit resister and an LED from a rail to this pin. Charge in progress: low. Charge complete or charger in sleep mode: high. Charge suspend (fault response): 1Hz, 50% duty cycle pulses. This pin can be disabled via EN_ICHG_MON[1:0] register.
5	SCL	DI	I²C Interface Clock. Connect SCL pin to a logic rail through a 10kΩ resistor.
6	SDA	DIO	I²C Interface Data. Connect SDA pin to a logic rail through a 10kΩ resistor.
7	nINT	DO	Open-Drain Interrupt Output. Connect nINT pin to a logic rail through 10kΩ resistor. The nINT pin sends an active low, 256μs pulse to host to report charger device status and fault.
8, 10	NC	—	No Connect. Keep the pins float.
9	nCE	DI	Charge Enable Pin. When this pin is driven low, battery charging is enabled.
11	TS	AI	Temperature Qualification Voltage Input to Support JEITA Profile. Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from REGN pin to TS pin to PGND. Charge suspends when TS pin is out of range. When TS pin is not used, connect a 10kΩ resistor from REGN pin to TS pin and connect a 10kΩ resistor from TS pin to PGND. It is recommended to use a 103AT-2 thermistor.
12	nQON	DI	BATFET Enable/Reset Control Input. When BATFET is in ship mode, a logic low of $t_{SHIPMODE}$ (1.1s TYP) duration turns on BATFET to exit ship mode. When VBUS is not plugged-in, a logic low of t_{QON_RST} (10s TYP) duration resets SYS (system power) by turning BATFET off for t_{BATFET_RST} (325ms TYP) and then re-enables BATFET to provide full system power reset. The pin contains an internal pull-up to maintain default high logic.
13, 14	BAT	P	Battery Connection Point to Positive Terminal of Battery Pack. The internal BATFET and current sensing are connected between SYS pin and BAT pin. Connect a 10μF capacitor close to the BAT pin.
15, 16	SYS	P	Converter Output Connection Point. The internal current sensing network is connected between SYS pin and BAT pin. Connect a 20μF capacitor close to SYS pin.
17, 18	PGND	—	Ground Pin.
19, 20	SW	P	Switching Node Output. Connected to output inductor. Connect a 0.047μF bootstrap capacitor from SW pin to BTST pin.
21	BTST	P	PWM High-side Driver Positive Supply. Internally, the BTST pin is connected to the cathode of the boost-strap diode. Connect a 0.047μF bootstrap capacitor from SW pin to BTST pin.
22	REGN	P	LSFET Driver and Internal Supply Output. Internally, the REGN pin is connected to the anode of the boost-strap diode. Connect a 4.7μF (10V rating) ceramic capacitor from REGN pin to PGND. The capacitor should be placed close to the IC.
23	PMID	DO	PMID Pin. Connected to the drain of the reverse blocking MOSFET (RBFET) and the drain of HSFET. Connect a 10μF ceramic capacitor from PMID pin to PGND.
24	VBUS	P	Charger Input. The internal N-channel reverse blocking MOSFET (RBFET) is connected between VBUS and PMID pins. Place a 1μF ceramic capacitor from VBUS to PGND close to the device.
Exposed Pad	—	P	Thermal Pad and Ground Reference. This pad is ground reference for the device and it is also the thermal pad used to conduct heat from the device. This pad should be tied externally to a ground plane through PCB vias under the pad.

NOTE:
1. AI = Analog Input, AO = Analog Output, AIO = Analog Input Output, DI = Digital Input, DO = Digital Output, DIO = Digital Input Output, P = Power.

ELECTRICAL CHARACTERISTICS

(V_{VAC_UVLOZ} < V_{VAC} < V_{VAC_OV} and V_{VAC} > V_{BAT} + V_{SLEEP}, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
QUIESCENT CURRENTS						
Battery Discharge Current (BAT, SW, SYS) in Buck Mode	I_{BAT}	V_{BAT} = 4.5V, V_{VBUS} < V_{VAC_UVLOZ}, leakage between BAT and VBUS		1	TBD	μA
Battery Discharge Current (BAT) in Buck Mode		V_{BAT} = 4.5V, HIZ mode and BATFET_DIS = 1 or no VBUS, I²C disabled, BATFET disabled		10	TBD	μA
Battery Discharge Current (BAT, SW, SYS)		V_{BAT} = 4.5V, HIZ mode and BATFET_DIS = 1 or no VBUS, I²C disabled, BATFET enabled		20	TBD	μA
Input Supply Current (VBUS) in Buck Mode	I_{VBUS_HIZ}	V_{VBUS} = 3.9V, HIZ mode and BATFET_DIS = 1, no battery		20	TBD	μA
		V_{VBUS} = 5V, HIZ mode and BATFET_DIS = 1, no battery		24	TBD	μA
		V_{VBUS} = 12V, HIZ mode and BATFET_DIS = 1, no battery		50	TBD	μA
	I_{VBUS}	V_{VBUS} = 12V, V_{VBUS} > V_{BAT}, converter not switching		1.3	TBD	mA
		V_{BAT} = 3.8V, I_{SYS} = 0A, V_{VBUS} > V_{BAT}, V_{VBUS} > V_{VAC_UVLOZ}, converter switching		4		mA
Battery Discharge Current in Boost Mode	I_{BOOST}	V_{BAT} = 4.2V, I_{VBUS} = 0A, converter switching		3		mA
BAT PIN, VAC PIN AND VBUS PIN POWER-UP						
VBUS Operating Range	V_{VBUS_OP}	V_{VBUS} rising	3.9		13.5	V
VBUS for Active I²C, No Battery Sense VAC Pin Voltage	V_{VAC_UVLOZ}	V_{VAC} rising		3.25	TBD	V
I²C Active Hysteresis	$V_{VAC\_UVLOZ\_HYS}$	V_{VAC} falling from above V_{VAC_UVLOZ}		60		mV
One of the Conditions to Turn On REGN	$V_{VAC\_PRESENT}$	V_{VAC} rising		3.25	TBD	V
One of the Conditions to Turn On REGN Hysteresis	$V_{VAC\_PRESENT\_HYS}$	V_{VAC} falling		60		mV
Sleep Mode Falling Threshold	V_{SLEEP}	(V_{VAC} - V_{BAT}), $V_{VBUSMIN\_FALL}$ ≤ V_{BAT} ≤ V_{REG}, V_{VAC} falling	TBD	70	TBD	mV
Sleep Mode Rising Threshold	V_{SLEEPZ}	(V_{VAC} - V_{BAT}), $V_{VBUSMIN\_FALL}$ ≤ V_{BAT} ≤ V_{REG}, V_{VAC} rising	TBD	200	TBD	mV
VAC 6.5V Over-Voltage Rising Threshold	$V_{VAC\_OV\_RISE}$	V_{VAC} rising, OVP[1:0] = 01	TBD	6.5	TBD	V
VAC 10.5V Over-Voltage Rising Threshold		V_{VAC} rising, OVP[1:0] = 10	TBD	10.5	TBD	
VAC 14V Over-Voltage Rising Threshold		V_{VAC} rising, OVP[1:0] = 11	TBD	14	TBD	
VAC 6.5V Over-Voltage Hysteresis	$V_{VAC\_OV\_HYS}$	V_{VAC} falling, OVP[1:0] = 01		500		mV
VAC 10.5V Over-Voltage Hysteresis		V_{VAC} falling, OVP[1:0] = 10		500		
VAC 14V Over-Voltage Hysteresis		V_{VAC} falling, OVP[1:0] = 11		500		
BAT for Active I²C, No Adapter	V_{BAT_UVLOZ}	V_{BAT} rising	TBD	2.45		V
BAT Depletion Threshold	$V_{BAT\_DPL\_FALL}$	V_{BAT} falling	TBD	2.25	TBD	V
	$V_{BAT\_DPL\_RISE}$	V_{BAT} rising	TBD	2.5	TBD	
BAT Depletion Rising Hysteresis	$V_{BAT\_DPL\_HYS}$	V_{BAT} rising		250		mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{VAC_UVLOZ} < V_{VAC} < V_{VAC_OV} and V_{VAC} > V_{BAT} + V_{SLEEP}, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Bad Adapter Detection Falling Threshold	$V_{VBUSMIN\_FALL}$	V_{VBUS} falling	TBD	3.5	TBD	V
Bad Adapter Detection Hysteresis	$V_{VBUSMIN\_HYS}$			250		mV
Bad Adapter Detection Current Source	I_{BAD_SRC}	Sink current from VBUS to PGND		30		mA
POWER-PATH						
System Regulation Voltage	V_{SYS_MIN}	V_{BAT} < SYS_MIN[2:0] = 101 (3.5V), BATFET_DIS = 1	TBD	3.65		V
	V_{SYS}	I_{SYS} = 0A, V_{BAT} = 4.4V, V_{BAT} > V_{SYS_MIN}, BATFET_DIS = 1		V_{BAT} + 50mV		V
Maximum DC System Voltage Output	V_{SYS_MAX}	I_{SYS} = 0A, V_{BAT} ≤ 4.4V, V_{BAT} > V_{SYS_MIN} = 3.5V, BATFET_DIS = 1	TBD	4.45	TBD	V
Top Reverse Blocking MOSFET On-Resistance between VBUS and PMID - Q1	R_{ON_RBFET}			65		mΩ
Top Switching MOSFET On-Resistance between PMID and SW - Q2	R_{ON_HSFET}	V_{REGN} = 5V		70		mΩ
Bottom Switching MOSFET On-Resistance between SW and PGND - Q3	R_{ON_LSFET}	V_{REGN} = 5V		55		mΩ
BATFET forward Voltage in Supplement Mode	V_{FWD}			30		mV
BAT-SYS MOSFET On-Resistance	$R_{ON(BAT-SYS)}$	V_{BAT} = 4.2V, measured from BAT pin to SYS pin		28	TBD	mΩ
BATTERY CHARGER						
Charge Voltage Program Range	$V_{BAT\_REG\_RANGE}$		3.856		4.624	V
Charge Voltage Step	$V_{BAT\_REG\_STEP}$			32		mV
Charge Voltage Setting	V_{BAT_REG}	VREG[4:0] = 01011 (4.208V)	TBD	4.208	TBD	V
		VREG[4:0] = 01111 (4.352V)	TBD	4.352	TBD	V
Charge Voltage Setting Accuracy	$V_{BAT\_REG\_ACC}$	V_{BAT_REG} = 4.208V or V_{BAT_REG} = 4.352V	TBD	0.5%	TBD	
Charge Current Regulation Range	$I_{CHG\_REG\_RANGE}$		0		3000	mA
Charge Current Regulation Step	$I_{CHG\_REG\_STEP}$			60		mA
Charge Current Regulation Setting	I_{CHG_REG}	I_{CHG} = 240mA, V_{BAT} = 3.1V or V_{BAT} = 3.8V	TBD	0.24	TBD	A
Charge Current Regulation Accuracy	$I_{CHG\_REG\_ACC}$		TBD	20%	TBD	
Charge Current Regulation Setting	I_{CHG_REG}	I_{CHG} = 720mA, V_{BAT} = 3.1V or V_{BAT} = 3.8V	TBD	0.720	TBD	A
Charge Current Regulation Accuracy	$I_{CHG\_REG\_ACC}$		TBD	10%	TBD	
Charge Current Regulation Setting	I_{CHG_REG}	I_{CHG} = 1.38A, V_{BAT} = 3.1V or V_{BAT} = 3.8V	TBD	1.380	TBD	A
Charge Current Regulation Accuracy	$I_{CHG\_REG\_ACC}$		TBD	5%	TBD	
Pre-Charge Current Regulation Setting	I_{PRECHG}	IPRECHG[3:0] = 0010 (180mA)	TBD	180	TBD	mA
Pre-Charge Current Regulation Accuracy	I_{PRECHG_ACC}		TBD	20%	TBD	
Battery LOWV Falling Threshold	$V_{BATLOWV\_FALL}$	I_{CHG} = 240mA	TBD	2.96	TBD	V
Battery LOWV Rising Threshold	$V_{BATLOWV\_RISE}$	Pre-charge to fast charging	TBD	3.16	TBD	V

ELECTRICAL CHARACTERISTICS (continued)

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Termination Current Regulation Setting	I_{TERM}	I_{CHG} > 780mA, V_{BAT_REG} = 4.208V, ITERM[3:0] = 0010 (180mA)	TBD	180	TBD	mA
Termination Current Regulation Accuracy	I_{TERM_ACC}		TBD	20%	TBD	
Termination Current Regulation Setting	I_{TERM}	I_{CHG} = 600mA, V_{BAT_REG} = 4.208V, ITERM[3:0] = 0000 (60mA)	TBD	60	TBD	mA
Termination Current Regulation Accuracy	I_{TERM_ACC}		TBD	25%	TBD	
Battery Short Voltage	V_{SHORT}	V_{BAT} falling	TBD	2.05	TBD	V
	V_{SHORTZ}	V_{BAT} rising	TBD	2.2	TBD	
Battery Short Current	I_{SHORT}	V_{BAT} < V_{SHORTZ}	TBD	90	TBD	mA
Recharge Threshold below V_{BAT_REG}	V_{RECHG}	V_{BAT} falling, VRECHG = 0 (100mV)	TBD	100	TBD	mV
		V_{BAT} falling, VRECHG = 1 (200mV)	TBD	200	TBD	
System Discharge Load Current	$I_{SYSLOAD}$	V_{SYS} = 4.2V		23		mA
INPUT VOLTAGE AND CURRENT REGULATION						
Input Voltage Regulation Limit	V_{INDPM}	VINDPM[3:0] = 0000 (3.9V)	TBD	3.85	TBD	V
Input Voltage Regulation Accuracy	V_{INDPM_ACC}		TBD	3%	TBD	
Input Voltage Regulation Limit	V_{INDPM}	VINDPM[3:0] = 0110 (4.4V)	TBD	4.35	TBD	V
Input Voltage Regulation Accuracy	V_{INDPM_ACC}		TBD	3%	TBD	
Input Voltage Regulation Limit Tracking VBAT	V_{DPM_VBAT}	V_{BAT} = 4.0V, V_{INDPM} = 3.9V, VDPM_BAT_TRACK[1:0] = 11 (300mV)	TBD	4.3	TBD	V
Input Voltage Regulation Accuracy Tracking VBAT	$V_{DPM\_VBAT\_ACC}$		TBD	3%	TBD	
USB Input Current Regulation Limit	I_{INDPM}	V_{VBUS} = 5V, current pulled from SW, IINDPM[4:0] = 00100 (500mA)	TBD	500	TBD	mA
		V_{VBUS} = 5V, current pulled from SW, IINDPM[4:0] = 01000 (900mA)	TBD	900	TBD	
		V_{VBUS} = 5V, current pulled from SW, IINDPM[4:0] = 01110 (1.5A)	TBD	1500	TBD	
Input Current Limit during System Start-Up Sequence	I_{IN_START}			200		mA
BAT PIN OVER-VOLTAGE PROTECTION						
Battery Over-Voltage Threshold	V_{BATOVP_RISE}	V_{BAT} rising, as percentage of V_{BAT_REG}	TBD	104	TBD	%
Battery Over-Voltage Threshold	V_{BATOVP_FALL}	V_{BAT} falling, as percentage of V_{BAT_REG}	TBD	102	TBD	%
THERMAL REGULATION AND THERMAL SHUTDOWN						
Junction Temperature Regulation Threshold	$T_{JUNCTION\_REG}$	Temperature increasing, TREG = 1 (110℃)		110		℃
Junction Temperature Regulation Threshold	$T_{JUNCTION\_REG}$	Temperature increasing, TREG = 0 (90℃)		90		℃
Thermal Shutdown Rising Temperature	T_{SHUT}	Temperature increasing		160		℃
Thermal Shutdown Hysteresis	T_{SHUT_HYS}			30		℃

ELECTRICAL CHARACTERISTICS (continued)

(V_{VAC_UVLOZ} < V_{VAC} < V_{VAC_OV} and V_{VAC} > V_{BAT} + V_{SLEEP}, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
JEITA THERMISTOR COMPARATOR (BUCK MODE)						
T1 (0℃) Threshold (Charge suspended T1 below this temperature)	V_{T1}	Charger suspends charge, as percentage of V_{REGN}	TBD	73.5%	TBD	
Falling	V_{T1}	As percentage of V_{REGN}	TBD	71.6%	TBD	
T2 (10℃) Threshold (Charge back to I_{CHG}/2 and 4.2V below this temperature)	V_{T2}	As percentage of V_{REGN}	TBD	68.2%	TBD	
Falling	V_{T2}	As percentage of V_{REGN}	TBD	66.9%	TBD	
T3 (45℃) Threshold (Charge back to I_{CHG} and 4.05V above this temperature)	V_{T3}	Charger suspends charge, as percentage of V_{REGN}	TBD	44.5%	TBD	
Falling	V_{T3}	As percentage of V_{REGN}	TBD	45.8%	TBD	
T5 (60℃) Threshold (Charge suspended above this temperature)	V_{T5}	As percentage of V_{REGN}	TBD	34.1%	TBD	
Falling	V_{T5}	As percentage of V_{REGN}	TBD	35.4%	TBD	
COLD OR HOT THERMISTER COMPARATOR (BOOST MODE)						
Cold Temperature Threshold (TS pin voltage rising threshold)	V_{BCOLD}	As percentage of V_{REGN} (Approx. -20℃ w/ 103AT)	TBD	80%	TBD	
Falling	V_{BCOLD}	As percentage of V_{REGN} (Approx. -20℃ w/ 103AT)	TBD	79%	TBD	
Hot Temperature Threshold (TS pin voltage falling threshold)	V_{BHOT}	As percentage of V_{REGN} (Approx. 60℃ w/ 103AT)	TBD	31.2%	TBD	
Rising	V_{BHOT}	As percentage of V_{REGN} (Approx. 60℃ w/ 103AT)	TBD	34.3%	TBD	
CHARGE OVER-CURRENT COMPARATOR (CYCLE-BY-CYCLE)						
HSFET Cycle-by-Cycle Over-Current Threshold	I_{HSFET_OCP}		TBD	5.4	TBD	A
System Overload Threshold	I_{BATFET_OCP}		TBD	6.8		A
CHARGE UNDER-CURRENT COMPARATOR (CYCLE-BY-CYCLE)						
LSFET Under-Current Falling Threshold	I_{LSFET_UCP}	From sync mode to non-sync mode		160		mA
PWM						
PWM Switching Frequency	f_{SW}	Oscillator frequency, buck mode	TBD	1600	TBD	kHz
		Oscillator frequency, boost mode	TBD	1600	TBD	
Maximum PWM Duty Cycle (1)	D_{MAX}			98%		
BOOST MODE OPERATION						
Boost Mode Regulation Voltage	V_{OTG_REG}	V_{BAT} = 3.8V, I_{PMID} = 0A, BOOSTV[1:0] = 10 (5.15V)	TBD	5.15	TBD	V
Boost Mode Regulation Voltage Accuracy	$V_{OTG\_REG\_ACC}$	V_{BAT} = 3.8V, I_{PMID} = 0A, BOOSTV[1:0] = 10 (5.15V)	TBD	3%	TBD	
Battery Voltage Exiting Boost Mode	$V_{BATLOWV\_OTG}$	V_{BAT} falling, MIN_BAT_SEL = 0	TBD	2.96	TBD	V
		V_{BAT} rising, MIN_BAT_SEL = 0	TBD	3.16	TBD	V
		V_{BAT} falling, MIN_BAT_SEL = 1	TBD	2.6	TBD	V
		V_{BAT} rising, MIN_BAT_SEL = 1	TBD	2.8	TBD	V
OTG Mode Output Current	I_{OTG}	BOOST_LIM = 1 (1.2A)	TBD	1.4	TBD	A
Boost Mode RBFET Over-Current Protection Accuracy	$I_{OTG\_OCP\_ACC}$	BOOST_LIM = 0 (0.5A)	TBD	0.6	TBD	A
OTG Over-Voltage Threshold	V_{OTG_OVP}	Rising threshold	TBD	6	TBD	V
HSFET Under-Current Falling Threshold	I_{OTG_HSZCP}			100		mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{VAC_UVLOZ} < V_{VAC} < V_{VAC_OV} and V_{VAC} > V_{BAT} + V_{SLEEP}, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REGN LDO						
REGN LDO Output Voltage	V_{REGN}	V_{VBUS} = 9V, I_{REGN} = 40mA	TBD	5	TBD	V
		V_{VBUS} = 5V, I_{REGN} = 20mA	TBD	4.65	TBD	
LOGIC I/O PIN CHARACTERISTICS (nCE, PSEL, SCL, SDA, nINT)						
Input Low Threshold	V_{IL}			0.4	TBD	V
Input High Threshold	V_{IH}		TBD	1		V
High-Level Leakage Current	I_{BIAS}	Pull up rail 1.8V		0.1	TBD	μA
LOGIC I/O PIN CHARACTERISTICS (nPG, STAT)						
Low-Level Output Voltage	V_{OL}			0.2	TBD	V

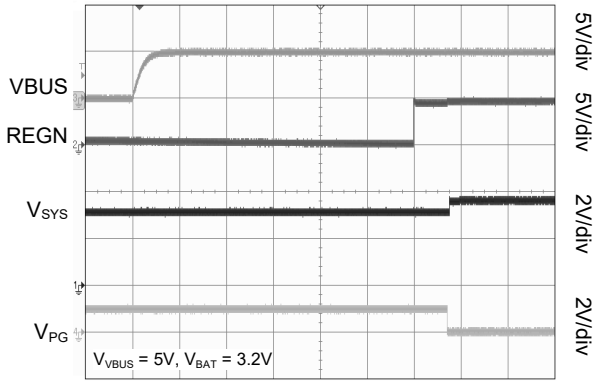
NOTE: 1. Specified by design. Not production tested.

TIMING REQUIREMENTS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{VBUS}/V_{BAT} POWER-UP						
VBUS OVP Reaction Time	t_{ACOV}	V_{VBUS} rising above ACOV threshold to turn off Q2		0.1		μs
Bad Adapter Detection Duration	t_{BADSRC}			30		ms
BATTERY CHARGER						
Deglitch Time for Charge Termination	t_{TERM_DGL}			250		ms
Deglitch Time for Recharge	t_{RECHG_DGL}			250		ms
System Over-Current Deglitch Time to Turn Off Q4	$t_{SYSOVLD\_DGL}$			100		μs
Battery Over-Voltage Deglitch Time to Disable Charge	t_{BATOVP}			1		μs
Typical Charge Safety Timer Range	t_{SAFETY}	CHG_TIMER = 1		10		hr
Typical Top-Off Timer Range	t_{TOP_OFF}	TOP_OFF_TIMER[1:0] = 10 (30min)		30		min
nQON TIMING						
nQON Low Time to Turn On BATFET and to Exit Ship Mode	$t_{SHIPMODE}$			1.1		s
nQON Low Time to Reset BATFET	t_{QON_RST}			10		s
BATFET Off Time during Full System Reset	t_{BATFET_RST}			325		ms
Enter Ship Mode Delay	t_{SM_DLY}			12.5		s
DIGITAL CLOCK AND WATCHDOG TIMER						
WATCHDOG[1:0] = 01	t_{WDT}	REGN LDO disabled		40		s
Digital Low Power Clock	f_{LPDIG}	REGN LDO disabled		30		kHz
Digital Clock	f_{DIG}	REGN LDO enabled		500		kHz
SCL Clock Frequency	f_{SCL}			400		kHz

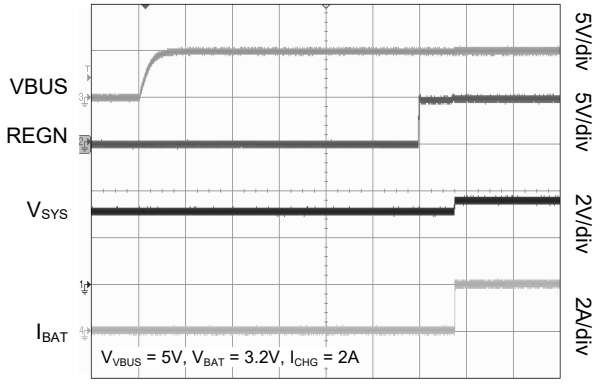
TYPICAL PERFORMANCE CHARACTERISTICS

Power-Up with Charge Disable



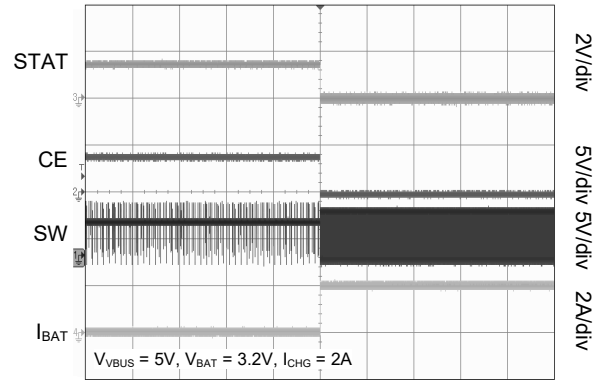
Time (40ms/div)

Power-Up with Charge Enable



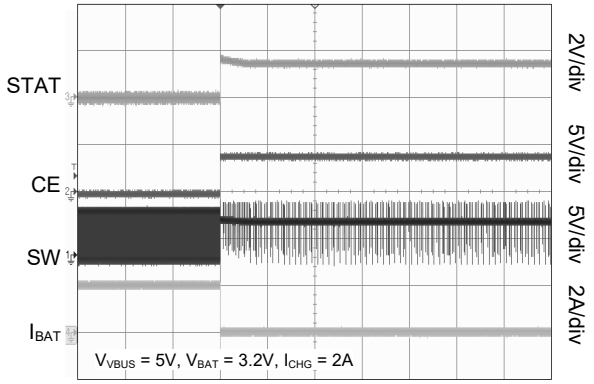
Time (40ms/div)

Charge Enable



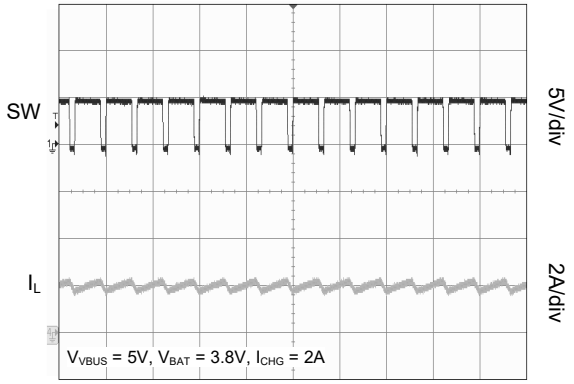
Time (10ms/div)

Charge Disable



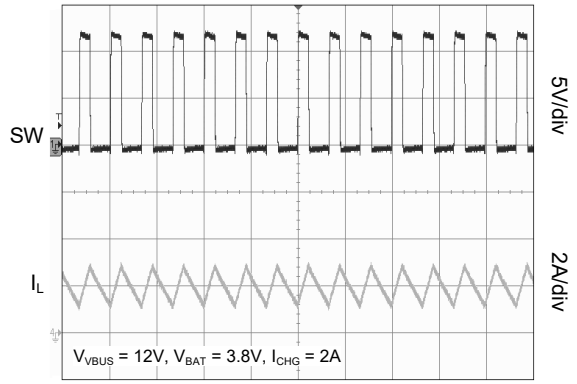
Time (10ms/div)

PWM Switching in Buck Mode



Time (1μs/div)

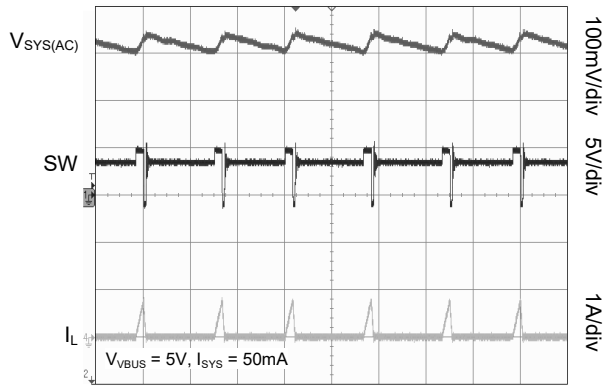
PWM Switching in Buck Mode



Time (1μs/div)

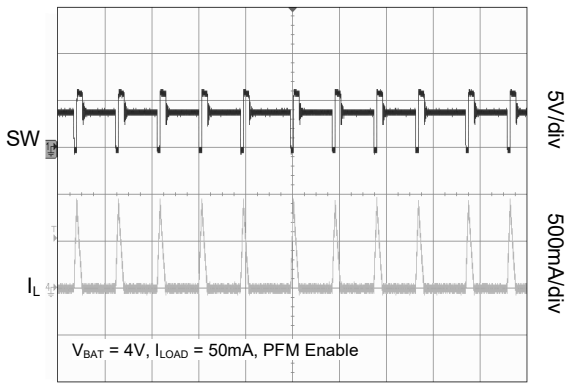
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

PFM Switching in Buck Mode, Charge Disable



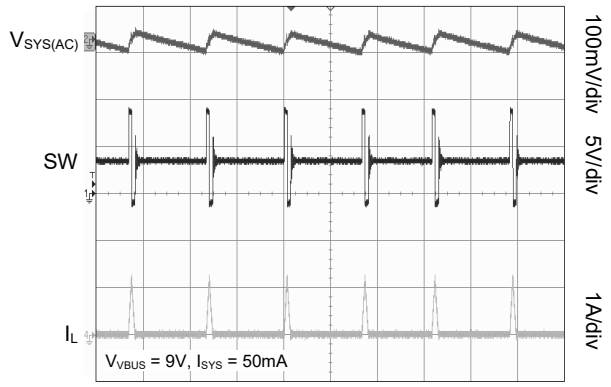
Time (4μs/div)

OTG Switching



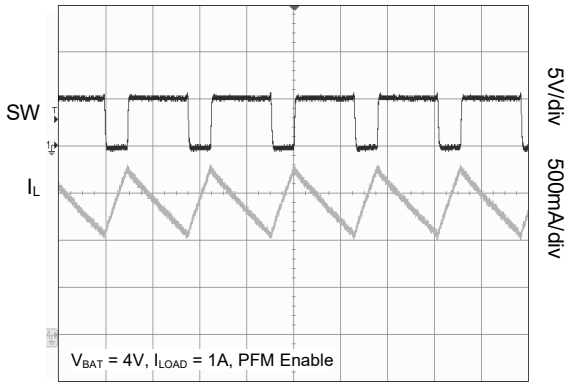
Time (4μs/div)

PFM Switching in Buck Mode, Charge Disable



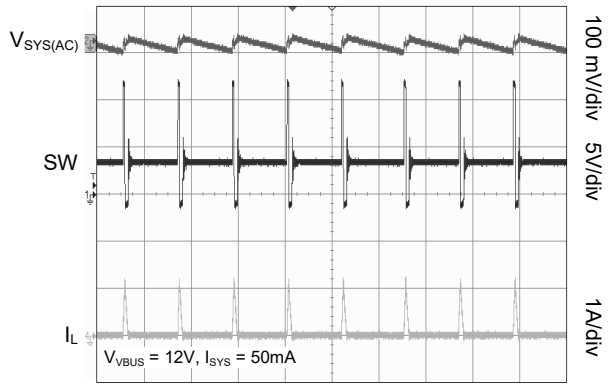
Time (4μs/div)

OTG Switching



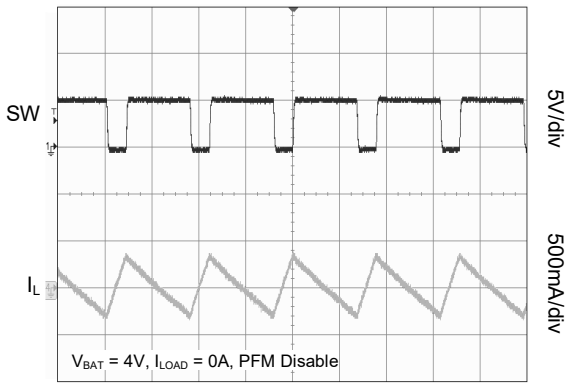
Time (400ns/div)

PFM Switching in Buck Mode, Charge Disable



Time (4μs/div)

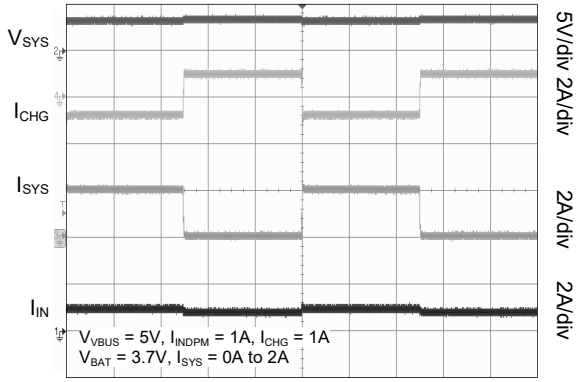
OTG Switching



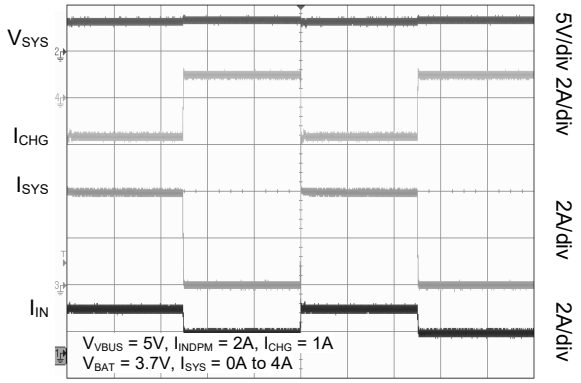
Time (400ns/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

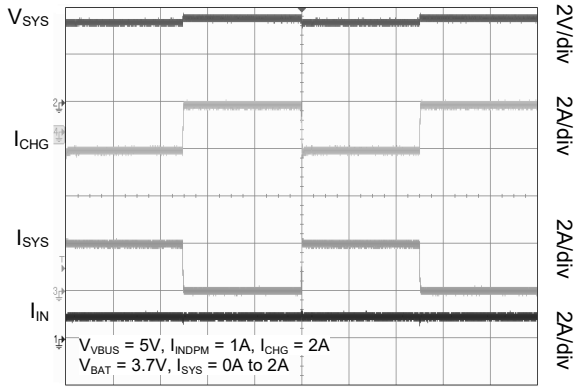
System Load Transient



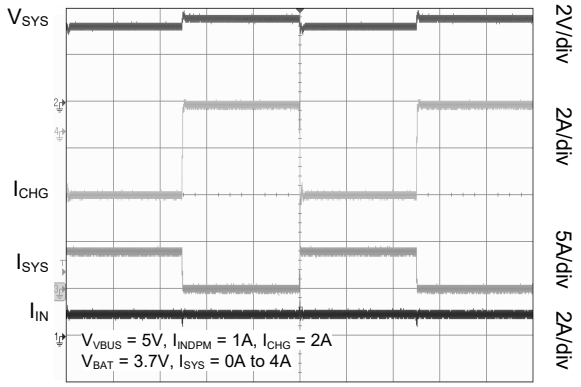
System Load Transient



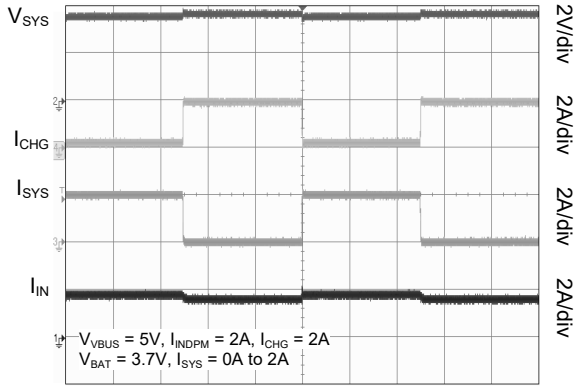
System Load Transient



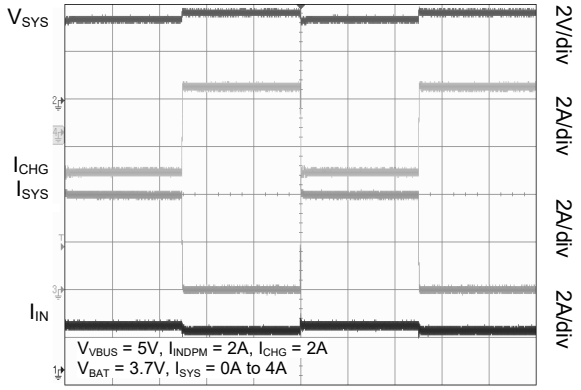
System Load Transient



System Load Transient

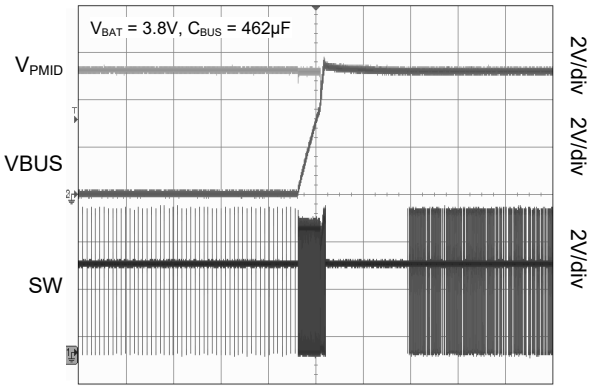


System Load Transient

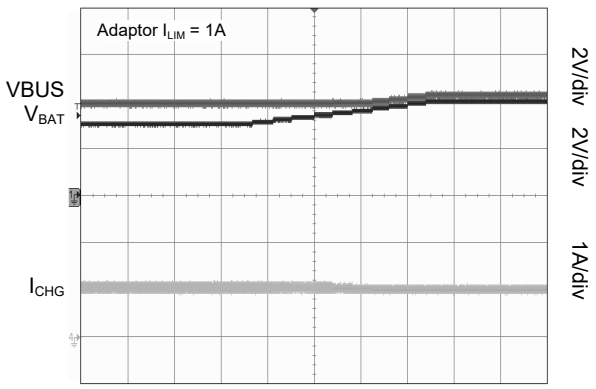


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

OTG Start-Up



VINDPM Tracking Battery Voltage



TYPICAL APPLICATION

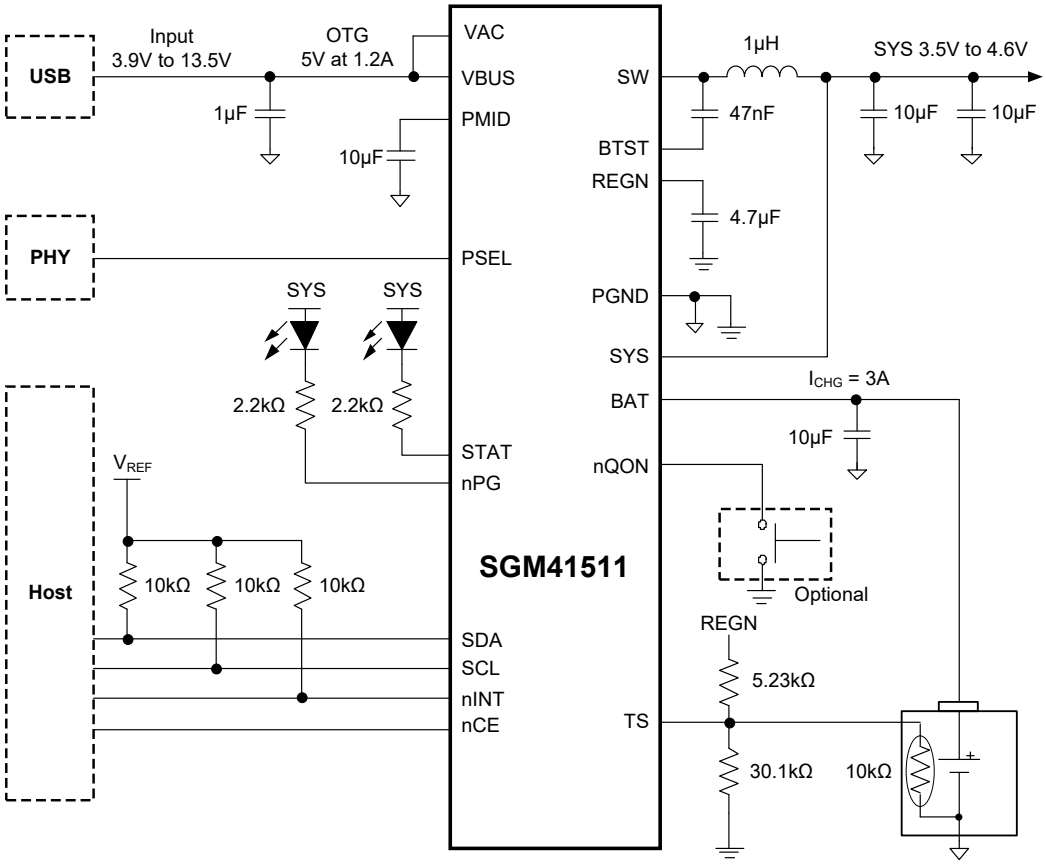


Figure 1. Typical Application Circuit

FUNCTIONAL BLOCK DIAGRAM

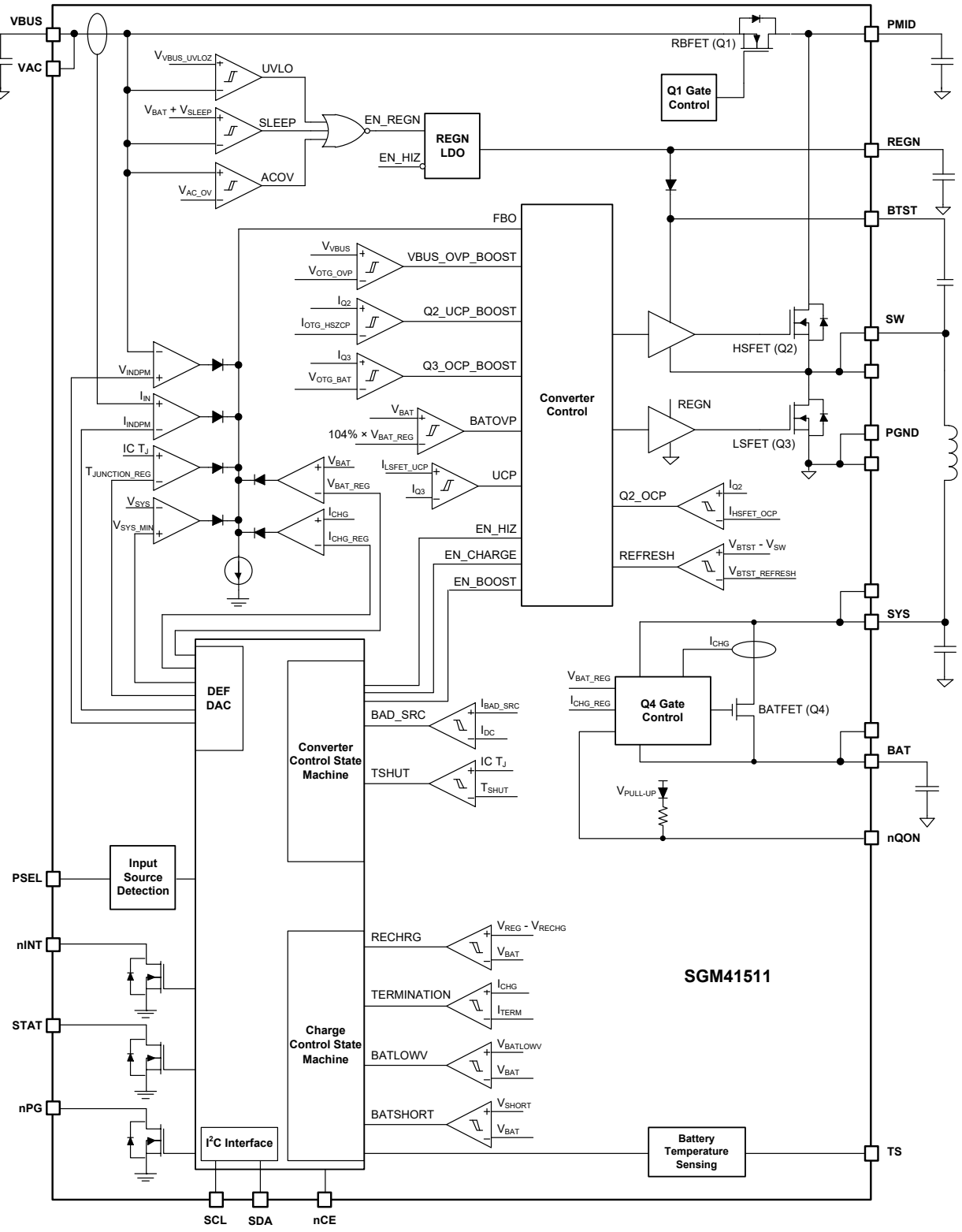


Figure 2. Block Diagram

DETAILED DESCRIPTION

Power-On-Reset (POR)

The device powers internal bias circuits from the higher voltage of V_{VBUS} and V_{BAT}. When V_{VBUS} rises above V_{VBUS_UVLOZ} or V_{BAT} rises above V_{BAT_UVLOZ}, the sleep comparator, battery depletion comparator and BATFET driver are active. I^2C interface is ready for communication and all the registers are reset to default value. The host can access all the registers after POR.

Device Power-Up from Battery without Input Source

If only battery is present and the voltage is above depletion threshold ($V_{BAT\_DPL\_RISE}$), the BATFET turns on and connects battery to system. The REGN stays off to minimize the quiescent current. The low R_{DSON} of BATFET and the low quiescent current on BAT minimize the conduction loss and maximize the battery run time.

The device always monitors the discharge current through BATFET (**Supplement Mode**). When the system is overloaded or shorted ($I_{BAT} > I_{BATFET\_OCP}$), the device turns off BATFET immediately and sets BATFET_DIS bit to indicate BATFET is disabled until the input source plugs in again or one of the methods described in **BATFET Enable Mode (Exit Ship Mode)** is applied to re-enable BATFET.

Power-Up from Input Source

When an input source is plugged in, the device checks the input source voltage to turn on REGN LDO and all the bias circuits. It detects and sets the input current limit before the buck converter is started. The power-up sequence from input source is as listed:

1. Power-up REGN LDO.
2. Poor source qualification.
3. Input Source Type Detection based on PSEL to set default input current limit (IINDPM[4:0]) register or input source type.
4. Input voltage limit threshold setting. (VINDPM threshold)
5. Converter power-up.

Power-Up REGN LDO

The REGN LDO supplies internal bias circuits as well as the HSFET and LSFET gate drive. The REGN LDO also provides bias rail to TS external resistors. The pull-up rail of STAT can be connected to REGN as well. The REGN is enabled when all the below conditions are valid:

1. V_{VAC} voltage above $V_{VAC\_PRESENT}$ voltage.
2. V_{VAC} voltage above V_{BAT} + V_{SLEEPZ} in buck mode or V_{VBUS} voltage below V_{BAT} + V_{SLEEP} in boost mode.
3. After 220ms delay is completed.

If any one of the above conditions is not valid, the device is in high impedance mode (HIZ) with REGN LDO off. The device draws less than I_{VBUS_HIZ} from VBUS during HIZ state. The battery powers up the system when the device is in HIZ.

Poor Source Qualification

After REGN LDO powers up, the device confirms the current capability of the input source. The input source must meet both of the following requirements in order to start the buck converter.

1. V_{VBUS} voltage below V_{VAC_OV} voltage.
2. V_{VBUS} voltage above V_{VBUS_MIN} voltage when pulling I_{BAD_SRC} (typical 30mA).

Once the input source passes all the conditions above, the status register VBUS_GD bit is set high and the nINT pin is pulsed to signal to the host. If the device fails the poor source detection, it repeats poor source qualification every 2 seconds.

DETAILED DESCRIPTION (continued)

Input Source Type Detection

After the VBUS_GD bit is set and REGN LDO is powered, the device runs input source detection through the PSEL pin. The SGM41511 sets input current limit through PSEL pin.

After input source type detection is completed, an INT pulse is asserted to the host. In addition, the following registers and pin are changed:

1. Input current limit (IINDPM[4:0]) register is changed to set current limit.
2. PG_STAT bit is set.
3. VBUS_STAT[2:0] register is updated to indicate USB or other input source.

The host can over-write IINDPM[4:0] register to change the input current limit if needed. The charger input current is always limited by the IINDPM[4:0] register.

PSEL Pin Sets Input Current Limit

The SGM41511 has PSEL pin for input current limit setting to interface with USB PHY. It directly takes the USB PHY device output to decide whether the input is USB host or charging port. When the device operates in host-control mode, the host needs to enable IINDET_EN bit to read the PSEL value and update the IINDPM[4:0] register. When the device is in default mode, PSEL value updates IINDPM[4:0] in real time.

Table 1. Input Current Limit Setting from PSEL

INPUT DETECTION	PSEL Pin	INPUT CURRENT LIMIT (I_{LIM})	VBUS_STAT[2:0]
USB SDP	High	500mA	001
Adapter	Low	2400mA	011

Input Voltage Limit Threshold Setting (VINDPM Threshold)

The device supports wide range of input voltage limit (3.9V to 5.4V) for USB. The default VINDPM[3:0] setting is 4.5V.

The device supports dynamic VINDPM[3:0] tracking settings which tracks the battery voltage. This function can be enabled via the VDPM_BAT_TRACK[1:0] register bits. When enabled, the actual input voltage limit will be the higher of the VINDPM[3:0] register and V_{BAT} + VDPM_BAT_TRACK[1:0] offset.

Converter Power-Up

After the input current limit is set, the converter is enabled and the HSFET and LSFET start switching. If battery charging is disabled, BATFET turns off. Otherwise, BATFET stays on to charge the battery.

The device provides soft-start when system rail is ramped up. When the system rail is below 2.2V, the input current is limited to the lower of 200mA or IINDPM[4:0] register setting. After the system rises above 2.2V, the device limits input current to the value set by IINDPM[4:0] register.

As a battery charger, the device deploys a highly efficient 1.6MHz step-down switching regulator. The fixed frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current and temperature, simplifying output filter design.

The device switches to PFM control at light load when battery is below minimum system voltage setting or charging is disabled. The PFM_DIS bit can be used to prevent PFM operation in either buck or boost configuration.

DETAILED DESCRIPTION (continued)

Boost Mode Operation from Battery

The device supports boost converter operation to deliver power from the battery to other portable devices through USB port. The boost mode output current rating meets the USB On-The-Go 500mA output requirement.

The maximum output current is up to 1.2A. The boost operation can be enabled if the conditions are valid:

1. V_{BAT} voltage above V_{OTG_BAT} voltage.
2. V_{VBUS} voltage less than V_{BAT} + V_{SLEEP} (in sleep mode).
3. Boost mode operation is enabled (OTG_CONFIG bit = 1).
4. Voltage at TS (thermistor) pin is within acceptable range (V_{BHOT} < V_{TS} < V_{BCOLD}).
5. After 30ms delay from boost mode enable.

In boost mode, the device employs 1.6MHz step-up switching regulator.

During boost mode, the status register VBUS_STAT[2:0] bits is set to 111, the V_{VBUS} output is 5.15V and the output current can reach up to 1.2A, selected through I²C (BOOST_LIM bit). The boost output is maintained when V_{BAT} is above V_{OTG_BAT} threshold.

When OTG is enabled, the device starts up with PFM and later transits to PWM to minimize the overshoot. The PFM_DIS bit can be used to prevent PFM operation in either buck or boost configuration.

Host Mode and Default Mode

The SGM41511 is a host controlled charger, but it can operate in default mode without host management. In default mode, the device can be used as an autonomous charger with no host or while host is in sleep mode. When the charger is in default mode, WATCHDOG_FAULT bit is high. When the charger is in host mode, WATCHDOG_FAULT bit is low.

After power-on-reset, the device starts in default mode with watchdog timer expired, or default mode. All the registers are in the default settings. During default mode, any change on PSEL pin will make real time IINDPM[4:0] register changes.

In default mode, the device keeps charging the battery with default 10 hours fast charging safety timer. At the end of the 10 hours, the charging is stopped and the buck converter continues to operate to supply system load.

Writing a 1 to the WD_RST bit transitions the charger from default mode to host mode. All the device parameters can be programmed by the host. To keep the device in host mode, the host has to reset the watchdog timer by writing 1 to WD_RST bit before the watchdog timer expires (WATCHDOG_FAULT bit is set), or disable watchdog timer by setting WATCHDOG[1:0] = 00.

When the watchdog timer expires (WATCHDOG_FAULT bit = 1), the device returns to default mode and all registers are reset to default values except IINDPM[4:0], VINDPM[3:0], BATFET_RST_EN, BATFET_DLY and BATFET_DIS bits.

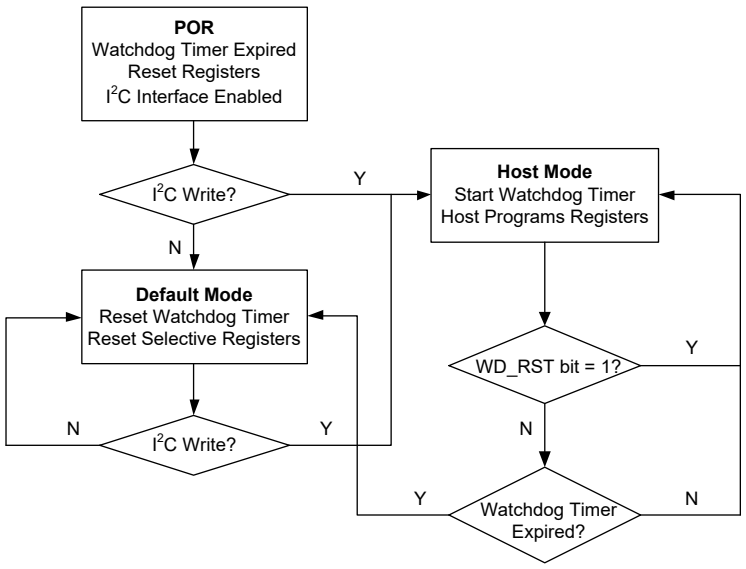


Figure 3. Watchdog Timer Flow Chart

DETAILED DESCRIPTION (continued)

Power Path Management

The device accommodates a wide range of input sources from USB, wall adapter, to car charger. The device provides automatic power path selection to supply the system (SYS) from input source (VBUS), battery (BAT), or both.

Battery Charging Management

The device charges single-cell Li-Ion battery with up to 3A charge current for high capacity tablet battery. The 28mΩ BATFET improves charging efficiency and minimize the voltage drop during discharging.

Autonomous Charging Cycle

With battery charging is enabled (CHG_CONFIG bit = 1 and nCE pin is low), the device autonomously completes a charging cycle without host involvement. The device default charging parameters are listed in Table 2. The host can always control the charging operations and optimize the charging parameters by writing to the corresponding registers through I²C.

Table 2. Charging Parameter Default Setting

Default Mode	SGM41511
Charging Voltage	4.208V
Charging Current	2.04A
Pre-Charge Current	180mA
Termination Current	180mA
Temperature Profile	JEITA
Safety Timer	10 hours

A new charge cycle starts when the following conditions are valid:

- Converter starts.
- Battery charging is enabled. (CHG_CONFIG bit = 1, ICHG[5:0] register is not 0mA and nCE pin is low.)
- No thermistor fault on TS pin.
- No safety timer fault.
- BATFET is not forced to turn off. (BATFET_DIS bit = 0)

The charger device automatically terminates the charging cycle when the charging current is below termination threshold, battery voltage is above recharge threshold, and device not is in DPM mode or thermal regulation. When a fully charged battery is discharged below recharge threshold (selectable through VRECHG bit), the device automatically starts a new charging cycle. After the charge is done, toggling nCE pin or CHG_CONFIG bit can initiate a new charging cycle.

The STAT output indicates the charging status: charging (low), charging complete or charge disable (high) or charging fault (blinking). The STAT output can be disabled by setting EN_ICHG_MON[1:0] = 11. In addition, the CHRG_STAT[1:0] status register indicates the different charging phases: 00: charging disable, 01: pre-charge, 10: fast charging (constant current mode) and constant voltage mode, 11: charging done. Once a charging cycle is completed, an INT pulse is asserted to notify the host.

Battery Charging Profile

The device charges the battery in five phases: battery short, preconditioning, constant current, constant voltage and top-off trickle charging (optional). At the beginning of a charging cycle, the device checks the battery voltage and regulates current and voltage accordingly.

Table 3. Charging Current Setting

V_{BAT}	CHARGING CURRENT	REGISTER DEFAULT SETTING	CHRG_STAT[1:0]
< 2.2V	I_{SHORT}	60mA	01
2.2V to 3V	I_{PRECHG}	180mA	01
> 3V	I_{CHG}	2.048A	10

DETAILED DESCRIPTION (continued)

If the charger device is in DPM regulation or thermal regulation during charging, the actual charging current will be less than the programmed value. In this case, termination is temporarily disabled and the charging safety timer is counted at half the clock rate.

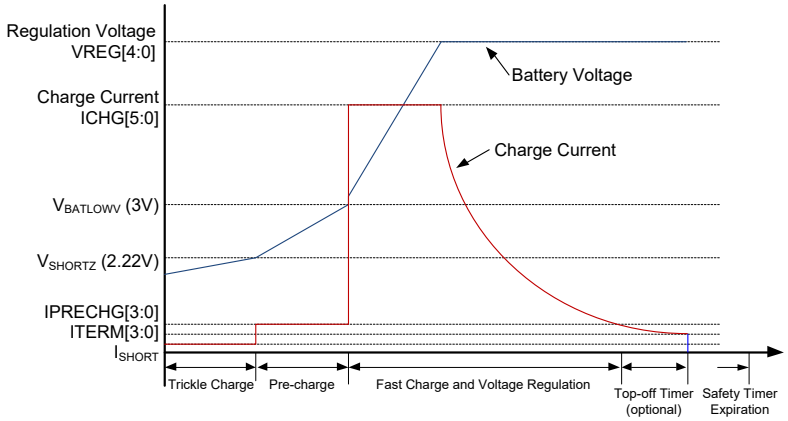


Figure 4. Battery Charging Profile

Charging Termination

The device terminates a charge cycle when the battery voltage is above recharge threshold, and the current is below termination current. After the charging cycle is completed, the BATFET turns off. The converter keeps running to power the system, and BATFET can turn on again to engage Supplement Mode.

When termination occurs, the CHRG_STAT[1:0] status register is set to 11, and an INT pulse is asserted to the host. Termination is temporarily disabled when the charger device is in input current, voltage or thermal regulation. Termination can be disabled by writing 0 to EN_TERM bit prior to charge termination.

At low termination current (25mA - 50mA), due to the comparator offset, the actual termination current may be 10mA - 20mA higher than the termination target. In order to compensate for comparator offset, a programmable top-off timer can be applied after termination is detected. The termination timer will follow safety timer constraints, such that if safety timer is suspended, so will the termination timer. Similarly, if safety timer is doubled, so will the termination timer. TOPOFF_ACTIVE bit reports whether the top-off timer is active or not. The host can read CHRG_STAT[1:0] and TOPOFF_ACTIVE bits to find out the termination status.

Top-off timer gets reset at one of the following conditions:

1. Charge disables to enable.
2. Termination status low to high.
3. Set REG_RST bit.

The top-off timer settings are read in once termination is detected by the charger. Programming a top-off timer value after termination will have no effect unless a recharge cycle is initiated. An INT pulse is asserted to the host when entering top-off timer segment as well as when top-off timer expires.

Thermistor Qualification

The charger device provides a single thermistor input for battery temperature monitor.

JEITA Guideline Compliance during Charging Mode

To improve the safety of charging Li-Ion batteries, JEITA guideline was released on April 20, 2007. The guideline emphasized the importance of avoiding a high charge current and high charge voltage at certain low and high temperature ranges.

To initiate a charge cycle, the voltage on TS pin must be within the V_{T1} to V_{T5} thresholds. If TS voltage exceeds the T1-T5 range, the controller suspends charging and waits until the battery temperature is within the T1 to T5 range.

At cool temperature (T1-T2), JEITA recommends the charge current to be reduced to half of the charge current or lower. At warm temperature (T3-T5), JEITA recommends charge voltage less than 4.1V.

DETAILED DESCRIPTION (continued)

The charger provides flexible voltage/current settings beyond the JEITA requirement. The voltage setting at warm temperature (T3-T5) can be VREG or 4.1V (configured by JEITA_VSET bit). The current setting at cool temperature (T1-T2) can be further reduced to 20% of fast charging current (configured by JEITA_ISET bit).

The resistor bias network has been updated as below.

$$R_{T2} = \frac{V_{REGN} \times R_{THCOLD} \times R_{THHOT} \times \left(\frac{1}{V_{T1}} - \frac{1}{V_{T5}} \right)}{R_{THHOT} \times \left(\frac{V_{REGN}}{V_{T5}} - 1 \right) - R_{THCOLD} \times \left(\frac{V_{REGN}}{V_{T1}} - 1 \right)} \quad (1)$$

$$R_{T1} = \frac{\left(\left(\frac{V_{REGN}}{V_{T1}} \right) - 1 \right)}{\left(\frac{1}{R_{T2}} \right) + \left(\frac{1}{R_{THCOLD}} \right)} \quad (2)$$

Select 0℃ to 60℃ range for Li-Ion or Li-polymer battery:

- $R_{THTCOLD}$ = 27.28kΩ
- R_{THTHOT} = 3.02kΩ
- R_{T1} = 5.23kΩ
- R_{T2} = 30.9kΩ

Boost Mode Thermistor Monitor during Battery Discharge Mode

For battery protection during boost mode, the device monitors the battery temperature to be within the V_{BCOLD} to V_{BHOT} thresholds. When temperature is outside of the temperature thresholds, the boost mode is suspended. In additional, VBUS_STAT[2:0] bits are set to 000 and NTC_FAULT[2:0] register is reported. Once temperature returns within thresholds, the boost mode is recovered and NTC_FAULT[2:0] register is cleared.

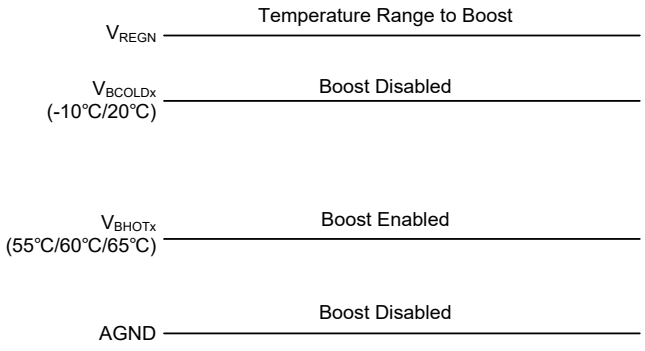


Figure 5. TS Pin Thermistor Sense Threshold in Boost Mode

DETAILED DESCRIPTION (continued)

Charging Safety Timer

The device has built-in safety timer to prevent extended charging cycle due to abnormal battery conditions. The safety timer is 2 hours when the battery is below $V_{BATLOWV}$ threshold and 10 hours when the battery is higher than $V_{BATLOWV}$ threshold.

The user can program fast charging safety timer through I^2C (CHG_TIMER bit). When safety timer expires, the fault register CHRG_FAULT[1:0] bits are set to 11 and an INT pulse is asserted to the host. The safety timer feature can be disabled through I^2C by setting EN_TIMER bit.

During input voltage, current, JEITA cool or thermal regulation, the safety timer counts at half clock rate as the actual charge current is likely to be below the register setting. For example, if the charger is in input current regulation (IINDPM_STAT bit = 1) throughout the whole charging cycle, and the safety timer is set to 5 hours, the safety timer will expire in 10 hours. This half clock rate feature can be disabled by writing 0 to TMR2X_EN bit.

During the fault, timer is suspended. Once the fault condition goes away, fault resumes. If user stops the current charging cycle, and starts again, timer gets reset (toggle nCE pin or CHG_CONFIG bit).

Narrow Voltage DC (NVDC) Architecture

The device deploys NVDC architecture with BATFET separating system from battery. The minimum system voltage is set by SYS_MIN[2:0] register. Even with a fully depleted battery, the system is regulated above the minimum system voltage (default 3.5V).

When the battery is below minimum system voltage setting, the BATFET operates in linear mode (LDO mode), and the system is typically 180mV above the minimum system voltage setting. As the battery voltage rises above the minimum system voltage, BATFET is fully on and the voltage difference between the system and battery is the VDS of BATFET.

When the battery charging is disabled and above minimum system voltage setting or charging is terminated, the system is always regulated at typically 50mV above battery voltage. The status register VSYS_STAT bit goes high when the system is in minimum system voltage regulation.

Figure 6. System Voltage vs. Battery Voltage

Dynamic Power Management (DPM)

To meet maximum current limit in USB spec and avoid over loading the adapter, the device features dynamic power management (DPM), which continuously monitors the input current and input voltage. When input source is overloaded, either the current exceeds the input current limit (I_{INDPM}) or the voltage falls below the input voltage limit (V_{INDPM}). The device then reduces the charge current until the input current falls below the input current limit and the input voltage rises above the input voltage limit.

When the charge current is reduced to zero, but the input source is still overloaded, the system voltage starts to drop. Once the system voltage falls below the battery voltage, the device automatically enters the supplement mode where the BATFET turns on and battery starts discharging so that the system is supported from both the input source and battery.

DETAILED DESCRIPTION (continued)

During DPM mode, the status register VINDPM_STAT bit (VINDPM) or IINDPM_STAT bit (IINDPM) goes high. Figure 7 shows the DPM response with 9V/1.2A adapter, 3.2V battery, 2.8A charge current and 3.4V minimum system voltage setting.

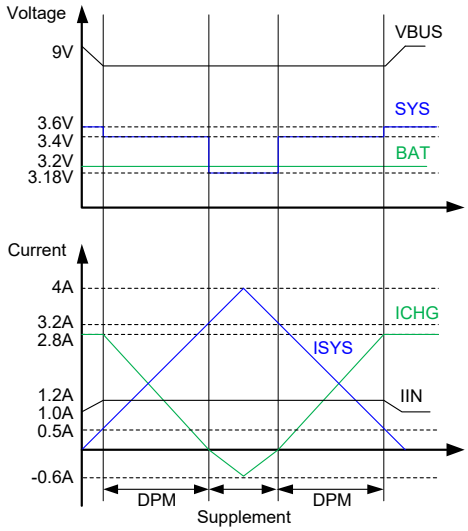


Figure 7. DPM Response

Supplement Mode

When the system voltage falls 180mV (V_{BAT} > V_{SYS_MIN}) or 45mV (V_{BAT} < V_{SYS_MIN}) below the battery voltage, the BATFET turns on and the BATFET gate is regulated the gate drive of BATFET so that the minimum BATFET VDS stays at 30mV when the current is low. This prevents oscillation from entering and exiting the supplement mode.

As the discharge current increases, the BATFET gate is regulated with a higher voltage to reduce R_{DSON} until the BATFET is in full conduction. At this point onwards, the BATFET VDS linearly increases with discharge current. Figure 8 shows the V-I curve of the BATFET gate regulation operation. BATFET turns off to exit supplement mode when the battery is below battery depletion threshold.

Figure 8. BATFET V-I Curve

Ship Mode and nQON Pin

BATFET Disable Mode (Ship Mode)

To extend battery life and minimize power when system is powered off during system idle, ship, or storage, the device can turn off BATFET so that the system voltage is zero to minimize the battery leakage current. When the host sets BATFET_DIS bit, the charger can turn off BATFET immediately or with a delay by t_{SM_DLY} as configured by BATFET_DLY bit.

DETAILED DESCRIPTION (continued)

BATFET Enable Mode (Exit Ship Mode)

When the BATFET is disabled (in ship mode) and indicated by setting BATFET_DIS bit, one of the following events can enable BATFET to restore system power:

1. Plug in adapter.
2. Clear BATFET_DIS bit.
3. Set REG_RST bit to reset all registers including BATFET_DIS bit to default 0.
4. A logic high to low transition on nQON pin with $t_{SHIPMODE}$ deglitch time to enable BATFET to exit ship mode.

BATFET Full System Reset

The BATFET functions as a load switch between battery and system when input source is not plugged in. By changing the state of BATFET from on to off, systems connected to SYS pin can be effectively forced to have a power-on-reset. The nQON pin supports push-button interface to reset system power without host by changing the state of BATFET.

When the nQON pin is driven to logic low for t_{QON_RST} while input source is not plugged in and BATFET is enabled (BATFET_DIS bit = 0), the BATFET is turned off for t_{BATFET_RST} and then it is re-enabled to reset system power. This function can be disabled by setting BATFET_RST_EN bit to 0.

nQON Pin Operations

The nQON pin incorporates two functions to control BATFET.

1. BATFET Enable: An nQON logic transition from high to low with longer than $t_{SHIPMODE}$ deglitch turns on BATFET to exit ship mode.

2. BATFET Reset: When nQON pin is driven to logic low by at least t_{QON_RST} while adapter is not plugged in (BATFET_DIS bit = 0), the BATFET is turned off for t_{BATFET_RST}. The BATFET is re-enabled after t_{BATFET_RST} duration. This function allows systems connected to SYS to have power-on-reset. This function can be disabled by setting BATFET_RST_EN bit to 0.

Figure 9 shows the sample external configurations for each.

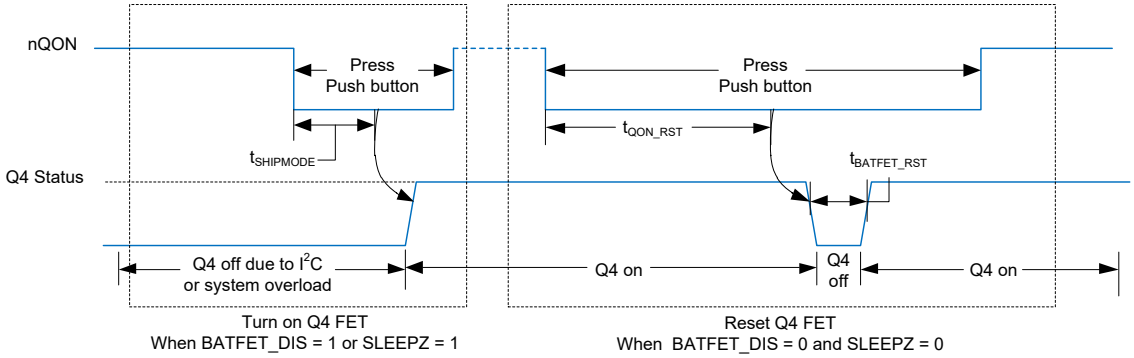


Figure 9. nQON Timing

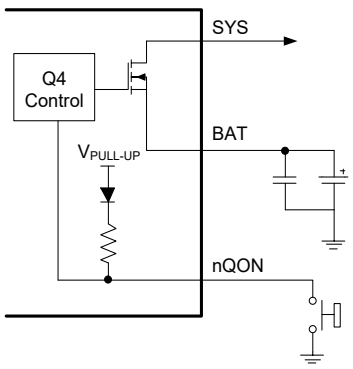


Figure 10. nQON Circuit

DETAILED DESCRIPTION (continued)

Status Outputs (nPG, STAT and nINT Pins)

Power Good Indicator (nPG Pin and PG_STAT Bit)

The PG_STAT bit goes high and nPG pin goes low to indicate a good input source when:

- V_{VBUS} voltage above V_{VBUS_UVLOZ} voltage.
- V_{VBUS} voltage above V_{BAT} (not in sleep mode).
- V_{VBUS} voltage below V_{VAC_OV} threshold.
- V_{VBUS} voltage above $V_{VBUSMIN}$ (typical 3.5V) when I_{BAD_SRC} (typical 30mA) current is applied (not a poor source).
- Completed **Input Source Type Detection**.

Charging Status Indicator (STAT Pin)

The device indicates charging state on the open-drain STAT pin. The STAT pin can drive LED. The STAT pin function can be disabled by setting the EN_ICHG_MON[1:0] bits = 11.

Table 4. STAT Pin State

CHARGING STATE	STAT INDICATOR
Charging in progress (including recharge)	Low
Charging complete	High
Sleep mode, charge disable	High
Charge suspend (input over-voltage, TS fault, timer fault or system over-voltage). Boost mode suspend (due to TS fault)	Blinking at 1Hz

Interrupt to Host (nINT Pin)

In some applications, the host does not always monitor the charger operation. The INT pulse notifies the system on the device operation. The following events will generate 256μs INT pulse.

- USB/adapter source identified (through PSEL detection).
- Good input source detected.
  V_{VBUS} voltage above battery (not in sleep mode).
  V_{VBUS} voltage below V_{VAC_OV} threshold.
  V_{VBUS} voltage above $V_{VBUSMIN}$ (typical 3.5V) when I_{BAD_SRC} (typical 30mA) current is applied (not a poor source).
- Input removed.
- Charge completed.
- Any fault event in REG09 register.
- VINDPM or IINDPM event detected (maskable).

When a fault occurs, the charger device sends out INT and keeps the fault state in REG09 until the host reads the fault register. Before the host reads REG09 and all the faults are cleared, the charger device would not send any INT upon new faults. To read the current fault status, the host has to read REG09 two times consecutively. The first read reports the pre-existing fault register status and the second read reports the current fault register status.

DETAILED DESCRIPTION (continued)

Protections

Voltage and Current Monitoring in Converter Operation

The device closely monitors the input and system voltage, as well as internal FET currents for safe buck and boost mode operation.

Voltage and Current Monitoring in Buck Mode

1. Input Over-Voltage (ACOV)

If VBUS voltage exceeds V_{VAC_OV} (programmable via OVP[1:0] bits), the device stops switching immediately.

During input over-voltage event (ACOV), the fault register CHRG_FAULT[1:0] bits are set to 01. An INT pulse is asserted to the host. The device will automatically resume normal operation once the input voltage drops back below the OVP threshold.

2. System Over-Voltage Protection (SYSOVP)

The charger device clamps the system voltage during load transient so that the components connect to system would not be damaged due to high voltage. SYSOVP threshold is 350mV above minimum system regulation voltage when the system is regulating at V_{SYSMIN}. Upon SYSOVP, converter stops switching immediately to clamp the overshoot. The charger provides 30mA discharge current to bring down the system voltage.

Voltage and Current Monitoring in Boost Mode

The device closely monitors the VBUS voltage, as well as RBFET and LSFET current to ensure safe boost mode operation.

VBUS Soft-Start

When the boost function is enabled, the device soft-starts boost mode to avoid inrush current.

VBUS Output Protection

The device monitors boost output voltage and other conditions to provide output short circuit and over-voltage protection. The boost mode builds in accurate constant current regulation to allow OTG to adapt to various types of load. If short circuit is detected on VBUS pin, the boost mode turns off and retries 7 times. If retries are not successful, OTG is disabled with OTG_CONFIG bit cleared. In addition, the BOOST_FAULT bit is set and an INT pulse is generated. The BOOST_FAULT bit can be cleared by host by re-enabling boost mode.

Boost Mode Over-Voltage Protection

When the VBUS voltage rises above regulation target and exceeds V_{OTG_OVP}, the device enters over-voltage protection which stops switching, clears OTG_CONFIG bit and exits boost mode. At boost mode over-voltage duration, the fault register BOOST_FAULT bit is set high to indicate fault in boost operation. An INT pulse is also asserted to the host.

Thermal Regulation and Thermal Shutdown

Thermal Protection in Buck Mode

The SGM41511 monitors the internal junction temperature T_J to avoid overheat the chip and limits the IC surface temperature at 110℃ in buck mode. When the internal junction temperature exceeds thermal regulation limit (110℃), the device lowers down the charge current. During thermal regulation, the actual charging current is usually below the programmed battery charging current. Therefore, termination is disabled, the safety timer runs at half the clock rate, and the status register THERM_STAT bit goes high.

Additionally, the device has thermal shutdown to turn off the converter and BATFET when IC surface temperature exceeds T_{SHUT} (160℃). The fault register CHRG_FAULT[1:0] is set to 10 and an INT pulse is asserted to the host. The BATFET and converter is enabled to recover when IC temperature is T_{SHUT_HYS} (30℃) below T_{SHUT} (160℃).

Thermal Protection in Boost Mode

The SGM41511 monitors the internal junction temperature T_J to provide thermal shutdown during boost mode. When IC junction temperature exceeds T_{SHUT} (160℃), the boost mode is disabled by setting OTG_CONFIG bit low and BATFET is turned off. When IC junction temperature is below T_{SHUT} (160℃) - T_{SHUT_HYS} (30℃), the BATFET is enabled automatically to allow system to restore and the host can re-enable OTG_CONFIG bit to recover.

DETAILED DESCRIPTION (continued)

Battery Protection

Battery Over-Voltage Protection (BATOVP)

The battery over-voltage limit is clamped at 4% above the battery regulation voltage. When battery over-voltage occurs, the charger device immediately disables charging. The fault register BAT_FAULT bit goes high and an INT pulse is asserted to the host.

Battery Over-Discharge Protection

When battery is discharged below $V_{BAT\_DPL\_FALL}$, the BATFET is turned off to protect battery from over-discharge. To recover from over-discharge latch-off, an input source plug-in is required at VBUS pin. The battery is charged with I_{SHORT} (typically 60mA) current when the $V_{BAT} < V_{SHORTZ}$, or pre-charge current as set in IPRECHG[3:0] register when the battery voltage is between V_{SHORTZ} and $V_{BATLOWV}$.

System Over-Current Protection

When the system is shorted or significantly overloaded ($I_{BAT} > I_{BATOP}$) and the current exceeds BATFET over-current limit, the BATFET latches off. Section **BATFET Enable Mode (Exit Shipping Mode)** can reset the latch-off condition and turn on BATFET.

Serial interface

The device uses I²C compatible interface for flexible charging parameter programming and instantaneous device status reporting. I²CTM is a bi-directional 2-wire serial interface developed by Philips Semiconductor (now NXP Semiconductors). Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL). Devices can be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The device operates as a slave device with address 6BH, receiving control inputs from the master device like micro controller or a digital signal processor through REG00-REG0B. Register read beyond REG0B (0x0B) returns 0xFF. The I²C interface supports both standard mode (up to 100kbits), and fast mode (up to 400kbits). Connecting to the positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain.

Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

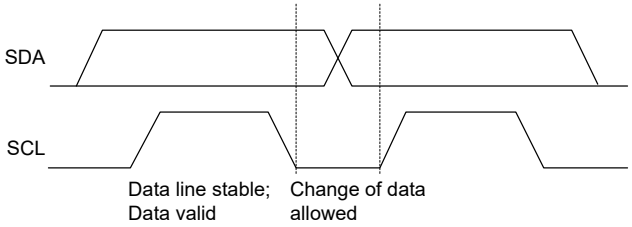


Figure 11. Bit Transfer on the I²C Bus

START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCl is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition. START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and free after the STOP condition.

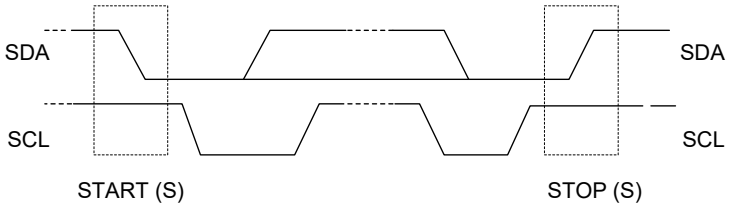


Figure 12. TS START and STOP conditions

DETAILED DESCRIPTION (continued)

Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the master into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and release the clock line SCL.

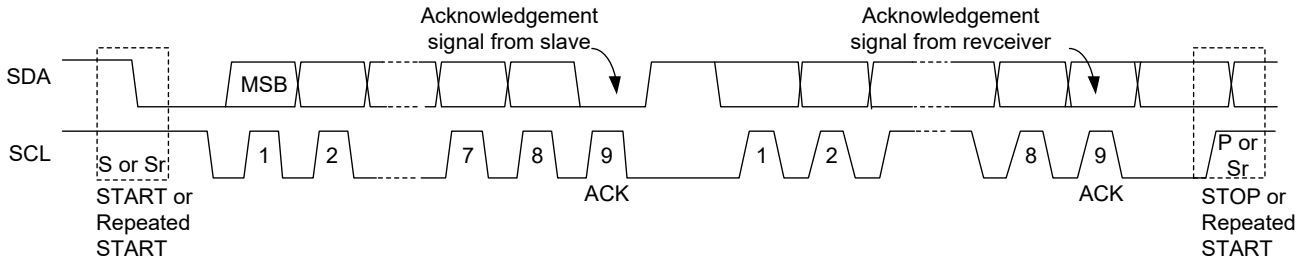


Figure 13. Data Transfer on the I²C Bus

Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge ninth clock pulse, are generated by the master. The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during the ninth clock pulse, this is the Not Acknowledge signal. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

DETAILED DESCRIPTION (continued)

Slave Address and Data Direction Bit

After the START, a slave address is sent. This address is 7 bits long followed by the eighth bit as a data direction bit (bit R/W). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).

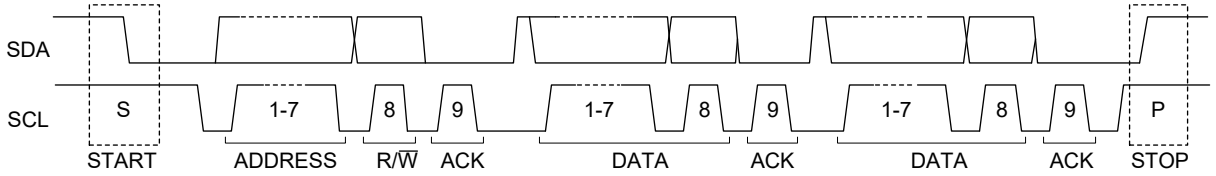


Figure 14. Complete Data Transfer

Single Read and Write

If the register address is not defined, the charger IC sends back NACK and goes back to the idle state.

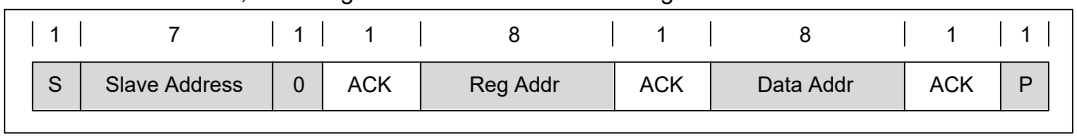


Figure 15. Single Write

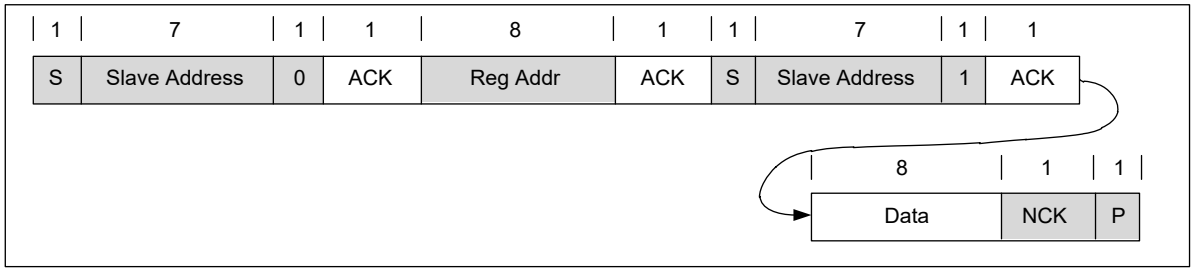


Figure 16. Single Read

Multi-Read and Multi-Write

The charger device supports multi-read and multi-write on REG00 through REG0B.

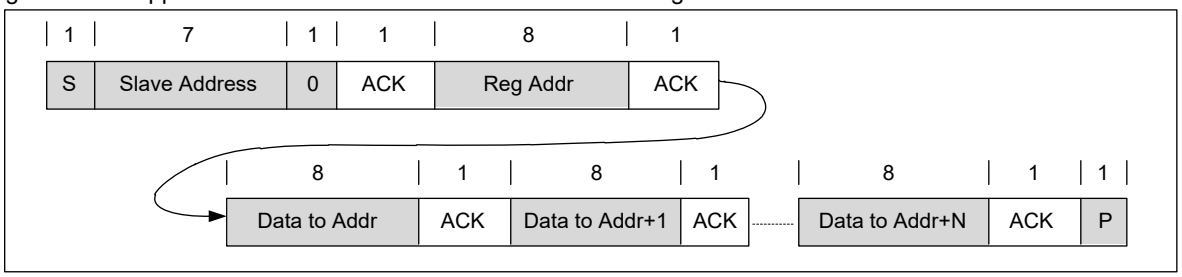


Figure 17. Multi-Write

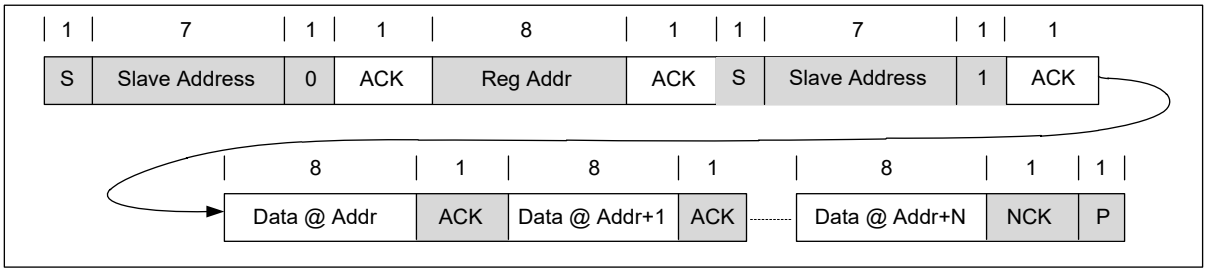


Figure 18. Multi-Read

DETAILED DESCRIPTION (continued)

REG09 is a fault register. It keeps all the fault information from last read until the host issues a new read. For example, if Charge Safety Timer Expiration fault occurs but recovers later, the fault register REG09 reports the fault when it is read the first time, but returns to normal when it is read the second time. In order to get the fault information at present, the host has to read REG09 for the second time. The only exception is NTC_FAULT which always reports the actual condition on the TS pin. In addition, REG09 does not support multi-read and multi-write.

REGISTER MAPS

I²C Slave Address: 6BH

REG00

Table 5. REG00 Register Description

BITS	BIT NAME	DESCRIPTION	COMMENT	POR	TYPE	RESET
D[7]	EN_HIZ	Enable HIZ Mode 0 = Disable (default) 1 = Enable		0	R/W	by REG_RST by Watchdog
D[6:5]	EN_ICHG_MON[1:0]	Enable STAT Pin Function 00 = Enable (default) 01 = Reserved 10 = Reserved 11 = Disable (float pin)		00	R/W	by REG_RST
D[4:0]	IINDPM[4:0]	IINDPM[4] 1 = 1600mA	Input Current Limit Offset: 100mA Range: 100mA (00000) - 3.2A (11111) Default: 2400mA (10111), maximum input current limit, not typical. IINDPM[4:0] bits are changed automatically after input source detection is completed. PSEL = High = 500mA PSEL = Low = 2400mA Host can over-write IINDPM[4:0] bits after input source detection is completed.	10111	R/W	by REG_RST
		IINDPM[3] 1 = 800mA				
		IINDPM[2] 1 = 400mA				
		IINDPM[1] 1 = 200mA				
		IINDPM[0] 1 = 100mA				

LEGEND: R/W = Read/Write; R = Read only.

REG01

Table 6. REG01 Register Description

BITS	BIT NAME	DESCRIPTION	COMMENT	POR	TYPE	RESET
D[7]	PFM_DIS	Enable PFM Mode 0 = Enable (default) 1 = Disable		0	R/W	by REG_RST
D[6]	WD_RST	I²C Watchdog Timer Reset 0 = Normal (default) 1 = Reset	Back to 0 after watchdog timer reset.	0	R/W	by REG_RST by Watchdog
D[5]	OTG_CONFIG	Enable OTG 0 = OTG disable (default) 1 = OTG enable	OTG_CONFIG would over-ride charge enable function in CHG_CONFIG.	0	R/W	by REG_RST by Watchdog
D[4]	CHG_CONFIG	Enable Charge Battery 0 = Charge disable 1 = Charge enable (default)	Charge battery is enabled when both nCE pin is pulled low and CHG_CONFIG bit is 1.	1	R/W	by REG_RST by Watchdog
D[3:1]	SYS_MIN[2:0]	Minimum System Voltage 000 = 2.6V 001 = 2.8V 010 = 3V 011 = 3.2V 100 = 3.4V 101 = 3.5V (default) 110 = 3.6V 111 = 3.7V		101	R/W	by REG_RST
D[0]	MIN_BAT_SEL	Minimum Battery Voltage for OTG Mode 0 = 2.8V V_{BAT} falling (default) 1 = 2.5V V_{BAT} falling	Default: 2.8V (0) V_{BAT} falling. V_{BAT} falling, $V_{BATLOWV\_OTG}$ = 2.8V; V_{BAT} rising, $V_{BATLOWV\_OTG}$ = 3.0V.	0	R/W	by REG_RST

LEGEND: R/W = Read/Write; R = Read only.

REGISTER MAPS (continued)

REG02

Table 7. REG02 Register Description

BITS	BIT NAME	DESCRIPTION	COMMENT	POR	TYPE	RESET
D[7]	BOOST_LIM	Boost Current Limit 0 = 0.5A 1 = 1.2A (default)	The current limit options listed are minimum current limit specs.	1	R/W	by REG_RST by Watchdog
D[6]	Q1_FULLON	Full FET 0 = Use higher Q1 R_{DSON} when programmed I_{INDPM} < 700mA (better accuracy) 1 = Use lower Q1 R_{DSON} always (better efficiency)	In boost mode, full FET is always used and this bit has no effect.	0	R/W	by REG_RST
D[5:0]	ICHG[5:0]	ICHG[5] 1 = 1920mA	Fast Charge Current Default: 2040mA (100010) Range: 0mA (000000) - 3000mA (110010) Notes: I_{CHG} = 0mA disables charge. Value above 110010 (3000mA) is clamped to register value 110010 (3000mA).	1	R/W	by REG_RST by Watchdog
		ICHG[4] 1 = 960mA		0	R/W	
		ICHG[3] 1 = 480mA		0	R/W	
		ICHG[2] 1 = 240mA		0	R/W	
		ICHG[1] 1 = 120mA		1	R/W	
		ICHG[0] 1 = 60mA		0	R/W	

LEGEND: R/W = Read/Write; R = Read only.

REG03

Table 8. REG03 Register Description

BITS	BIT NAME	DESCRIPTION	COMMENT	POR	TYPE	RESET
D[7:4]	IPRECHG[3:0]	IPRECHG[3] 1 = 480mA	Pre-Charge Current Offset: 60mA Range: 60mA (0000) - 780mA (1100) Default: 180mA (0010) Note: Value above 1100 (780mA) is clamped to register value 1100 (780mA).	0	R/W	by REG_RST by Watchdog
		IPRECHG[2] 1 = 240mA		0	R/W	
		IPRECHG[1] 1 = 120mA		1	R/W	
		IPRECHG[0] 1 = 60mA		0	R/W	
D[3:0]	ITERM[3:0]	ITERM[3] 1 = 480mA	Termination Current Offset: 60mA Default: 180mA (0010)	0	R/W	by REG_RST by Watchdog
		ITERM[2] 1 = 240mA		0	R/W	
		ITERM[1] 1 = 120mA		1	R/W	
		ITERM[0] 1 = 60mA		0	R/W	

LEGEND: R/W = Read/Write; R = Read only.

REGISTER MAPS (continued)

REG04

Table 9. REG04 Register Description

BITS	BIT NAME	DESCRIPTION	COMMENT	POR	TYPE	RESET
D[7:3]	VREG[4:0]	VREG[4] 1 = 512mV	Charge Voltage Offset: 3.856V Range: 3.856V (00000) to 4.624V (11000) Default: 4.208V (01011) Special Value: 4.352V (01111) Note: Value above 11000 (4.624V) is clamped to register value 11000 (4.624V).	0	R/W	by REG_RST by Watchdog
		VREG[3] 1 = 256mV		1	R/W	
		VREG[2] 1 = 128mV		0	R/W	
		VREG[1] 1 = 64mV		1	R/W	
		VREG[0] 1 = 32mV		1	R/W	
D[2:1]	TOPOFF_TIMER[1:0]	Top-Off Timer 00 = Disabled (default) 01 = 15 minutes 10 = 30 minutes 11 = 45 minutes	The extended time following the termination condition is met. When disabled, charge terminated when termination conditions are met.	0	R/W	by REG_RST by Watchdog
				0	R/W	
D[0]	VRECHG	Recharge Threshold 0 = 100mV (default) 1 = 200mV		0	R/W	by REG_RST by Watchdog

LEGEND: R/W = Read/Write; R = Read only.

REG05

Table 10. REG05 Register Description

BITS	BIT NAME	DESCRIPTION	COMMENT	POR	TYPE	RESET
D[7]	EN_TERM	Enable Termination 0 = Disable 1 = Enable (default)		1	R/W	by REG_RST by Watchdog
D[6]	Reserved	Reserved	Reserved	0	R/W	by REG_RST by Watchdog
D[5:4]	WATCHDOG[1:0]	Disable Watchdog Timer 00 = Disable timer 01 = 40s (default) 10 = 80s 11 = 160s		01	R/W	by REG_RST by Watchdog
D[3]	EN_TIMER	Enable Timer 0 = Disable 1 = Enable both fast charge and pre-charge timer (default)		1	R/W	by REG_RST by Watchdog
D[2]	CHG_TIMER	Charge Safety Timer 0 = 5hrs 1 = 10hrs (default)		1	R/W	by REG_RST by Watchdog
D[1]	TREG	Thermal Regulation Threshold 0 = 90℃ 1 = 110℃ (default)		1	R/W	by REG_RST by Watchdog
D[0]	JEITA_ISET (0C-10C)	JEITA Charging Current 0 = 50% of I_{CHG} 1 = 20% of I_{CHG} (default)		1	R/W	by REG_RST by Watchdog

LEGEND: R/W = Read/Write; R = Read only.

REGISTER MAPS (continued)

REG06

Table 11. REG06 Register Description

BITS	BIT NAME	DESCRIPTION	COMMENT	POR	TYPE	RESET
D[7:6]	OVP[1:0]	VAC OVP Threshold 00 = 5.5V 01 = 6.5V (5V input) (default) 10 = 10.5V (9V input) 11 = 14V (12V input)		0	R/W	by REG_RST
				1	R/W	
D[5:4]	BOOSTV[1:0]	Boost Regulation Voltage 00 = 4.85V 01 = 5.00V 10 = 5.15V (default) 11 = 5.30V		1	R/W	by REG_RST
				0	R/W	by REG_RST
D[3:0]	VINDPM[3:0]	VINDPM[3] 1 = 800mV	Absolute V_{INDPM} Threshold Offset: 3.9V Range: 3.9V (0000) - 5.4V (1111) Default: 4.5V (0110)	0	R/W	by REG_RST
		VINDPM[2] 1 = 400mV		1	R/W	
		VINDPM[1] 1 =200mV		1	R/W	
		VINDPM[0] 1 =100mV		0	R/W	

LEGEND: R/W = Read/Write; R = Read only.

REG07

Table 12. REG07 Register Description

BITS	BIT NAME	DESCRIPTION	COMMENT	POR	TYPE	RESET
D[7]	IINDET_EN	Input Current Limit Detection 0 = Not in input current limit detection (default) 1 = Force input current limit detection when VBUS is present	Return to 0 after input detection is completed.	0	R/W	by REG_RST by Watchdog
D[6]	TMR2X_EN	Enable Half Clock Rate Safety Timer 0 = Disable 1 = Safety timer slowed by 2× during input DPM (both V and I) or JEITA cool, or thermal regulation (default)		1	R/W	by REG_RST by Watchdog
D[5]	BATFET_DIS	Disable BATFET 0 = Allow Q4 to turn on (default) 1 = Turn off Q4 with t_{BATFET_DLY} delay time (REG07 D[3])		0	R/W	by REG_RST
D[4]	JEITA_VSET (45C-60C)	JEITA Charging Voltage 0 = Set charge voltage to 4.1V (MAX) (default) 1 = Set charge voltage to V_{REG}		0	R/W	by REG_RST by Watchdog
D[3]	BATFET_DLY	BATFET Delay 0 = Turn off BATFET immediately 1 = Turn off BATFET after t_{BATFET_DLY} (default)	BATFET_DIS bit is set.	1	R/W	by REG_RST
D[2]	BATFET_RST_EN	Enable BATFET Reset 0 = Disable BATFET reset 1 = Enable BATFET reset (default)		1	R/W	by REG_RST by Watchdog
D[1:0]	VDPM_BAT_ TRACK[1:0]	Dynamic VINDPM Tracking Setting 00 = Disable function (V_{INDPM} set by register) 01 = V_{BAT} + 200mV 10 = V_{BAT} + 250mV 11 = V_{BAT} + 300mV	Set VINDPM[3:0] to track V_{BAT} voltage. Actual V_{INDPM} is the higher of register value and V_{BAT} + VDPM_BAT_TRACK [1:0] offset.	0	R/W	by REG_RST
				0	R/W	by REG_RST

LEGEND: R/W = Read/Write; R = Read only.

REGISTER MAPS (continued)

REG08

Table 13. REG08 Register Description

BITS	BIT NAME	DESCRIPTION	POR	TYPE	RESET
D[7:5]	VBUS_STAT[2:0]	VBUS Status Register 000 = No input 001 = USB Host SDP (500mA) → PSEL HIGH 010 = Adapter 2.4A → PSEL LOW 111 = OTG Software current limit is reported in IINDPM[4:0] register	x	R	NA
			x	R	
			x	R	
D[4:3]	CHRG_STAT[1:0]	Charging Status 00 = Charge disable 01 = Pre-charge (< $V_{BATLOWV}$) 10 = Fast charging 11 = Charge termination	x	R	NA
			x	R	
D[2]	PG_STAT	Power Good Status 0 = Power not good 1 = Power good	x	R	NA
D[1]	THERM_STAT	Thermal Status 0 = Not in thermal regulation 1 = In thermal regulation	x	R	NA
D[0]	VSYS_STAT	System Regulation Voltage Status 0 = Not in VSYSMin regulation (V_{BAT} > V_{SYS_MIN}) 1 = In VSYSMin regulation (V_{BAT} < V_{SYS_MIN})	x	R	NA

LEGEND: R/W = Read/Write; R = Read only.

REG09

Table 14. REG09 Register Description

BITS	BIT NAME	DESCRIPTION	POR	TYPE	RESET
D[7]	WATCHDOG_FAULT	Watchdog Fault Flag 0 = Normal 1 = Watchdog timer expiration	x	R	NA
D[6]	BOOST_FAULT	Fault Flag in Boost Operation 0 = Normal 1 = VBUS overloaded in OTG, or VBUS OVP, or battery is too low (any conditions that prevent starting boost function)	x	R	NA
D[5:4]	CHRG_FAULT[1:0]	Charging Fault Register 00 = Normal 01 = Input fault (VAC OVP or V_{BAT} < V_{VBUS} < 3.8V) 10 = Thermal shutdown 11 = Charge safety timer expiration	x	R	NA
			x	R	NA
D[3]	BAT_FAULT	Battery OVP Fault Flag 0 = Normal 1 = Battery over-voltage	x	R	NA
D[2:0]	NTC_FAULT[2:0]	JEITA 000 = Normal 010 = Warm 011 = Cool 101 = Cold 110 = Hot (Buck mode) 000 = Normal 101 = Cold 110 = Hot (Boost mode)	x	R	NA
			x	R	NA
			x	R	NA

LEGEND: R/W = Read/Write; R = Read only.

REGISTER MAPS (continued)

REG0A

Table 15. REG0A Register Description

BITS	BIT NAME	DESCRIPTION	POR	TYPE	RESET
D[7]	VBUS_GD	Good Input Source Detected 0 = VBUS not attached 1 = VBUS attached	x	R	NA
D[6]	VINDPM_STAT	Input Voltage Regulation Limit Status 0 = Not in VINDPM 1 = In VINDPM	x	R	NA
D[5]	IINDPM_STAT	Input Current Regulation Limit Status 0 = Not in IINDPM 1 = In IINDPM	x	R	NA
D[4]	Reserved		x	R	NA
D[3]	TOPOFF_ACTIVE	Active Top-Off Timer 0 = Top-off timer not counting 1 = Top-off timer counting	x	R	NA
D[2]	ACOV_STAT	Input Over-voltage Status 0 = Device is not in ACOV 1 = Device is in ACOV	x	R	NA
D[1]	VINDPM_INT_MASK	VINDPM Event Detected (Maskable) 0 = Allow VINDPM INT pulse 1 = Mask VINDPM INT pulse	0	R/W	by REG_RST
D[0]	IINDPM_INT_MASK	IINDPM Event Detected (Maskable) 0 = Allow IINDPM INT pulse 1 = Mask IINDPM INT pulse	0	R/W	by REG_RST

LEGEND: R/W = Read/Write; R = Read only.

REG0B

Table 16. REG0B Register Description

BITS	BIT NAME	DESCRIPTION	POR	TYPE	RESET
D[7]	REG_RST	Register Reset 0 = Keep current register setting 1 = Reset to default register value and reset safety timer Note: Bit resets to 0 after register reset is completed	0	R/W	NA
D[6:3]	PN[3:0]	SGM41511: 0010	0	R	NA
			0	R	NA
			1	R	NA
			0	R	NA
D[2]	SGMPART		1	R	NA
D[1:0]	DEV_REV[1:0]		x	R	NA
			x	R	NA

LEGEND: R/W = Read/Write; R = Read only.

APPLICATION INFORMATION

A typical application consists of the device configured as an I²C controlled power path management device and a single cell battery charger for Li-Ion and Li-polymer batteries used in a wide range of smart phones and other portable devices. It integrates an input reverse blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and battery FET (BATFET Q4) between the system and battery. The device also integrates a bootstrap diode for the high-side gate drive.

Detailed Design Procedure

Inductor Selection

The 1.6MHz switching frequency allows the use of small inductor and capacitor values. Maintain an inductor saturation current higher than the charging current (I_{CHG}) plus half the ripple current (I_{RIPPLE}):

$$I_{SAT} \geq I_{CHG} + (1/2)\ I_{RIPPLE} \quad (3)$$

The inductor ripple current depends on the input voltage (V_{VBUS}), the duty cycle ($D = V_{BAT}/V_{VBUS}$), the switching frequency (f_S) and the inductance (L).

$$I_{RIPPLE} = \frac{V_{IN} \times D \times (1-D)}{f_S \times L} \quad (4)$$

The maximum inductor ripple current occurs when the duty cycle (D) is 0.5 or approximately 0.5. Usually inductor ripple is designed in the range between 20% and 40% maximum charging current as a trade-off between inductor size and efficiency for a practical design.

Input Capacitor

Design input capacitance to provide enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the charging current when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current I_{CIN} occurs where the duty cycle is closest to 50% and can be estimated using Equation 5.

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1-D)} \quad (5)$$

Low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and should be placed to the drain of the high-side MOSFET and source of the low-side MOSFET as close as possible. Voltage rating of the capacitor must be higher than normal input voltage level. A rating of 25V or higher capacitor is preferred for 15V input voltage. Capacitance of 22μF is suggested for typical of 3A to 4A charging current.

Output Capacitor

Ensure that the output capacitance has enough ripple current rating to absorb the output switching ripple current. Equation 6 shows the output capacitor RMS current I_{COUT} calculation.

$$I_{COUT} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \quad (6)$$

The output capacitor voltage ripple can be calculated as follows:

$$\Delta V_O = \frac{V_{OUT}}{8LCf_S^2}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

At certain input and output voltage and switching frequency, the voltage ripple can be reduced by increasing the output filter LC.

The charger device has internal loop compensation optimized for > 20μF ceramic output capacitance. The preferred ceramic capacitor is 10V rating, X7R or X5R.

APPLICATION INFORMATION (continued)

Power Supply Recommendations

In order to provide an output voltage on SYS, the SGM41511 device requires a power supply between 3.9V and 14.2V input with at least 100mA current rating connected to VBUS; or, a single-cell Li-Ion battery with voltage > $V_{BATUVLO}$ connected to BAT. The source current rating needs to be at least 3A in order for the buck converter of the charger to provide maximum output power to SYS.

Layout Guidelines

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loop (see Figure 19) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Follow this specific order carefully to achieve the proper layout.

1. Place input capacitor as close as possible to PMID pin and PGND pin connections and use shortest copper trace connection or PGND plane.

2. Place inductor input pin to SW pin as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.

3. Put output capacitor near to the inductor and the device. Ground connections need to be tied to the IC ground with a short copper trace connection or PGND plane.

4. Route analog ground separately from power ground. Connect analog ground and connect power ground separately. Connect analog ground and power ground together using thermal pad as the single ground connection point. Or using a 0Ω resistor to tie analog ground to power ground.

5. Use single ground connection to tie charger power ground to charger analog ground. Just beneath the device. Use ground copper pour but avoid power pins to reduce inductive and capacitive noise coupling.

6. Place decoupling capacitors next to the IC pins and make trace connection as short as possible.

7. It is critical that the exposed thermal pad on the backside of the device package be soldered to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers.

8. Ensure that the number and sizes of vias allow enough copper for a given current path.

Layout Example

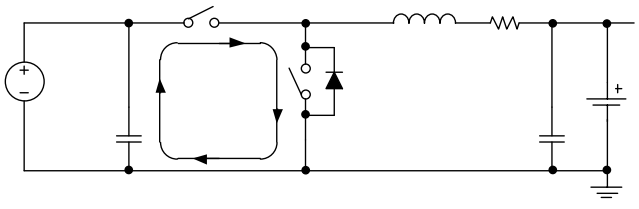
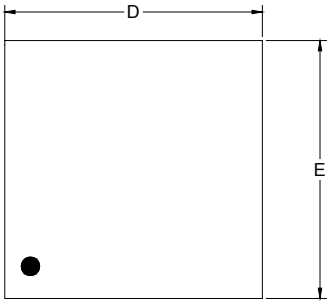


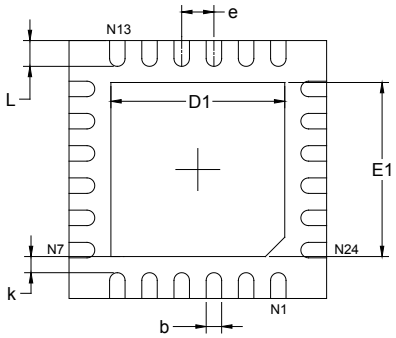
Figure 19. High Frequency Current Path

PACKAGE OUTLINE DIMENSIONS

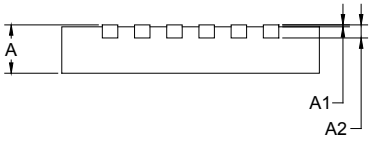
TQFN-4×4-24L



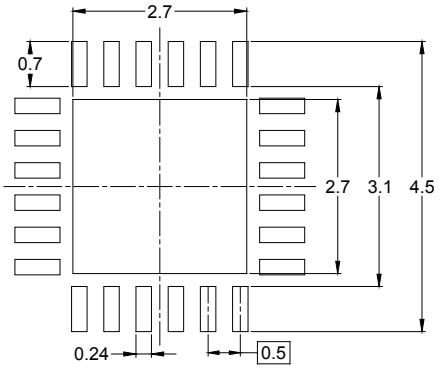
TOP VIEW



BOTTOM VIEW



SIDE VIEW

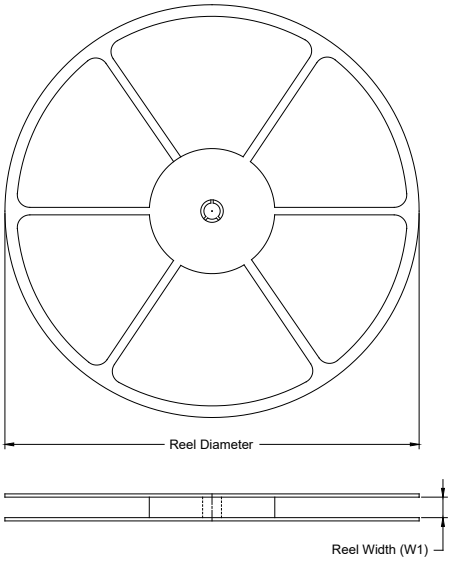


RECOMMENDED LAND PATTERN (Unit: mm)

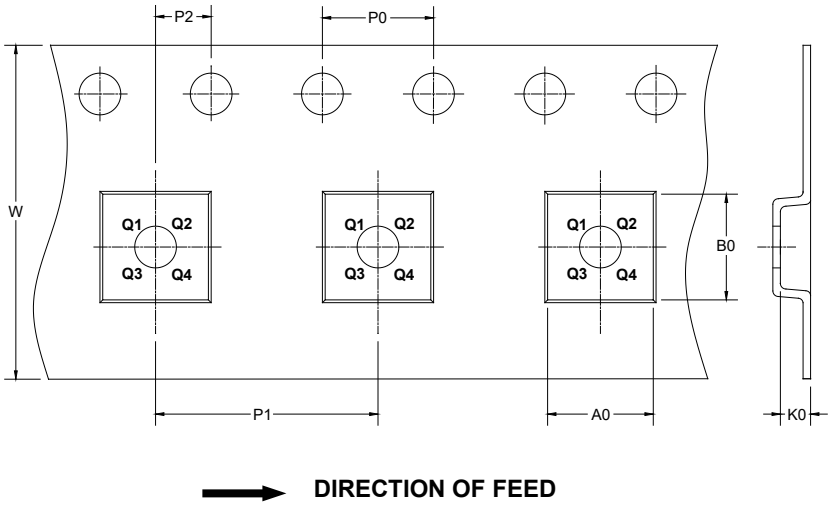
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	3.900	4.100	0.154	0.161
D1	2.600	2.800	0.102	0.110
E	3.900	4.100	0.154	0.161
E1	2.600	2.800	0.102	0.110
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.300	0.500	0.012	0.020

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



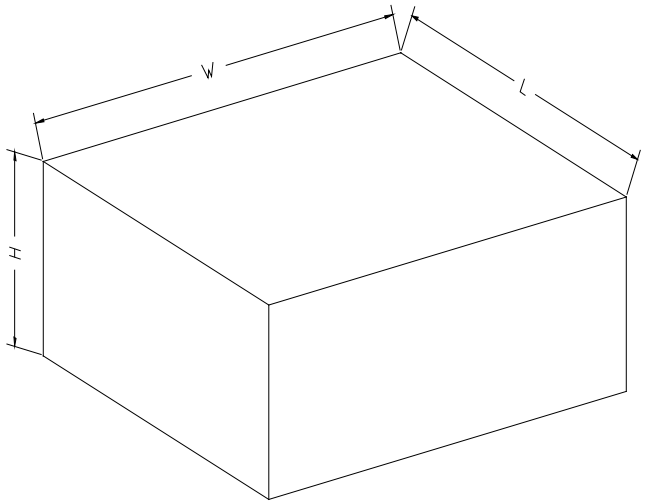
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-4×4-24L	13″	12.4	4.30	4.30	1.10	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002