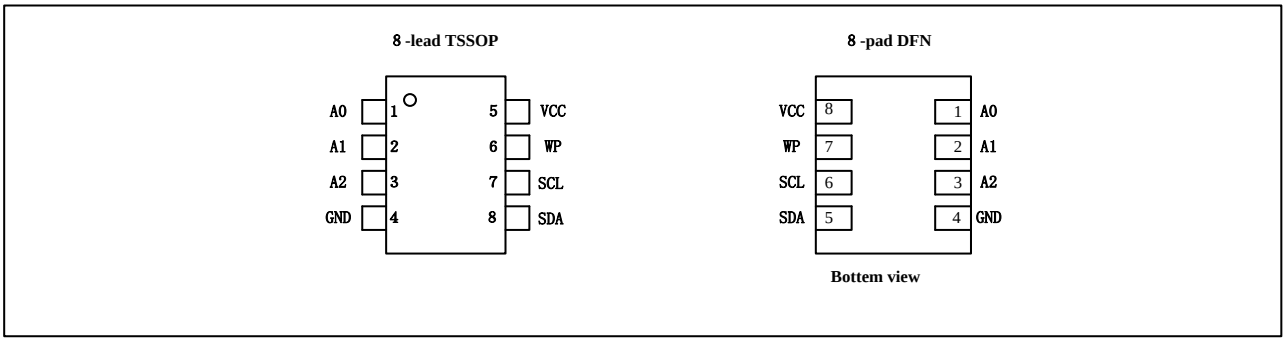
## Features

- Compatible with SMBus serial interface:
  - Up to 400 KHz transfer rate
- Memory array:
  - 2 Kbits organized as two 128-byte blocks
- Software data protection for lower 128-byte block
- Write:
  - Byte Write within 3 ms
  - 16 bytes Page Write within 3 ms
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Single supply voltage:
  - 1.7 V to 3.6 V
- High-reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
- Enhanced ESD/latch-up protection
  - HBM 6000V

## Description

- The BL34C02A is a 256-byte EEPROM device designed to operate the I2C Bus in the 1.7 V-3.6 V voltage range, with a maximum of 400 KHz transfer rate in the 1.7 V – 3.6 V voltage range。
- Locking the lower 128-byte block may be accomplished using a software write protection mechanism in conjunction with a high input voltage $V_{HV}$ on input A0.

## Pin Configuration



## Pin Descriptions

| Pin Name | Type | Functions |
|---|---|---|
| A0-A2 | I | Address Inputs |
| SDA | I/O | Serial Data |
| SCL | I | Serial Clock Input |
| WP | I | Write Protect |
| $V_{SS}$ | P | Ground |
| $V_{CC}$ | P | Power Supply |

**Table 1**

## Block Diagram

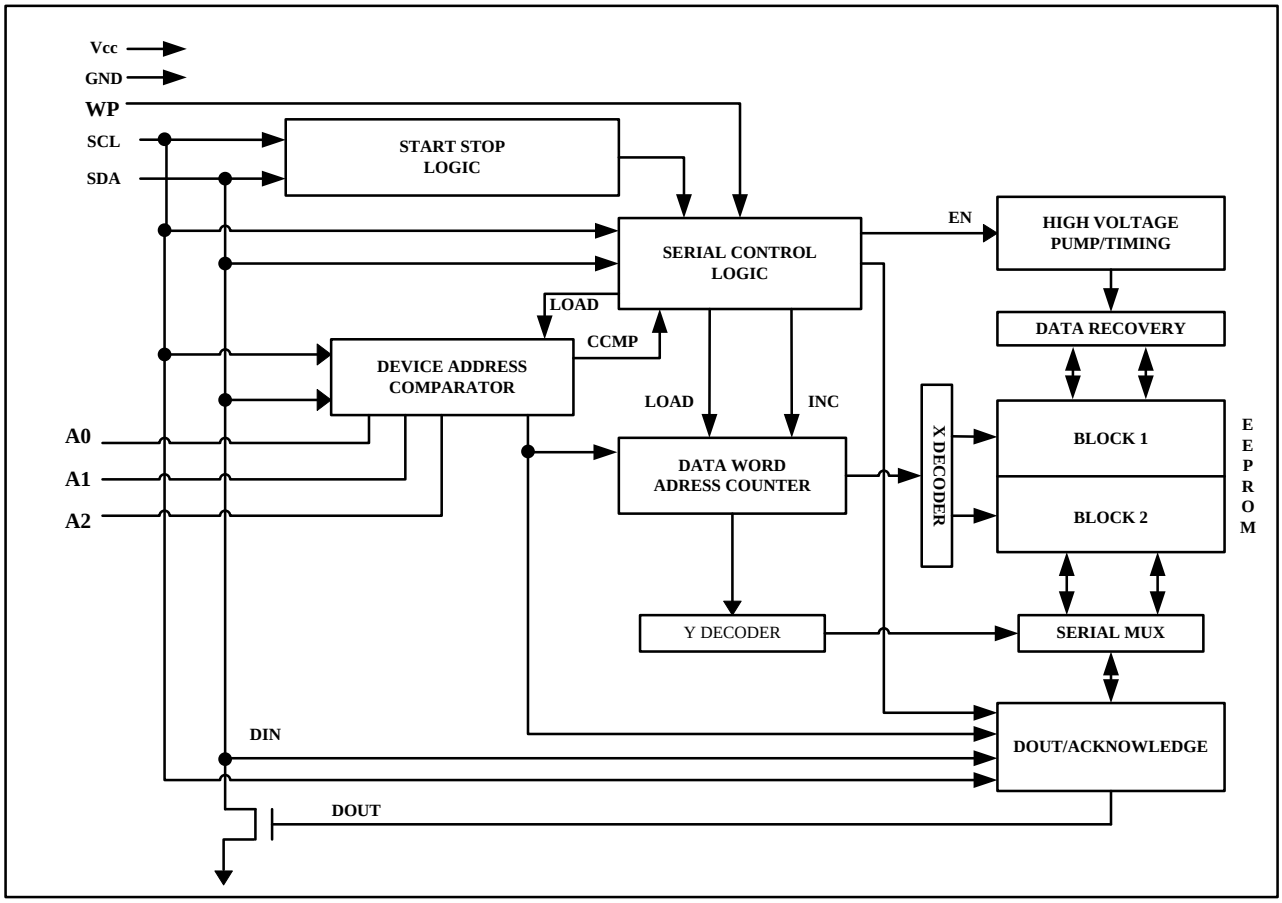



**Figure 1**

DEVICE/PAGE ADDRESSES (A2, A1 and A0): The A2, A1 and A0 pins are device address inputs that are hard wire for the BL34C02A. Eight 2K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section).

The A0 input is used to detect the $V_{HV}$ voltage, when decoding an SWP or CWP instruction.

SERIAL DATA (SDA): The SDA pin is bi-directional for serial data transfer. This pin is open-drain driven and may be wire-OR' ed with any number of other open-drain or open- collector devices.

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

WRITE PROTECT (WP): The BL34C02A has a Write Protect pin that provides hardware data protection. The Write Protect pin allows normal read/write operations when connected to ground (GND). When the Write Protection pin is connected to Vcc, the write protection feature is enabled.

# Functional Description

## 1. Memory addressing

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the device select code, shown in **Table 2** (on Serial Data (SDA), most significant bit first).

The device select code consists of a 4-bit device type identifier, and a 3-bit Chip Enable "Address" (A2, A1, A0). To address the memory array, the 4-bit device type identifier is 1010b; to access the write-protection settings, it is 0110b.

| | Chip Enable signals | | | Device type identifier | | | | Chip Enable bits | | | RW |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| Memory area selectcode (two arrays) | A2 | A1 | A0 | 1 | 0 | 1 | 0 | A2 | A1 | A0 | RW |
| Set write protection(SWP) | VSS | VSS | VHV | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| Clear write protection(CWP) | VSS | VCC | VHV | | | | | 0 | 1 | 1 | 0 |
| Permanently set write protection (PSWP) | A2 | A1 | A0 | | | | | A2 | A1 | A0 | 0 |
| Read SWP | VSS | VSS | VHV | | | | | 0 | 0 | 1 | 1 |
| Read CWP | VSS | VCC | VHV | | | | | 0 | 1 | 1 | 1 |
| Read PSWP | A2 | A1 | A0 | | | | | A2 | A1 | A0 | 1 |

**Table 2**

Up to eight memory devices can be connected on a single serial bus. Each one is given a unique 3-bit code on the slave address (A2, A1, A0) inputs. When the device select code is received, the device only responds if the slave address is the same as the value on the slave address (A2, A1, A0) inputs.

The 8th bit is the Read/Write bit (RW). This bit is set to 1 for Read and 0 for Write operations.
If a match occurs on the device select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9th bit time. If the device does not match the device select code, it deselects itself from the bus, and goes into Standby mode.

## 2. Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see **Figure 2**). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see **Figure 3**).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (see **Figure 3**).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a "0" to acknowledge that it has received each word. This happens during the ninth clock cycle.

STANDBY MODE: The BL34C02A features a low-power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the STOP bit and the completion of any internal operations.

MEMORY RESET: After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these steps:

1. Clock up to 9 cycles.

2. Look for SDA high in each cycle while SCL is high.

3. Create a start condition.

**Figure 2. Data Validity**

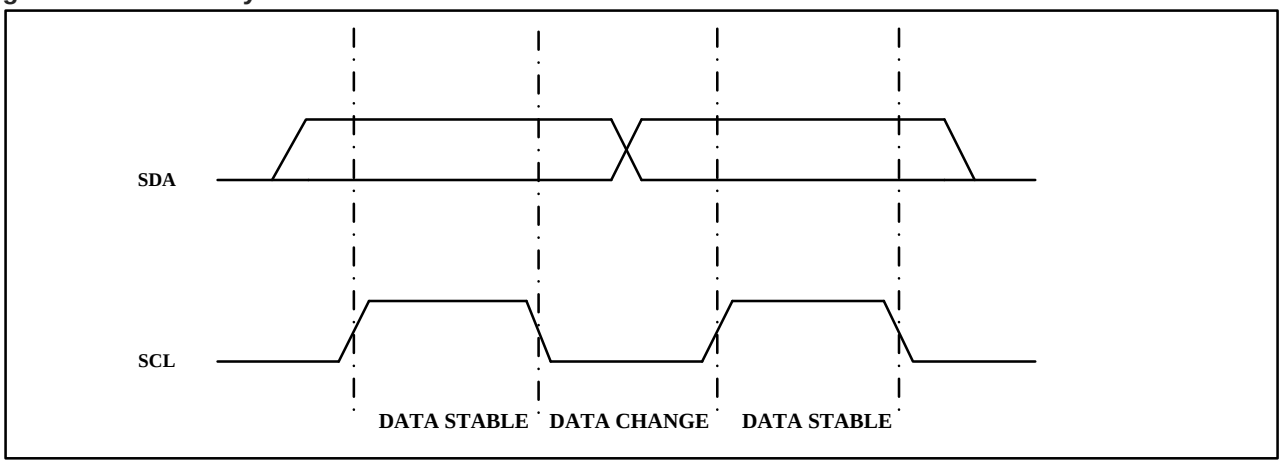



**Figure 3. Start and Stop Definition**

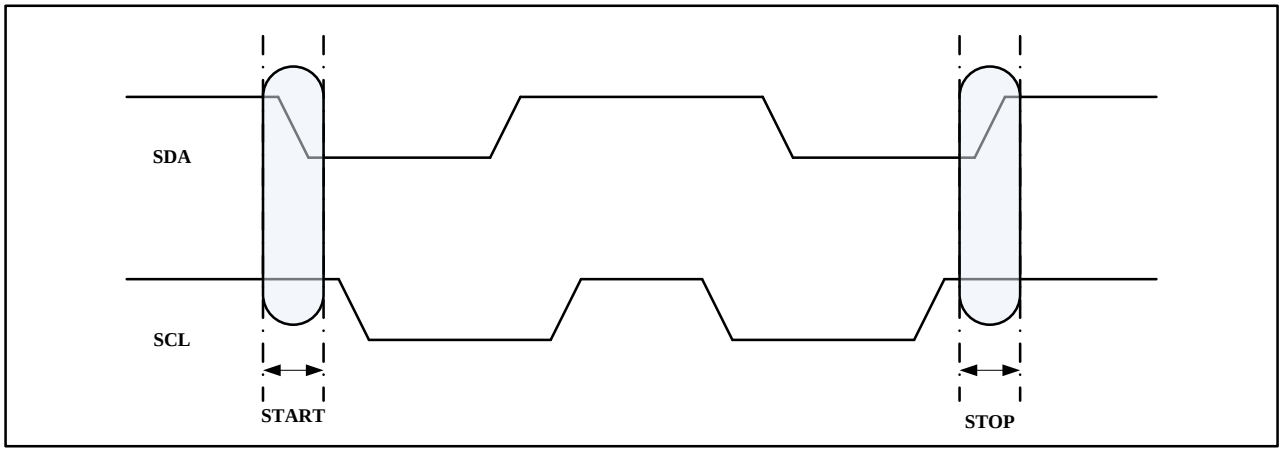
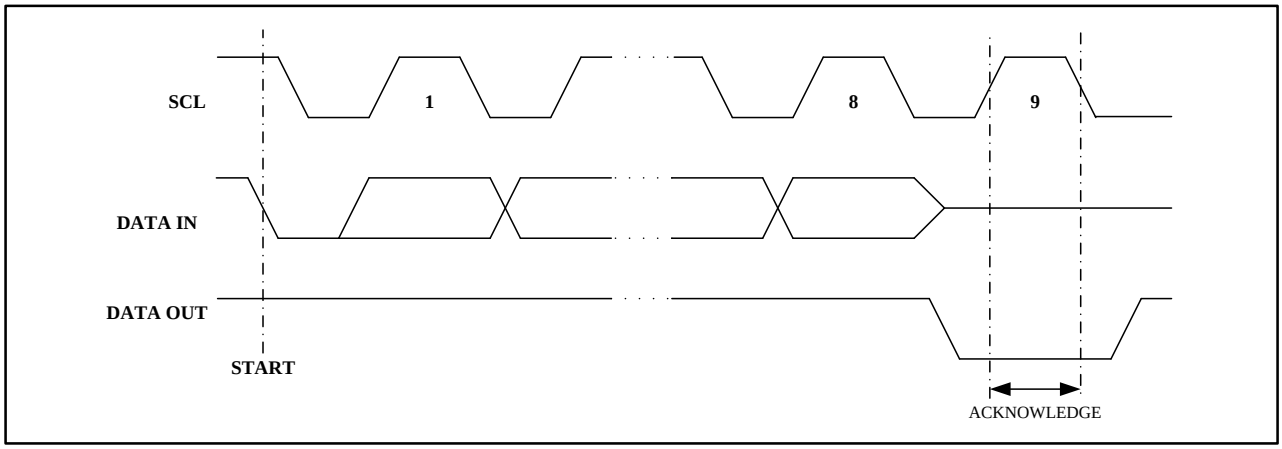


**Figure 4. Output Acknowledge**




DATA SECURITY: The BL34C02A has a hardware data protection scheme that allows the user to write protect the entire memory when the WP pin is at $V_{CC}$.

## 3. Write Operations

If the addressed location is hardware write-protected, the device replies to the data byte with NoAck, and the location is not modified.

BYTE WRITE: A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a "0" and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a "0" and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, $t_{WR}$, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete ( **Figure 6**).

If the addressed location is hardware write-protected, the device replies to the data byte with NoAck, and the location is not modified.

PAGE WRITE: The Page write mode allows up to 16 bytes to be written in a single Write cycle, provided that they are all located in the same page in the memory. A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a "0" and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a "0" and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, $t_{WR}$, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see **Figure 7**).

The data word address lower five bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 16 data words are transmitted to the EEPROM, the data word address will "roll over" and previous data will be overwritten.

If the addressed location is hardware write-protected, the device replies to the data byte with NoAck, and the location is not modified.

ACKNOWLEDGE POLLING: Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a "0", allowing the read or write sequence to continue.

## 4. Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to "1". There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page. Once the device address with the read/write select bit set to "1" is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input "0" but does generate a following stop condition (see **Figure 8**).

RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a "0" but does generate a following stop condition (see **Figure 9**)

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a "0" but does generate a following stop condition (see **Figure 10**).

**Figure 5. WORD ADDRESS**

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|

**Figure 6. Byte Write**

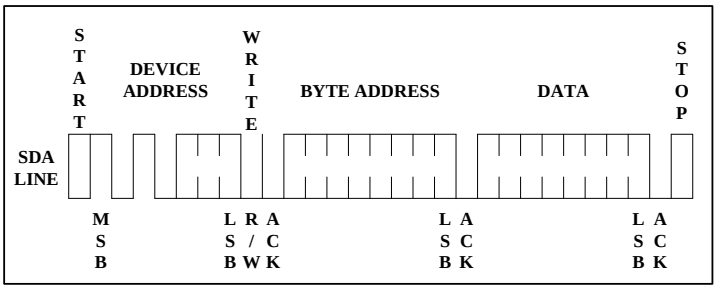



**Figure 7. Page Write**

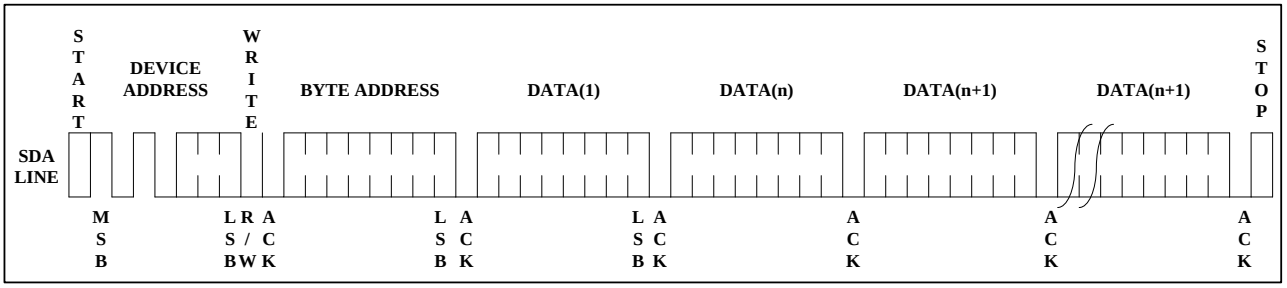



**Figure 8. Current Address Read**

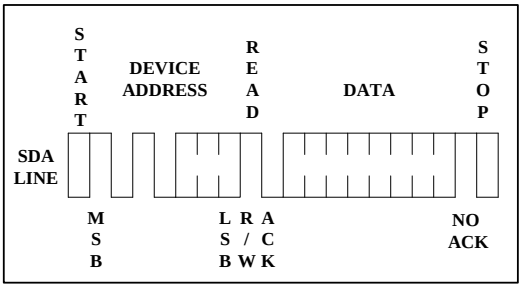



**Figure 9. Random Read**

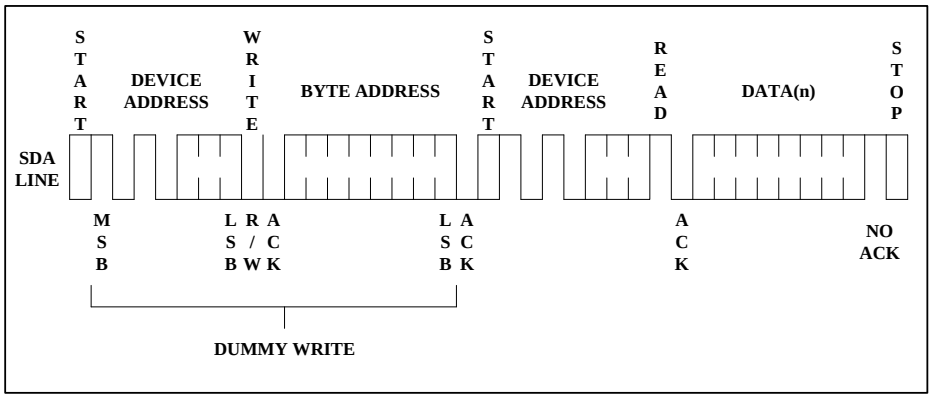
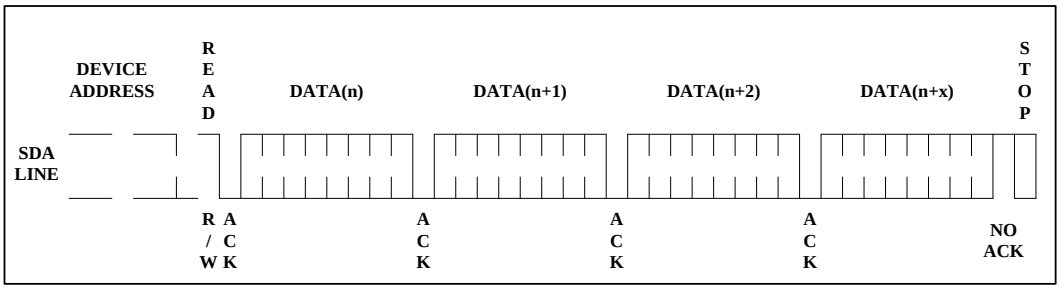


**Figure 10. Sequential Read**




## 5. Setting the write protection

The BL34C02A has a hardware write-protection feature, using the Write Protect (WP) signal. This signal can be driven high or low, and must be held constant for the whole instruction sequence. When Write Protect (WP) is held high, the whole memory array (addresses 00h to FFh) is write protected. When Write Protect (WP) is held low, the write protection of the memory array is dependent on whether software write-protection has been set.

Software write-protection allows the bottom half of the memory area (addresses 00h to 7Fh) to be write protected irrespective of subsequent states of the Write Protect (WP) signal.

Software write-protection is handled by three instructions:

- SWP: Set Write Protection
- CWP: Clear Write Protection
- PSWP: Permanently Set Write Protection

The level of write-protection (set or cleared) that has been defined using these instructions, remains defined even after a power cycle.

## 6. SWP and CWP

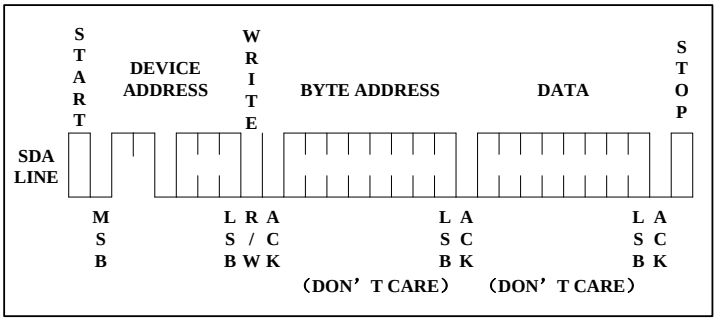
If the software write-protection has been set with the SWP instruction, it can be cleared again with a CWP instruction.

The two instructions (SWP and CWP) have the same format as a Byte Write instruction, but with a different device type identifier (as shown in Table 2). Like the Byte Write instruction, it is followed by an address byte and a data byte, but in this case the contents are all "Don't Care" (Figure 7). Another difference is that the voltage, VHV, must be applied on the A0 pin, and specific logical levels must be applied on the other two (A1 and A2, as shown in Table 2).

## 7. PSWP

If the software write-protection has been set with the PSWP instruction, the first 128 bytes of the memory are permanently write-protected. This write-protection cannot be cleared by any instruction, or by power-cycling the device, and regardless the state of Write Protect (WP). Also, once the PSWP instruction has been successfully executed, the BL34C02A no longer acknowledges any instruction (with a device type identifier of 0110) to access the write-protection settings.

**Figure 11. Setting the write protection (WP = 0)**




## Use within a DDR1/DDR2/DDR3 DRAM module

In the application, the BL34C02A is soldered directly in the printed circuit module. The three Chip Enable inputs (A0, A1, A2) must be connected to VSS or VCC directly (that is without using a pull-up or pull-down resistor) through the DIMM socket (see Table 4). The pull-up resistors needed for normal behavior of the I2C bus are connected on the I2C bus of the mother-board (as shown in Figure 12).

The Write Protect (WP) of the BL34C02A can be left unconnected. However, connecting it to VSS is recommended, to maintain full read and write access.

| DIMM position | A2 | A1 | A0 |
|---|---|---|---|
| 0 | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ |
| 1 | $V_{SS}$ | $V_{SS}$ | $V_{CC}$ |
| 2 | $V_{SS}$ | $V_{CC}$ | $V_{SS}$ |
| 3 | $V_{SS}$ | $V_{CC}$ | $V_{CC}$ |
| 4 | $V_{CC}$ | $V_{SS}$ | $V_{SS}$ |
| 5 | $V_{CC}$ | $V_{SS}$ | $V_{CC}$ |
| 6 | $V_{CC}$ | $V_{CC}$ | $V_{SS}$ |
| 7 | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ |

**Table3**

### 1. Programming the BL34C02A

The situations in which the BL34C02A is programmed can be considered under two headings:

- when the DDR DRAM is isolated (not inserted on the PCB motherboard)
- when the DDR DRAM is inserted on the PCB motherboard

Isolated DRAM module: With specific programming equipment, it is possible to define the BL34C02A content, using Byte and Page Write instructions, and its write-protection using the SWP and CWP instructions. To issue the SWP and CWP instructions, the DRAM module must be inserted in a specific slot where the A0 signal can be driven to VHV during the whole instruction. This programming step is mainly intended for use by DRAM module makers, whose end application manufacturers will want to clear this write-protection with the CWP on their own specific programming equipment, to modify the lower 128 bytes, and finally to set permanently the write-protection with the PSWP instruction.

DRAM module inserted in the application motherboard: As the final application cannot drive the A0 pin to VHV,

the only possible action is to freeze the write-protection with the PSWP instruction. Table 4 and Table 5 show how the Ack bits can be used to identify the write-protection status.

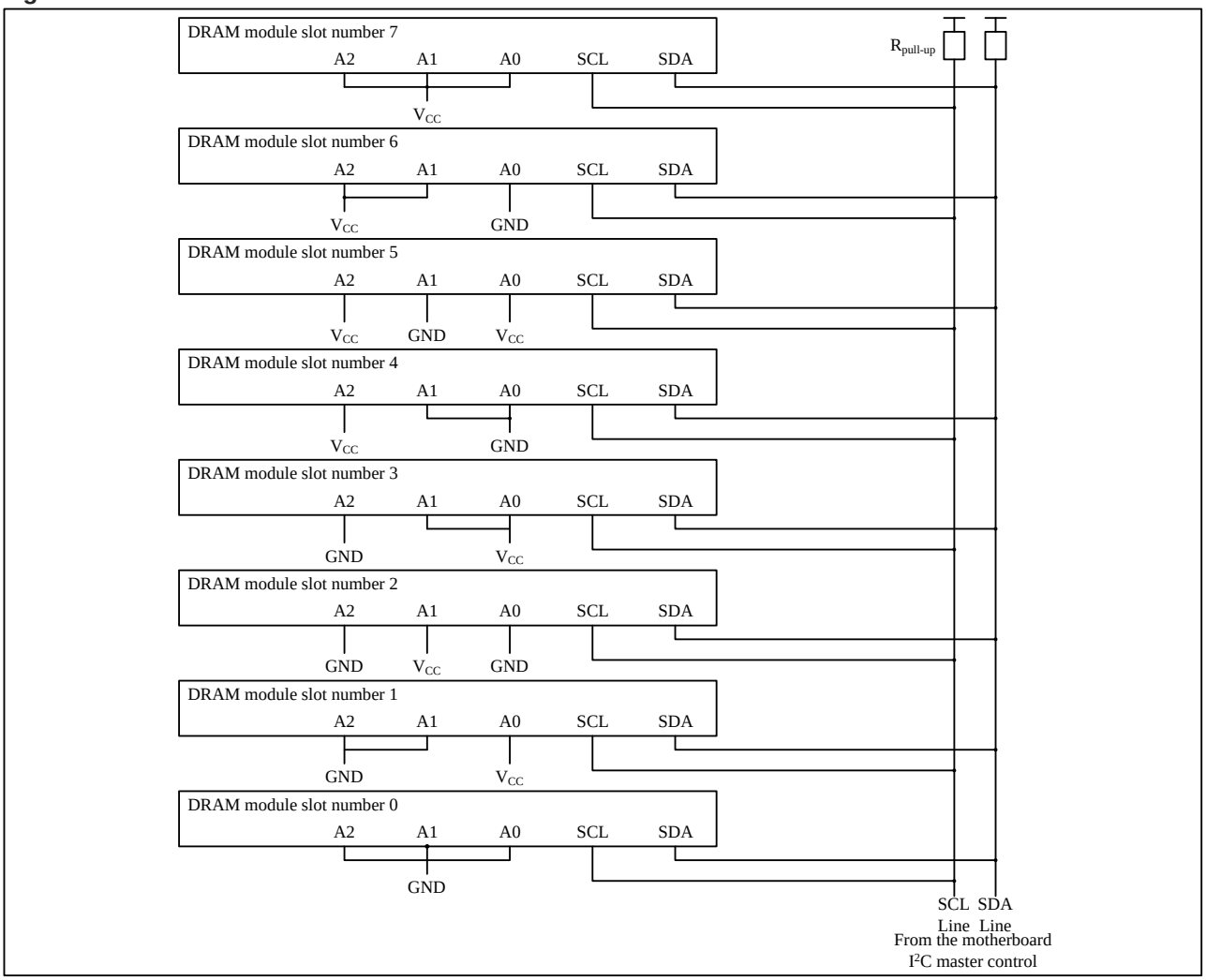
| Status | WP Input | Instruction | Ack | Address | Ack | Data byte | Ack | Write cycle ($t_W$) |
|---|---|---|---|---|---|---|---|---|
| Permanently protected | X | PSWP, SWP or CWP | NoAck | Not significant | NoAck | Not significant | NoAck | No |
| | | Page or Byte Write in lower 128 bytes | Ack | Address | Ack | Data | NoAck | No |
| Protected With SWP | 0 | SWP | NoAck | Not significant | NoAck | Not significant | NoAck | No |
| | | CWP | Ack | Not significant | Ack | Not significant | Ack | Yes |
| | | PSWP | Ack | Not significant | Ack | Not significant | Ack | Yes |
| | | Page or byte write in protected block | Ack | Address | Ack | Data | NoAck | No |
| Protected With SWP | 1 | SWP | NoAck | Not significant | NoAck | Not significant | NoAck | No |
| | | CWP | Ack | Not significant | Ack | Not significant | NoAck | No |
| | | PSWP | Ack | Not significant | Ack | Not significant | NoAck | No |
| | | Page or byte write | Ack | Address | Ack | Data | NoAck | No |
| Not Protected | 0 | PSWP, SWP or CWP | Ack | Not significant | Ack | Not significant | Ack | Yes |
| | | Page or byte write | Ack | Address | Ack | Data | Ack | Yes |
| | 1 | PSWP, SWP or CWP | Ack | Not significant | Ack | Not significant | Ack | No |
| | | Page or byte write | Ack | Address | Ack | Data | Ack | No |

**Table4**

| Status | Instruction | Ack | Address | Ack | Data byte | Ack |
|---|---|---|---|---|---|---|
| Permanently protected | PSWP, SWP or CWP | NoAck | Not significant | NoAck | Not significant | NoAck |
| Protected with SWP | SWP | NoAck | Not significant | NoAck | Not significant | NoAck |
| Protected with SWP | CWP | Ack | Not significant | NoAck | Not significant | NoAck |
| Protected with SWP | PSWP | Ack | Not significant | NoAck | Not significant | NoAck |
| Not protected | PSWP, SWP or CWP | Ack | Not significant | NoAck | Not significant | NoAck |

**Table5**

**Figure. 12**


DRAM module slot number 7
A2 A1 A0 SCL SDA
VCC
DRAM module slot number 6
A2 A1 A0 SCL SDA
VCC GND
DRAM module slot number 5
A2 A1 A0 SCL SDA
VCC GND VCC
DRAM module slot number 4
A2 A1 A0 SCL SDA
VCC GND
DRAM module slot number 3
A2 A1 A0 SCL SDA
GND VCC
DRAM module slot number 2
A2 A1 A0 SCL SDA
GND VCC GND
DRAM module slot number 1
A2 A1 A0 SCL SDA
GND VCC
DRAM module slot number 0
A2 A1 A0 SCL SDA
GND
Rpull-up
SCL Line
SDA Line
From the motherboard
I2C master control

## Electrical Characteristics

Absolute Maximum Stress Ratings：

- DC Supply Voltage . . . . . -0.5V to +6.5V
- Input / Output Voltage . . . . . GND-0.3V to VCC+0.3V
- Voltage on Pin A0. . . . . -0.5V to +10V
- Operating Ambient Temperature . . . . . -40℃ to +95℃
- Storage Temperature . . . . . .-65℃ to +150℃
- Electrostatic pulse (Human Body model) . . . . . 6000V

Comments:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

## DC Electrical Characteristics

Applicable over recommended operating range from: TA = -40℃ to +85℃, VCC = +1.7V to +3.6V (unless otherwise noted)

**Table 6. DC characteristics**

| Symbol | Parameter | Test condition (in addition to those in Table 8) | Min | Max | Unit |
|---|---|---|---|---|---|
| $I_{LI}$ | Input leakage current (SCL,SDA, A0, A1, A2) | $V_{IN}$ = GND or $V_{CC}$ | - | ±2 | µA |
| $I_{LO}$ | Output leakage current | SDA in Hi-Z, external voltage applied on SDA: GND or $V_{CC}$ | - | ±2 | µA |
| $I_{CC}$ | Supply current (read) | $f_c$ = 400 kHz or 1 MHz | - | 1 | mA |
| $I_{CC0}$ | Supply current (write) | During $t_W$, $V_{IN}$ = GND or $V_{CC}$ | - | 1 (1) | mA |
| $I_{CC1}$ | Standby supply current | Device not selected (2), $V_{IN}$ = GND or $V_{CC}$, $V_{CC}$ ⩾ 2.2 V | - | 2 | µA |
| | | Device not selected (2), $V_{IN}$ = GND or $V_{CC}$, $V_{CC}$ < 2.2 V | - | 1 | µA |
| $V_{IL}$ | Input low voltage (SCL, SDA, WP) | - | -0.45 | 0.3 x $V_{CC}$ | V |
| $V_{IH}$ | Input high voltage (SCL, SDA, WP) | - | 0.7 x $V_{CC}$ | $V_{CC}$+1 V | V |
| $V_{HV}$ | A0 high voltage detect | $V_{CC}$ < 2.2 V | 7 | 10 | V |
| | | $V_{CC}$ ⩾ 2.2 V | $V_{CC}$+4.8 V | 10 | V |
| $V_{OL}$ | Output low voltage | $I_{OL}$ = 0.15 mA | - | 0.2 | V |
| | | $I_{OL}$ = 3 mA | - | 0.4 | V |

1. The device is not selected after a power-up, after a read command (after the Stop condition), or after the completion of the internal write cycle $t_W$ ($t_W$ is triggered by the correct decoding of a write command).

## Pin Capacitance

Applicable over recommended operating range from TA = 25℃, f = 400kHz, VCC = +1.7V

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Input/Output Capacitance(SDA) | $C_{I/O}$ | - | - | 8 | pF | $V_{IO}$=0V |
| Input Capacitance(A0,A1,A2,SCL) | $C_{IN}$ | - | - | 6 | pF | $V_{IN}$=0V |

## AC Electrical Characteristics

Applicable over recommended operating range from TA = -40℃ to +85℃, VCC = +1.7V to +3.6V, CL = 1 TTL Gate and 100 pF (unless otherwise noted)

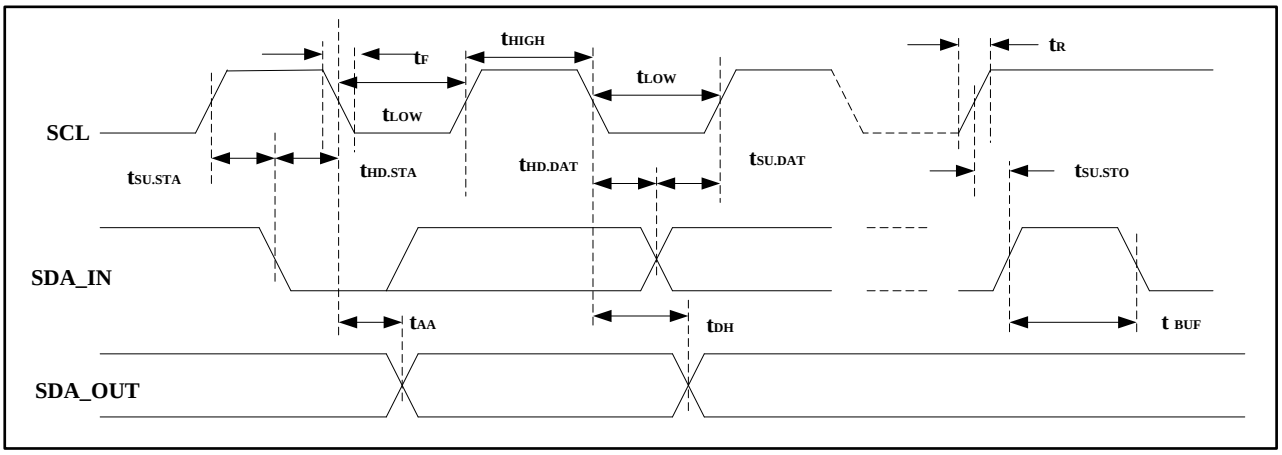
**Table 7. AC characteristics**

| Symbol | | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $f_{SCL}$ | $f_C$ | Clock frequency | 10 | 400 | kHz |
| $t_{HIGH}$ | $t_{CHCL}$ | Clock pulse width high time | 600 | - | ns |
| $t_{LOW}$ | $t_{CLCH}$ | Clock pulse width low time | 1300 | - | ns |
| $t_F$ | $t_{DL1DL2}$ (1) | SDA (out) fall time | 20 | 300 | ns |
| $t_R$ | $t_{XH1XH2}$ (2) | Input signal rise time | 20 | 300 | ns |
| $t_F$ | $t_{QL1QL2}$ (2) | Input signal fall time | 20 | 300 | ns |
| $t_{SU:DAT}$ | $t_{DXCH}$ | Data in setup time | 100 | - | ns |
| $t_{HD:DI}$ | $t_{CLDX}$ | Data in hold time | 0 | - | ns |
| $t_{HD:DAT}$ | $t_{CLQX}$ (3) | Data out hold time | 200 | 900 | ns |
| $t_{SU:STA}$ | $t_{CHDL}$ (4) | Start condition setup time | 600 | - | ns |
| $t_{HD:STA}$ | $t_{DLCL}$ | Stop condition hold time | 600 | - | ns |
| $t_{SU:STO}$ | $t_{CHDH}$ | Stop condition setup time | 600 | - | ns |
| $t_{BUF}$ | $t_{DHDL}$ | Time between Stop Condition and next Start Condition | 1300 | - | ns |
| $t_W$ | | Write time | - | 3 | ms |

1. Sampled only, not 100% tested.
2. Values recommended by I²C-bus/Fast-Mode specification.
3. To avoid spurious Start and Stop conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.
4. For a re-Start condition, or following a Write cycle.

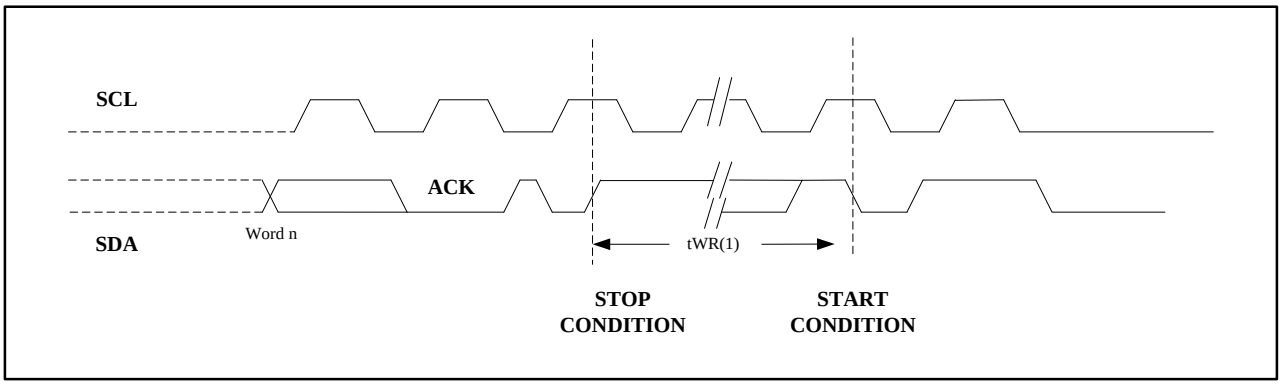
## Bus Timing

**Figure 13. SCL: Serial Clock, SDA: Serial Data I/O**




## Write Cycle Timing

**Figure 14. SCL: Serial Clock, SDA: Serial Data I/O**

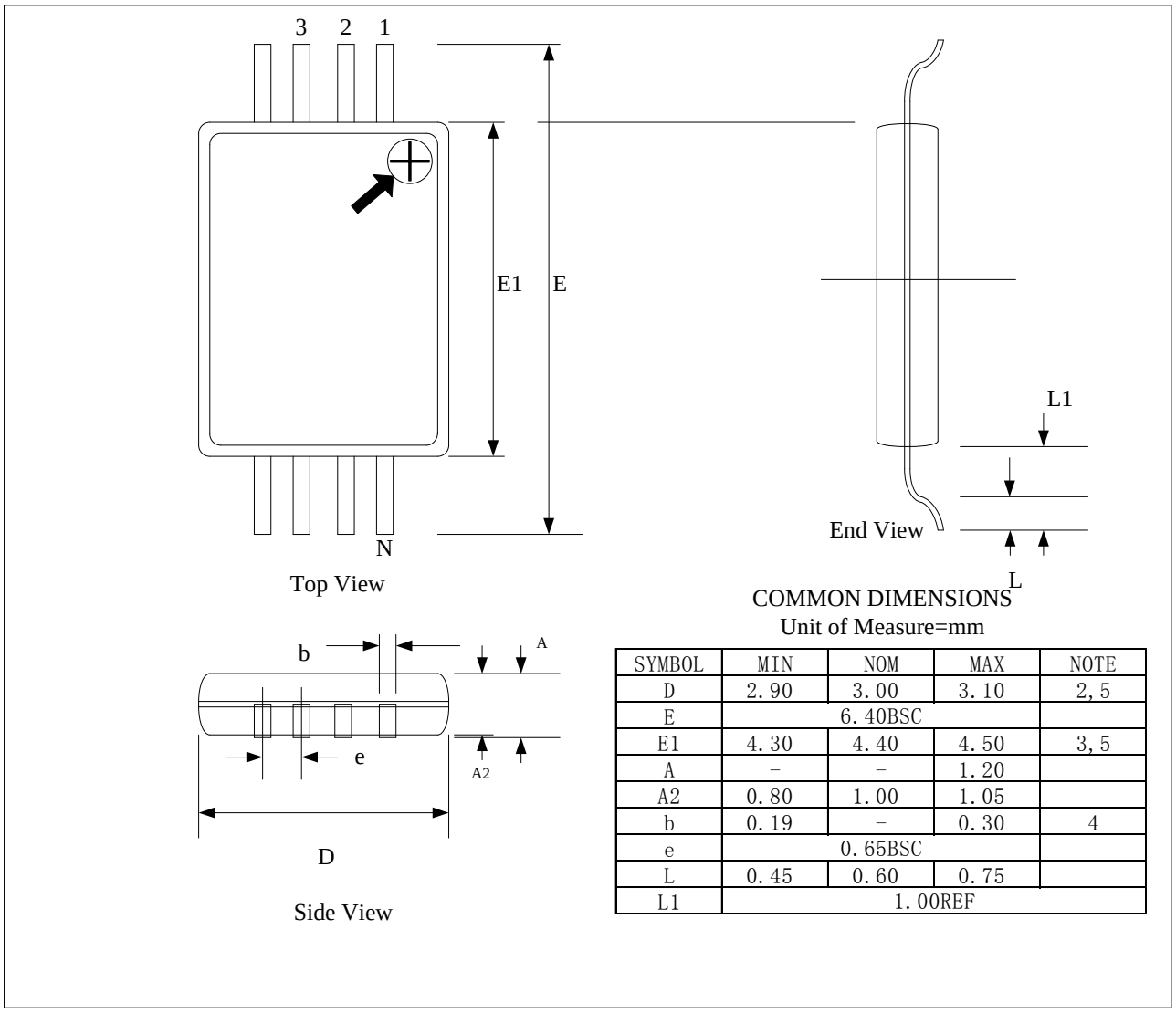



Notes:

The write cycle time $t_{WR}$ is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

# Package Information

## TSSOP




COMMON DIMENSIONS
Unit of Measure=mm

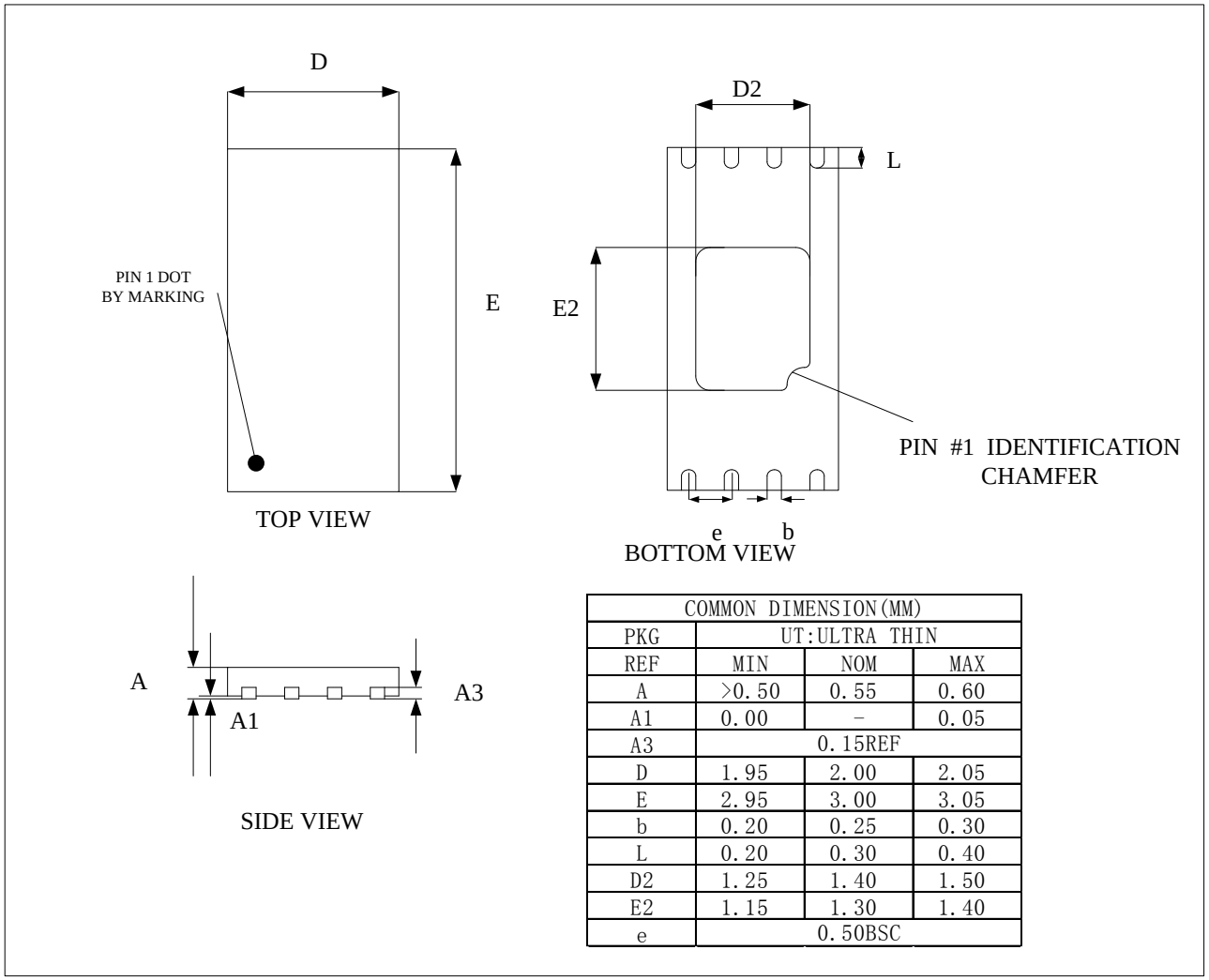
| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| D | 2.90 | 3.00 | 3.10 | 2,5 |
| E | | 6.40BSC | | |
| E1 | 4.30 | 4.40 | 4.50 | 3,5 |
| A | - | - | 1.20 | |
| A2 | 0.80 | 1.00 | 1.05 | |
| b | 0.19 | - | 0.30 | 4 |
| e | | 0.65BSC | | |
| L | 0.45 | 0.60 | 0.75 | |
| L1 | | 1.00REF | | |

**Figure 15**

NOTES:

1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006 in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010 in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07 mm.
5. Dimension D and E1 to be determined at Datum Plane H.

## UDFN




| COMMON DIMENSION(MM) | | | |
|---|---|---|---|
| PKG | UT:ULTRA THIN | | |
| REF | MIN | NOM | MAX |
| A | >0.50 | 0.55 | 0.60 |
| A1 | 0.00 | - | 0.05 |
| A3 | 0.15REF | | |
| D | 1.95 | 2.00 | 2.05 |
| E | 2.95 | 3.00 | 3.05 |
| b | 0.20 | 0.25 | 0.30 |
| L | 0.20 | 0.30 | 0.40 |
| D2 | 1.25 | 1.40 | 1.50 |
| E2 | 1.15 | 1.30 | 1.40 |
| e | 0.50BSC | | |

**Figure 16**

## Ordering Information

BL34C02A- 1 2 3

| Code | Description |
|---|---|
| 1 | Package type<br>SF: TSSOP-8L<br>NT: UDFN-8L |
| 2 | Packing type<br>R: Tape and Reel<br>T: Tube |
| 3 | Feature<br>S: Standard (default, Pb Free RoHS Std.)<br>C: Green (Halogen Free) |

| Device | Package | Shipping(Qty/Packing) |
|---|---|---|
| BL34C02A | TSSOP8L | 3000/Tape &Reel |
| BL34C02A | UDFN | 3000/Tape &Reel |

## Revision history

| |
|---|
| **Version 1.00 BL34C02A** |
| Initial version |
| **Version 1.01 BL34C02A** |
| Modify DC/AC Electrical Characteristics |