Features

- Compatible with all I²C bidirectional data transfer protocol
- Memory array:
  - 128 Kbits (8 Kbytes) of EEPROM
  - Page size: 64 bytes
- Single supply voltage and high speed:
  - 1MHz@1.8V

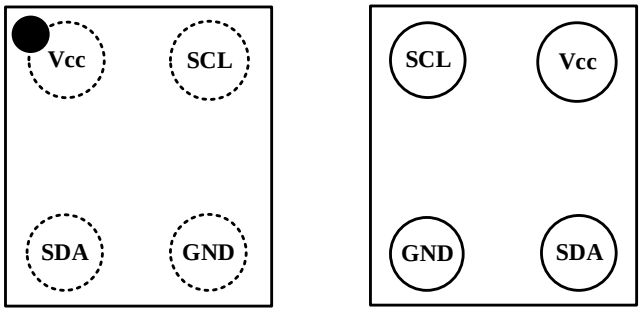
  Random and sequential Read modes
- Write:
  - Byte Write within 3 ms
  - Page Write within 3 ms
  - Partial Page Writes Allowed
- Software data Protection
- Slave Address Configurable
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- High-reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
- Enhanced ESD/Latch-up protection
- WLCSP4 Package

Description

- The BL24SA128D provides 131,072 bits of serial electrically erasable and programmable read-only memory (EEPROM), organized as 16,384 words of 8 bits each.
- The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential.

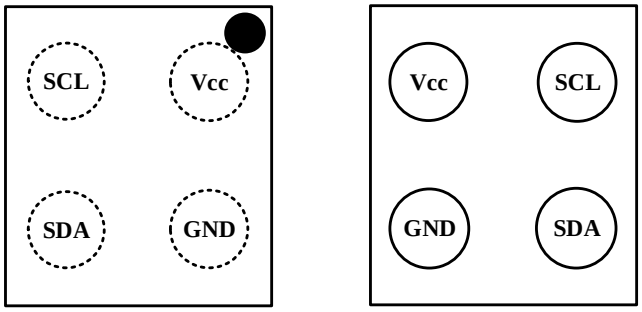
Pin Configuration

WLCSP 4 Ball Pitch 0.4mm*0.5mm



Marking side (Top view) **Pads side (Bottom view)**

WLCSP 4 Ball Pitch 0.4mm*0.4mm



Marking side (Top view) **Pads side (Bottom view)**

Pin Descriptions

Pin Name	Type	Functions
SDA	I/O	Serial Data
SCL	I	Serial Clock Input
GND	P	Ground
Vcc	P	Power Supply

Table 1

Block Diagram

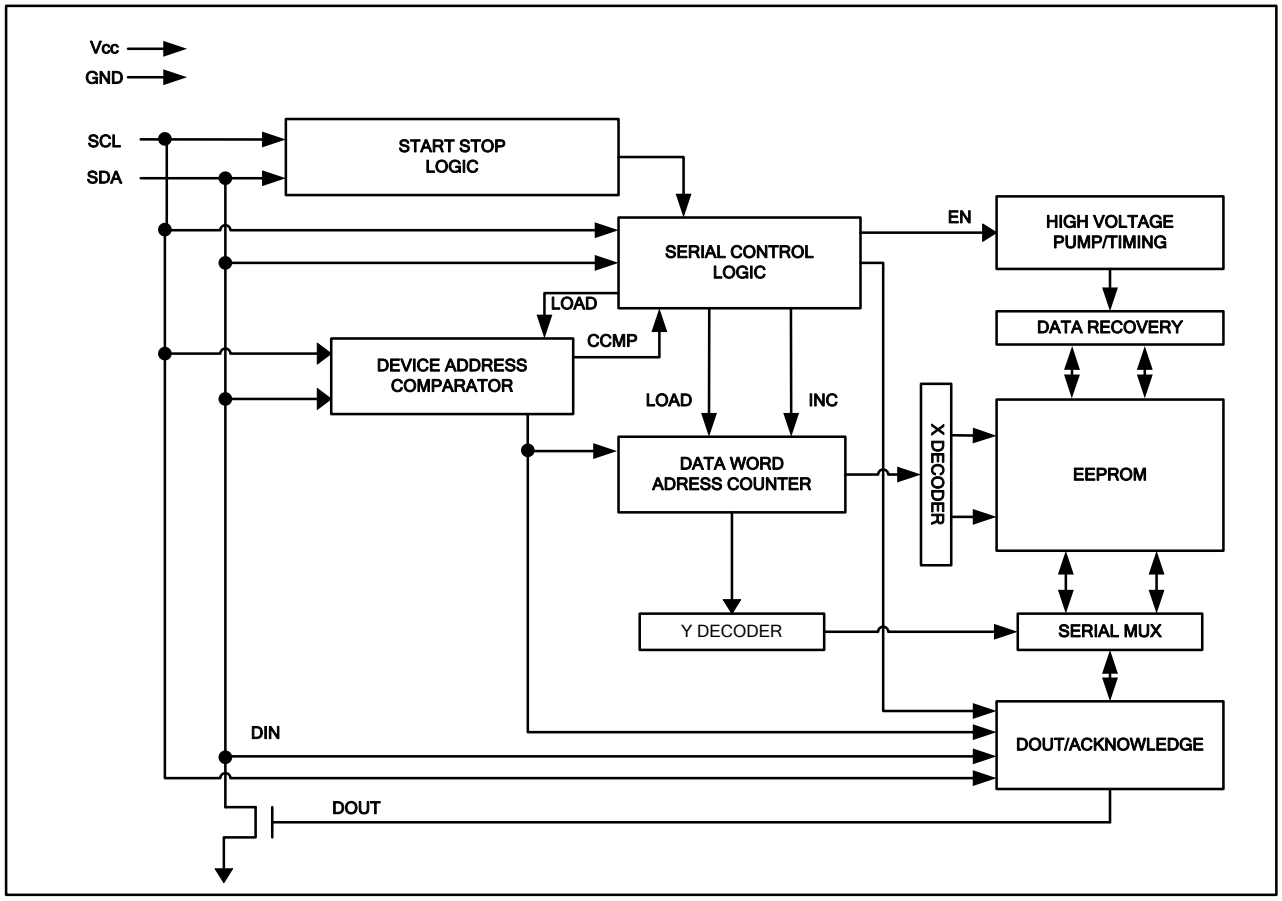


Figure 1

SERIAL DATA (SDA): The SDA pin is bi-directional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open- collector devices.

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

Functional Description

1. Memory Organization

BL24SA128D, 128k SERIAL EEPROM: Internally organized with 256 pages of 64 bytes each, the 128k requires a 14-bit data word address for random word addressing.

2. Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see **Figure 2**). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see **Figure 3**).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (see **Figure 3**).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a "0" to acknowledge that it has received each word. This happens during the ninth clock cycle.

STANDBY MODE: The BL24SA128D features a low-power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the STOP bit and the completion of any internal operations.

MEMORY RESET: After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these steps:

1. Clock up to 9 cycles.

2. Lock SDA high in each cycle while SCL is high.

3. Create a start condition.

Figure 2. Data Validity

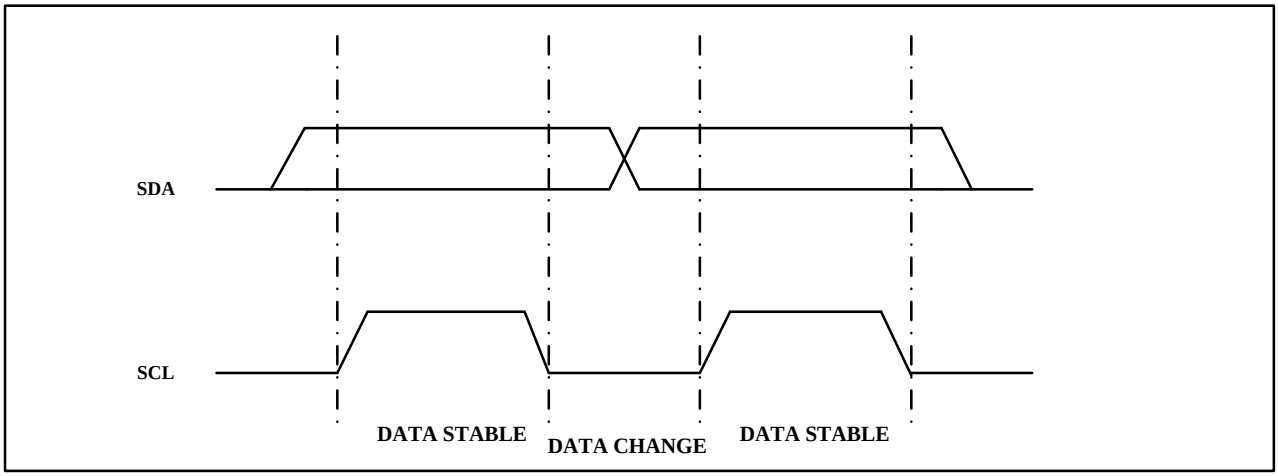


Figure 3. Start and Stop Definition

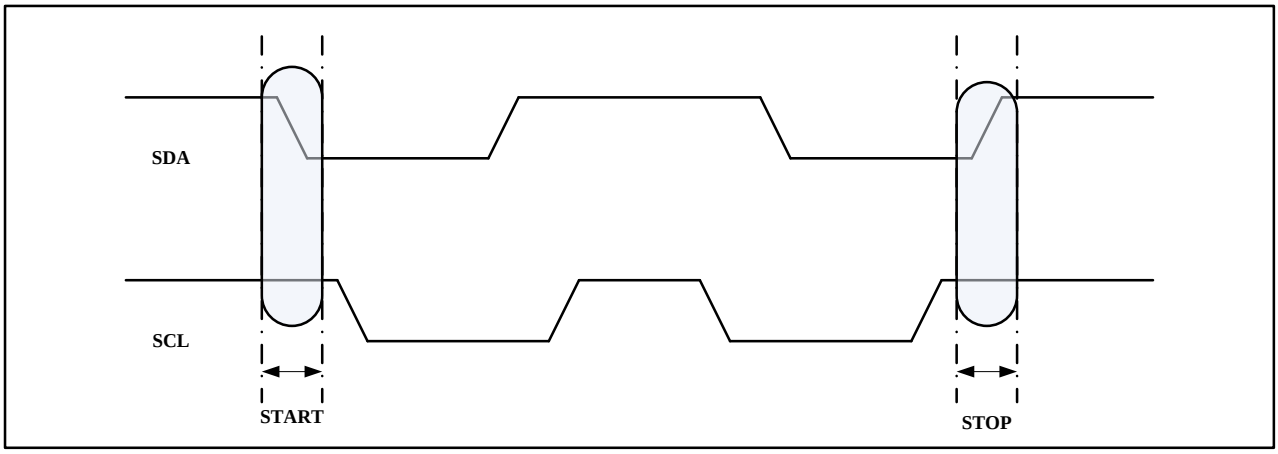
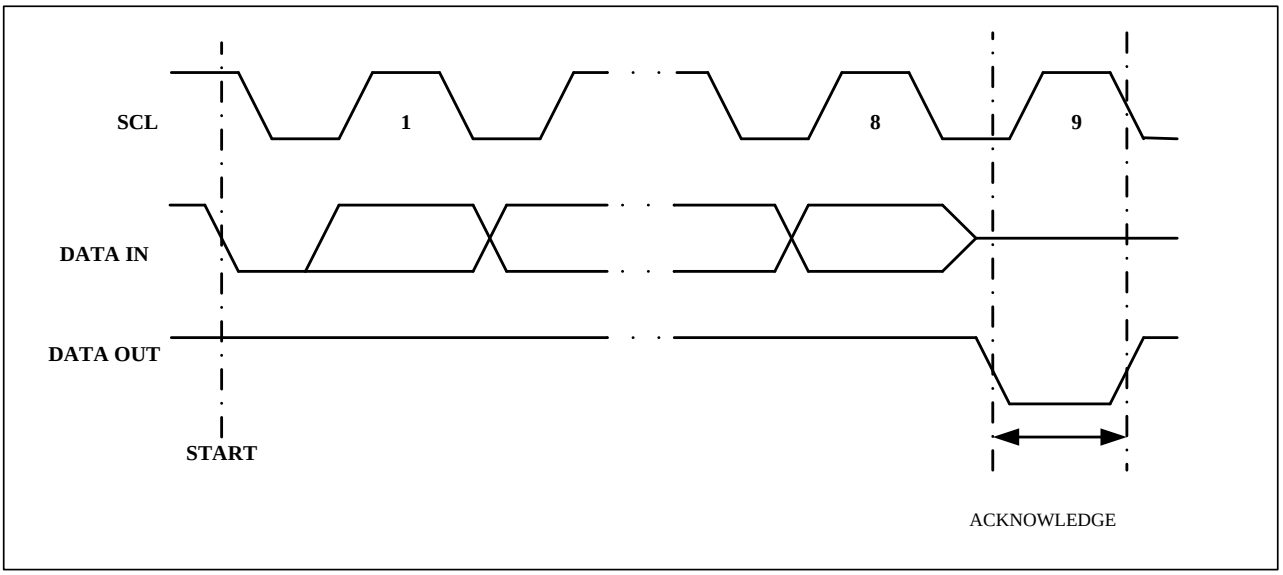


Figure 4. Output Acknowledge



3. Device Addressing

The 128k EEPROM devices all require an 8-bit device address word following a start condition to enable the chip for a read or write operation (see **Figure 5**)

MSB **LSB**

1	**0**	**1**	**0**	**A2**	**A1**	**A0**	**R/W**

Figure 5. Device Address

The device address word consists of a mandatory "1", "0" sequence for the first four most significant bits as shown. This is common to all the Serial EEPROM devices.

The fifth, sixth and seventh bits of the device address can be configured，default to 000b.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

BL24SA128D consists of a series of products with different fab-out default device address.

Part Number	A2	A1	A0
BL24SA128D	0	0	0
BL24SA128DA2	0	0	1
BL24SA128DA4	0	1	0
BL24SA128DA6	0	1	1
BL24SA128DA8	1	0	0
BL24SA128DAA	1	0	1
BL24SA128DAC	1	1	0
BL24SA128DAE	1	1	1

Table 2

4. Write Operations

BYTE WRITE: A write operation requires two 8-bit data word address, as as **Figure 6**, following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a "0" and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a "0" and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, tWR, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see **Figure 7**).

0	*****	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**

Figure 6. Date Word Address

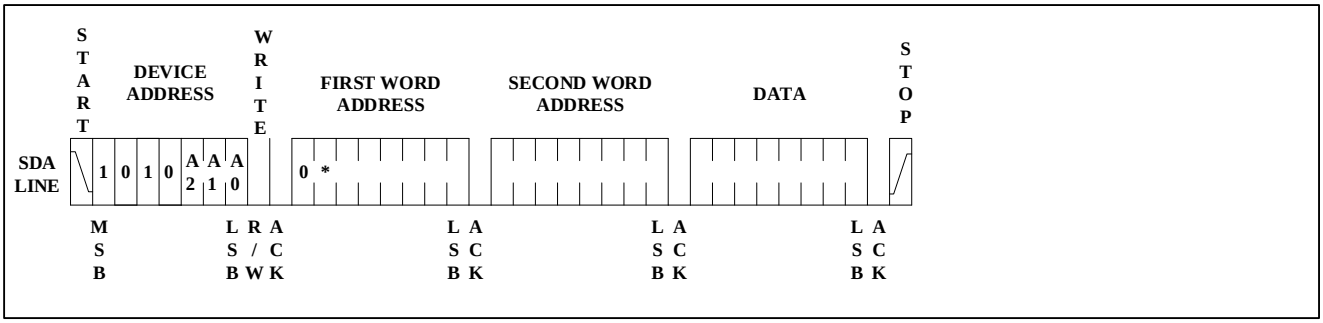


Figure 7. Byte Write

PAGE WRITE: The 128K EEPROM is capable of a 64-byte page writes. A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 63 more data words. The EEPROM will respond with a “0” after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see **Figure 8**).

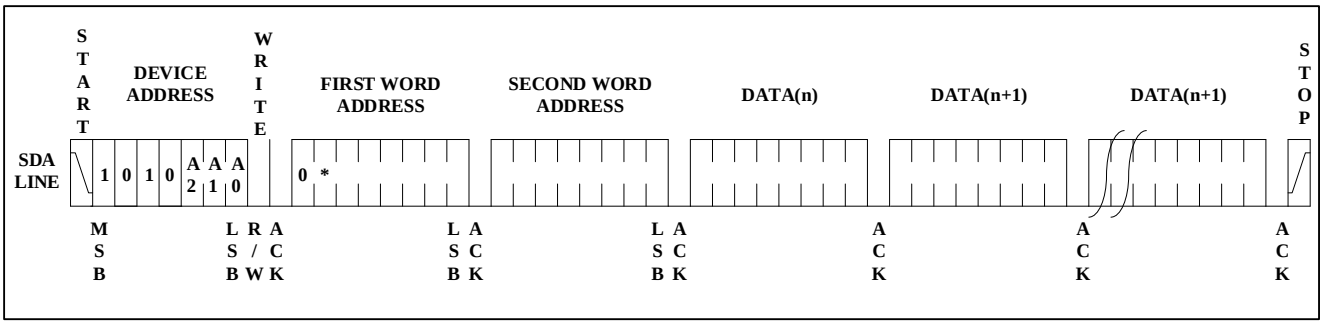


Figure 8. Page Write

The data word address lower six bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 64 data words are transmitted to the EEPROM, the data word address will "roll over" and previous data will be overwritten.

5. Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to "1". There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page. Once the device address with the read/write select bit set to "1" is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input "0" but does generate a following stop condition (see **Figure 9**).

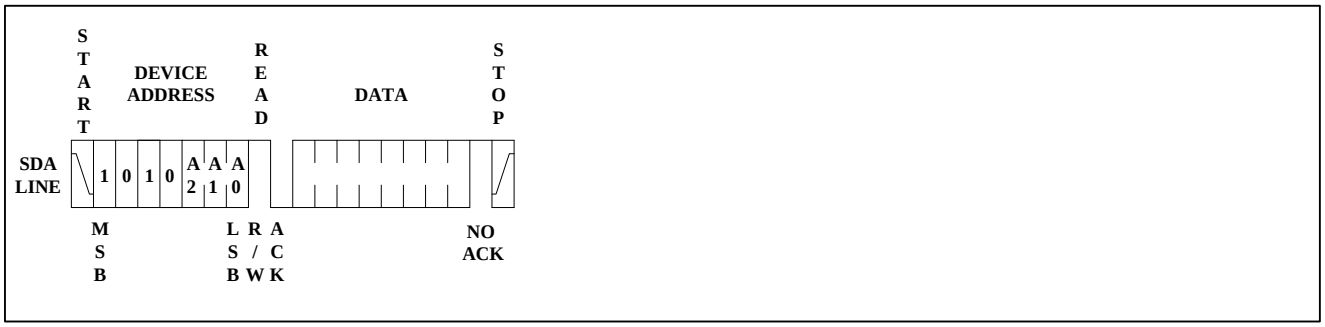


Figure 9. Current Address Read

RANDOM READ:

A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a "0" but does generate a following stop condition (see **Figure 10**)

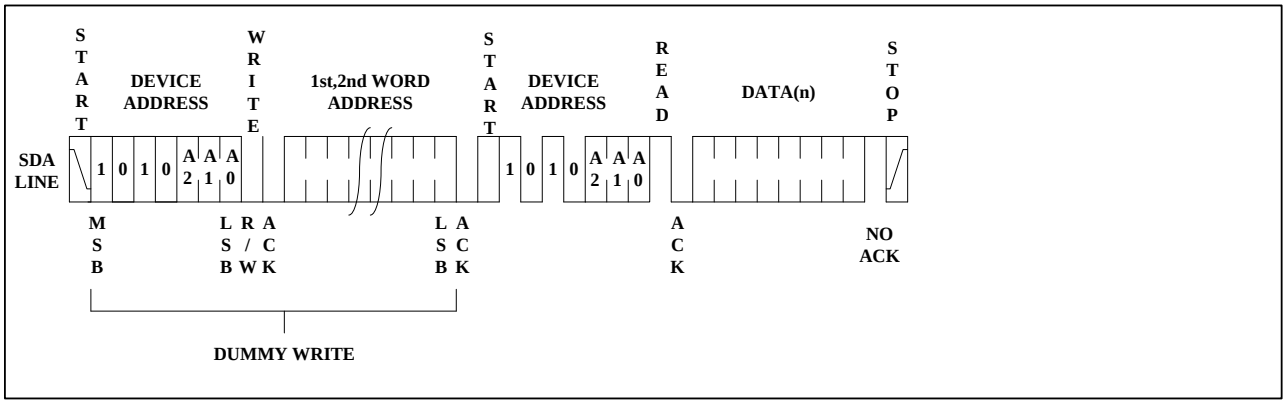


Figure 10. Random Read

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a "0" but does generate a following stop condition (see **Figure 11**).

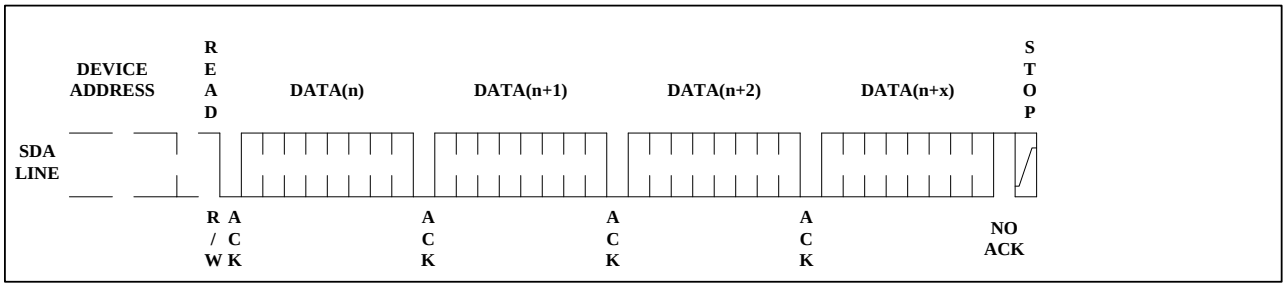


Figure 11. Sequential Read

6. Software write protection configuration

By writing specific values in a register (Table 3) located at address 11xx.xxxx.xxxx.xxxxb, the memory array can be write-protected by blocks.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Write	★	★	★	★	Partial Write protect activation	Size of write protected block	Size of write protected block	★
Read	0	0	0	0				0

Table 3

Notes:

Bit 7 – 4 and bit 0 are don't care bits.
Bit 3 enables or disables the partial write protection.
Bit 3=0: the whole memory can be written (no write protection)
Bit 3=1: the concerned block is write-protected
Bits 2 and 1 define the size of the memory block to be protected against write instructions:
Bit 2, Bit 1= 0, 0: the upper quarter of memory is write-protected
Bit 2, Bit 1= 0, 1: the upper half memory is write-protected
Bit 2, Bit 1= 1, 0: the upper 3/4 of memory are write-protected
Bit 2, Bit 1= 1, 1: the whole memory and the device addressing config register are write-protected
The device is delivered with the Write Protect register set to 0 (00h).

7. Device Addressing configuration

By writing specific values in a register (Table 4) located at address 10xx.xxxx.xxxx.xxxxb, the device address can be reconfigured.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Write	★	★	★	★	★	A2	A1	A0
Read	0	0	0	0	0			

Table 4

Note:

While the SWR register (Table 3) set to “0x0E”, bit3,bit 2, bit 1= 1, 1, 1, the device addressing config register (Table 4) is write-protected.

8. Electrical Characteristics

Absolute Maximum Stress Ratings:

- DC Supply Voltage . . . . . -0.3V to +6.5V
- Input / Output Voltage . . . . . GND-0.3V to VCC+0.3V
- Operating Ambient Temperature . . . . . -40℃ to +85℃
- Storage Temperature . . . . . .-65℃ to +150℃
- Electrostatic pulse (Human Body model) 6000V

Comments:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

Applicable over recommended operating range from: TA = -40℃ to +85℃, VCC = +1.7V to +3.6V (unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Supply Voltage	VCC1	1.7	-	3.6	V	-
Supply Current VCC=1.8V	ICC1	-	0.14	0.3	mA	READ at 400KHZ
Supply Current VCC=1.8V	ICC2	-	0.28	0.5	mA	WRITE at 400KHZ
Supply Current VCC=1.8V	ISB1	-	0.03	0.5	μA	VIN=VCC or VSS
Input Leakage Current	IL1	-	0.10	1.0	μA	VIN=VCC or VSS
Output Leakage Current	IL0	-	0.05	1.0	μA	VOUT=VCC or VSS
Input Low Level	VIL1	-0.3	-	VCC×0.3	V	VCC=1.7V to 5.5V
Input High Level	VIH1	VCC×0.7	-	VCC+0.3	V	VCC=1.7V to 5.5V
Output Low Level VCC=1.7V	VOL1	-	-	0.2	V	IOL=0.15mA
Output Low Level VCC=5.0V	VOL2	-	-	0.4	V	IOL=3.0mA

Table 5

Pin Capacitance

Applicable over recommended operating range from TA = 25℃, f = 1.0 MHz, VCC = +1.7V

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Input/Output Capacitance(SDA)	CI/O	-	-	8	pF	VIO=0V
Input Capacitance(A0,A1,A2,SCL)	CIN	-	-	6	pF	VIN=0V

Table 6

AC Electrical Characteristics

Applicable over recommended operating range from TA = -40℃ to +85℃, VCC = +1.7V to +3.6V, CL = 1 TTL Gate and 100 pF (unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Units
Clock Frequency, SCL	f_{SCL}	-	-	400	-	-	1000	KHZ
Clock Pulse Width Low	t_{LOW}	1.3	-	-	0.5	-	-	μs
Clock Pulse Width High	t_{HIGH}	0.6	-	-	0.26	-	-	μs
Noise Suppression Time	t_I	-	-	50	-	-	50	ns
Clock Low to Data Out Valid	t_{AA}	-	-	0.9	-	-	0.45	μs
Time the bus must be free before a new transmission can start	t_{BUF}	1.3	-	-	0.5	-	-	μs
Start Hold Time	$t_{HD:STA}$	0.6	-	-	0.25	-	-	μs
Start Setup Time	$t_{SU:STA}$	0.6	-	-	0.25	-	-	μs
Data In Hold Time	$t_{HD:DAT}$	0	-	-	0	-	-	μs
Data in Setup Time	$t_{SU:DAT}$	100	-	-	100	-	-	ns
Input Rise Time(1)	t_R	-	-	0.3	-	-	0.12	μs
Input Fall Time(1)	t_F	-	-	0.3	-	-	0.12	μs
Stop Setup Time	$t_{Su:STO}$	0.6	-	-	0.25	-	-	μs
Data Out Hold Time	t_{DH}	50	-	-	50	-	-	ns
Write Cycle Time	t_{WR}	-	1.9	3	-	1.9	3	ms
5.0V, 25℃, Byte Mode(1)	Endurance	1M	-	-	1M	-	-	Write Cycle

Table 7

Notes:

1. This parameter is characterized and is not 100% tested.
2. AC measurement conditions:
   RL (connects to VCC): 1.3 k
   Input pulse voltages: 0.3 VCC to 0.7 VCC
   Input rise and fall time: 50 ns
   Input and output timing reference voltages: 0.5 VCC
   The value of RL should be concerned according to the actual loading on the user's system.

Bus Timing

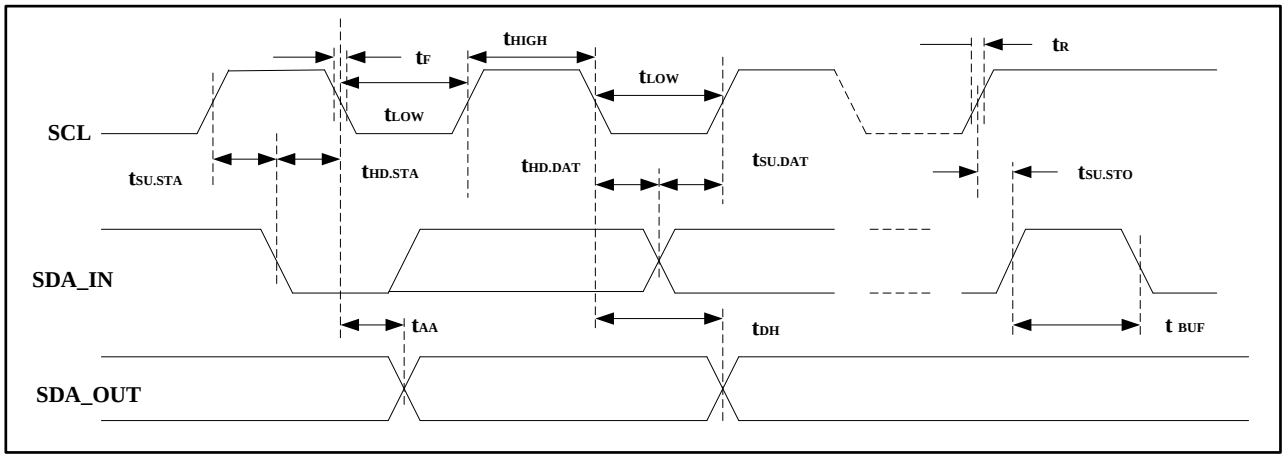


Figure 12. SCL: Serial Clock, SDA: Serial Data I/O

Write Cycle Timing

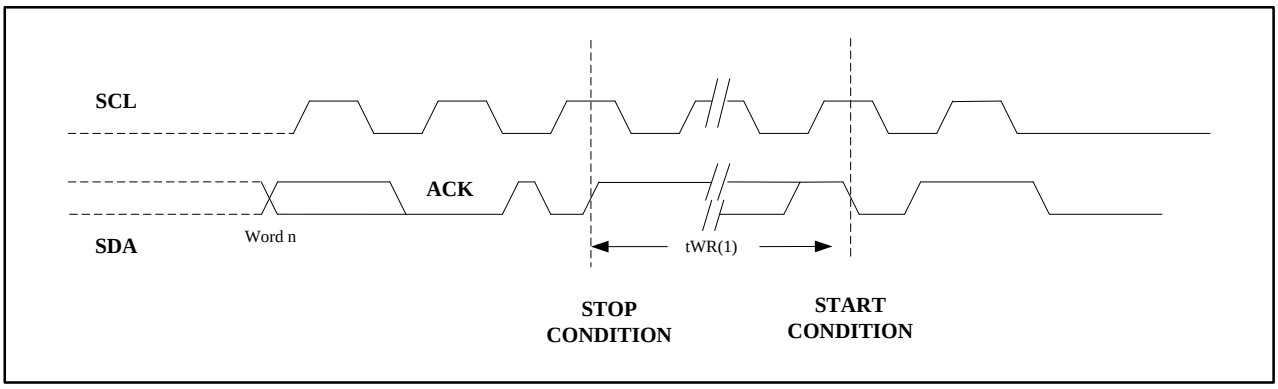


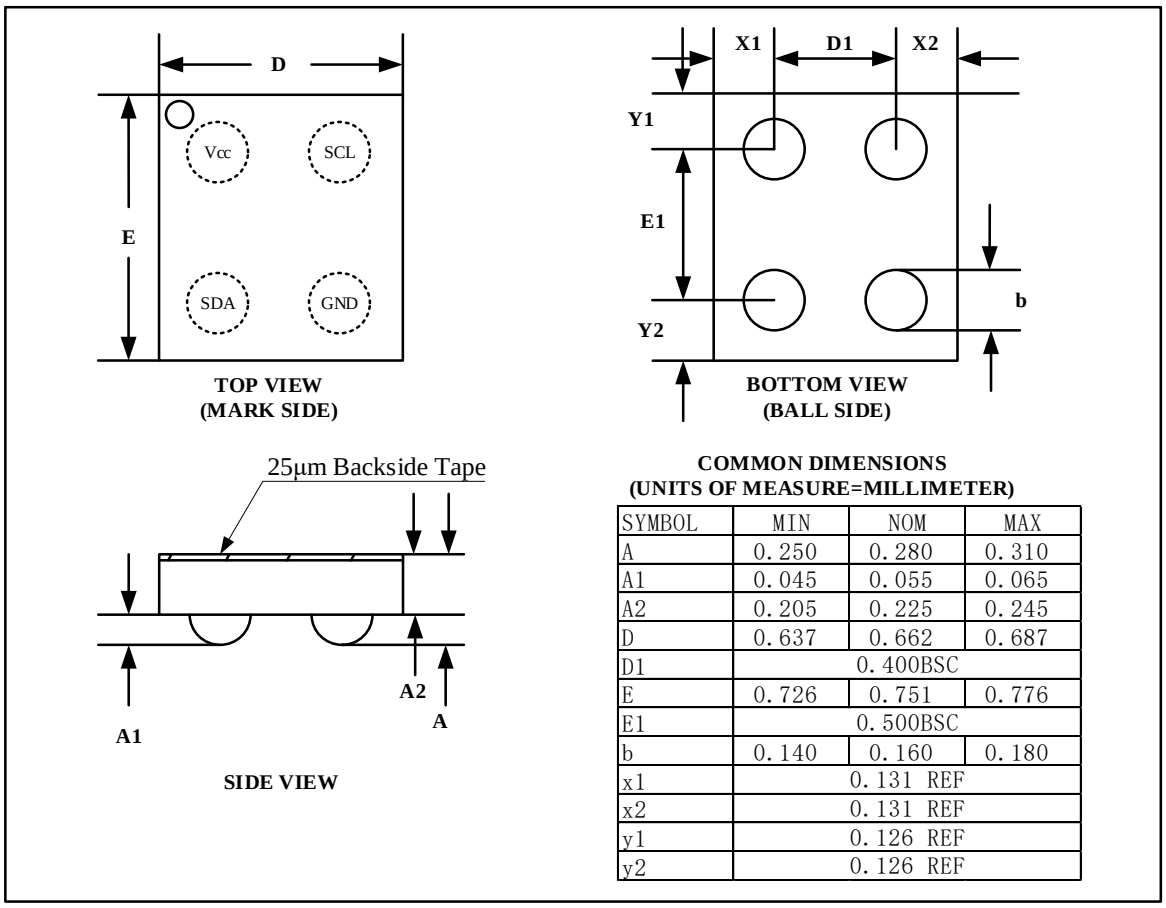
Figure 13. SCL: Serial Clock, SDA: Serial Data I/O

Notes:

The write cycle time tWR is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

Package Information

WLCSP 4 Ball Pitch 0.4mm*0.5mm

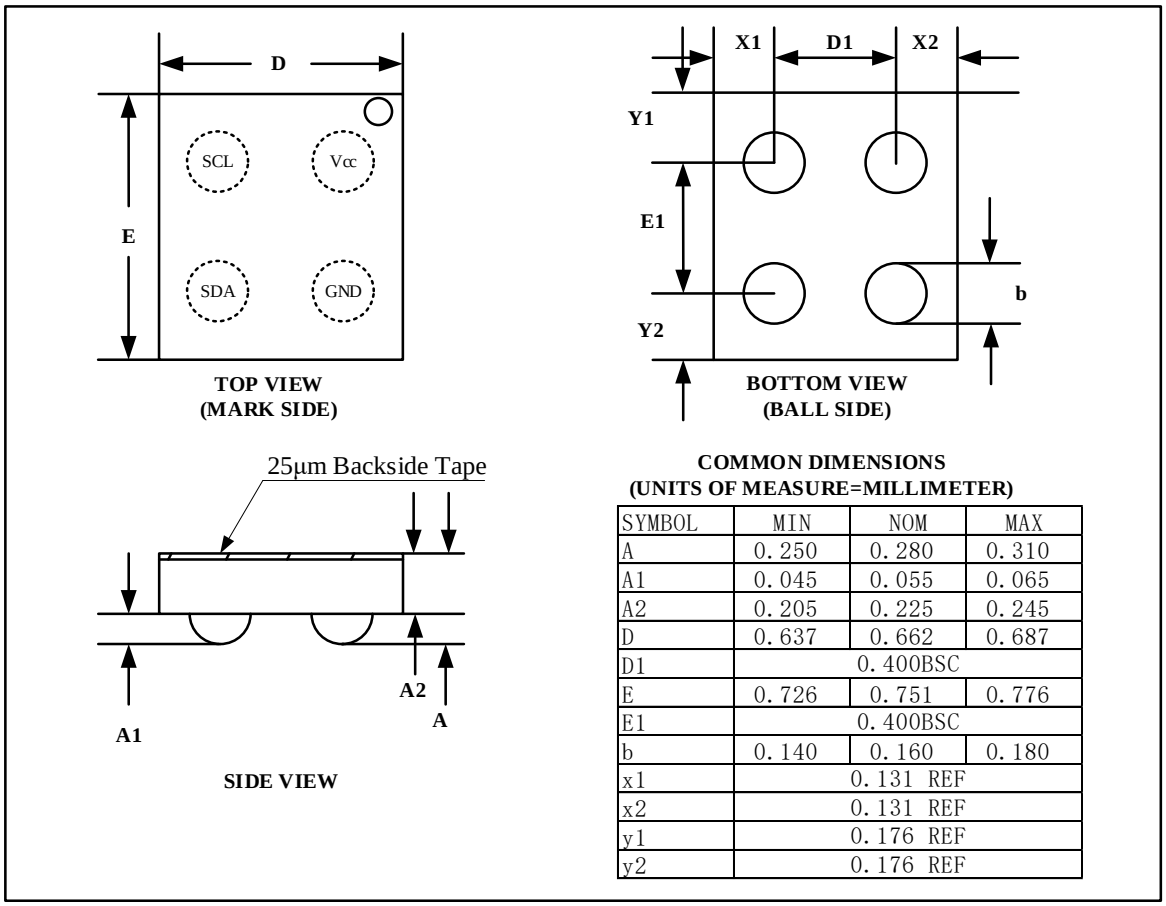


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.250	0.280	0.310
A1	0.045	0.055	0.065
A2	0.205	0.225	0.245
D	0.637	0.662	0.687
D1		0.400BSC	
E	0.726	0.751	0.776
E1		0.500BSC	
b	0.140	0.160	0.180
x1		0.131 REF	
x2		0.131 REF	
y1		0.126 REF	
y2		0.126 REF	

Figure 14

WLCSP 4 Ball Pitch 0.4mm*0.4mm



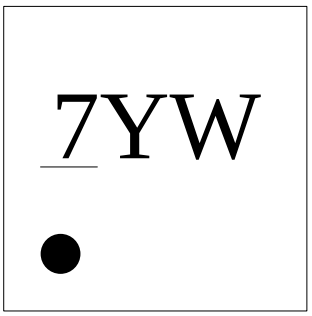
COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.250	0.280	0.310
A1	0.045	0.055	0.065
A2	0.205	0.225	0.245
D	0.637	0.662	0.687
D1		0.400BSC	
E	0.726	0.751	0.776
E1		0.400BSC	
b	0.140	0.160	0.180
x1		0.131 REF	
x2		0.131 REF	
y1		0.176 REF	
y2		0.176 REF	

Figure 15

Marking Diagram

WLCSP 4 Ball Pitch 0.4mm*0.5mm



1 PIN MARK

Y:The last digits of the year

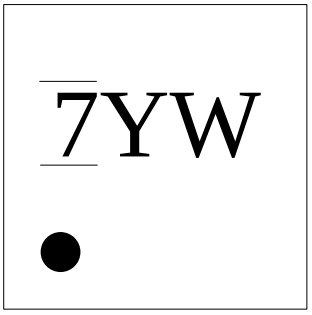
W:week code.

Y	1	…	3	4	5	…	9	0
Year	2021	…	2023	2024	2025	…	2019	2020

W	A	…	Y	Z	a	…	y	z
Week	1	…	25	26	27	…	51	52

Part Number	Mark
BL24SA128D-CS	7YW
BL24SA128DA2-CS	7YW
BL24SA128DA4-CS	7ȲW
BL24SA128DA6-CS	7ȲW
BL24SA128DA8-CS	7YW
BL24SA128DAA-CS	7YW
BL24SA128DAC-CS	7ȲW
BL24SA128DAE-CS	7ȲW

WLCSP 4 Ball Pitch 0.4mm*0.4mm



1 PIN MARK

Y:The last digits of the year

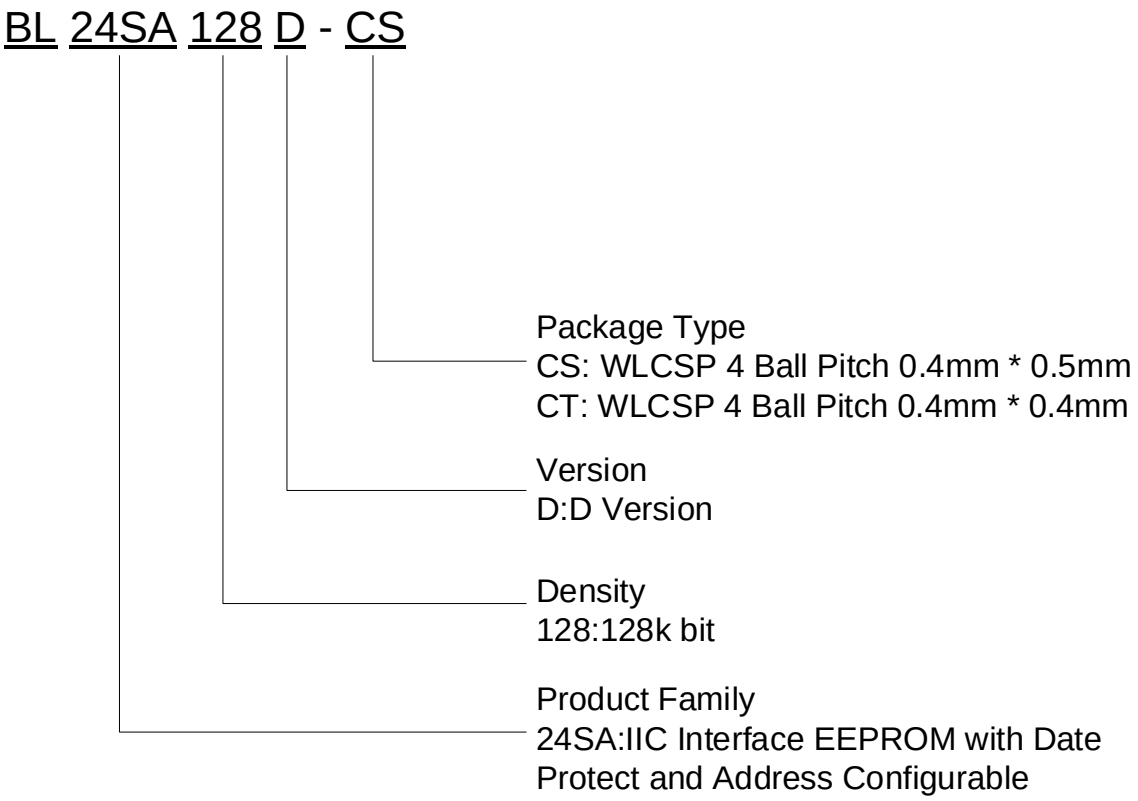
W:week code.

Y	1	…	3	4	5	…	9	0
Year	2021	…	2023	2024	2025	…	2019	2020

W	A	…	Y	Z	a	…	y	z
Week	1	…	25	26	27	…	51	52

Part Number	Mark
BL24SA128D-CT	7YW
BL24SA128DA2-CT	7YW
BL24SA128DA4-CT	7YW
BL24SA128DA6-CT	7YW
BL24SA128DA8-CT	7YW
BL24SA128DAA-CT	7YW
BL24SA128DAC-CT	7YW
BL24SA128DAE-CT	7YW

Ordering Information



Device	Package	Shipping (Qty/Packing)
BL24SA128D	WLCSP-4, 0.662*0.751 (Pb-Free/Halogen Free)	5000/Tape &Reel

Revision history

Version 1.00 BL24SA128D	**12/19/2019**
Initial Version	
Version 1.01 BL24SA128D	**6/4/2020**
Update the software write protection description	