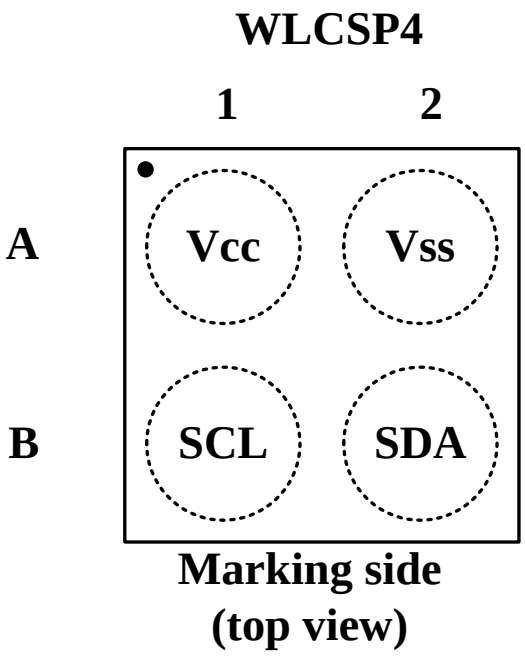
Features

- Compatible with all I²C bidirectional data transfer protocol
- Memory array:
  - 64 Kbits (8 Kbytes) of EEPROM
  - Page size: 32 bytes
- Single supply voltage and high speed:
  - 1 MHz
- Random and sequential Read modes
- Write:
  - Byte Write within 3 ms
  - Page Write within 3 ms
  - Partial Page Writes Allowed
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- High-reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
- Enhanced ESD/Latch-up protection
  - HBM 8000V
- WLCSP4 packages

Description

- The BL24C64A provides 65536 bits of serial electrically erasable and programmable read-only memory (EEPROM), organized as 8192 words of 8 bits each.
- The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential.

Pin Configuration



	Pin Name	Type	Functions
A1	Vcc	P	Power Supply
A2	Vss	P	Groung
B1	SCL	I	Serial Clock Input
B2	SDA	I/O	Serial Data

Table 1

Block Diagram

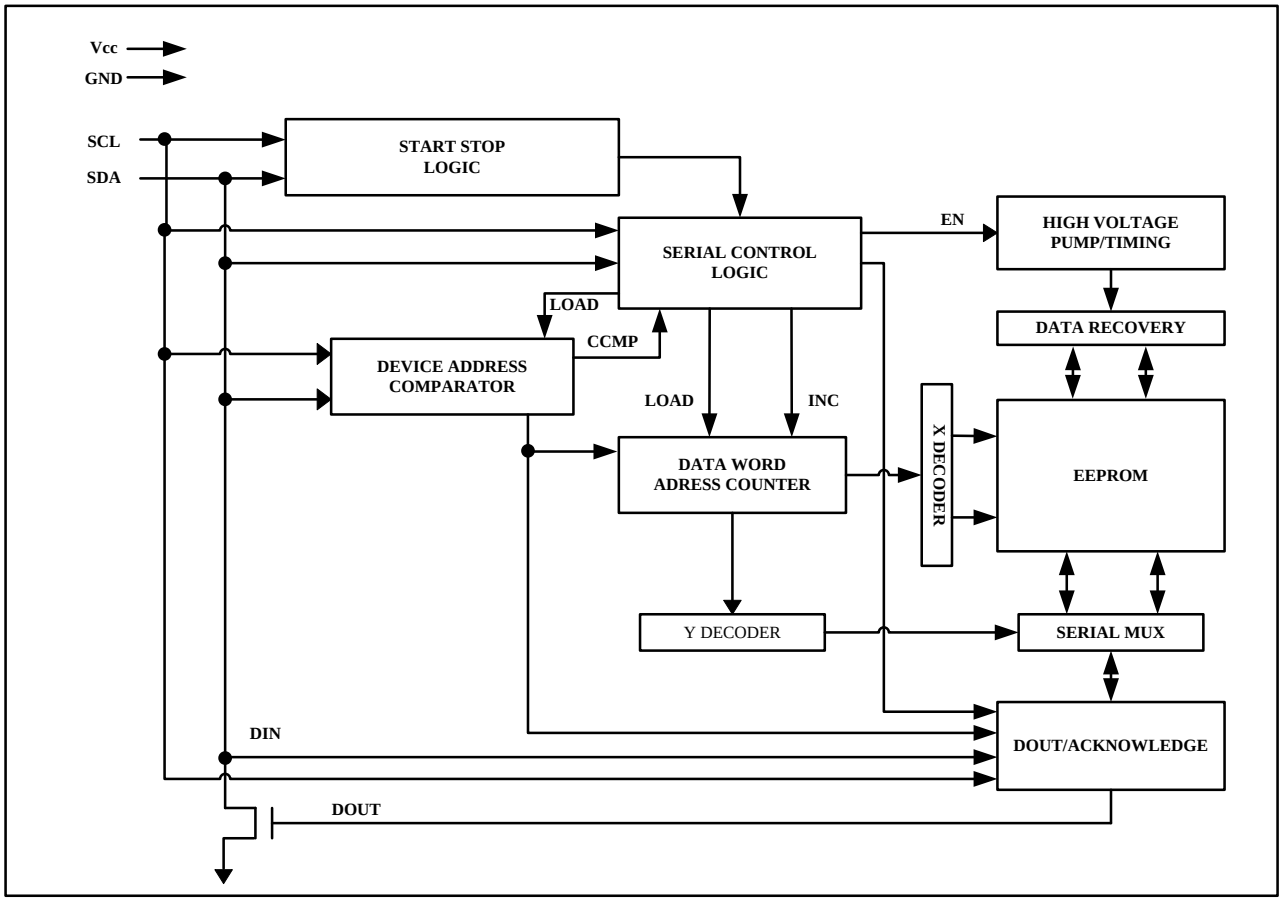


Figure 1

SERIAL DATA (SDA): The SDA pin is bi-directional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open- collector devices.

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

Functional Description

1. Memory Organization

BL24C64A, 64K SERIAL EEPROM: Internally organized with 256 pages of 32 bytes each, the 64K requires a 13-bit data word address for random word addressing.

2. Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see **Figure 2**). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see **Figure 3**).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (see **Figure 3**).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a "0" to acknowledge that it has received each word. This happens during the ninth clock cycle.

STANDBY MODE: The BL24C64A features a low-power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the STOP bit and the completion of any internal operations.

MEMORY RESET: After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these steps:

1. Clock up to 9 cycles.

2. Look for SDA high in each cycle while SCL is high.

3. Create a start condition.

ILLEGAL INSTRUCTION : The EEPROM maybe sends a "0" to acknowledge that it has received any one of the following two instruction as write/read instructions.

1.Device address=1011 0000b.

2.Device address=1011 0001b

If device address=1011 0001b,next step need 9 cycles Clock to stop the instruction.

Figure 2. Data Validity

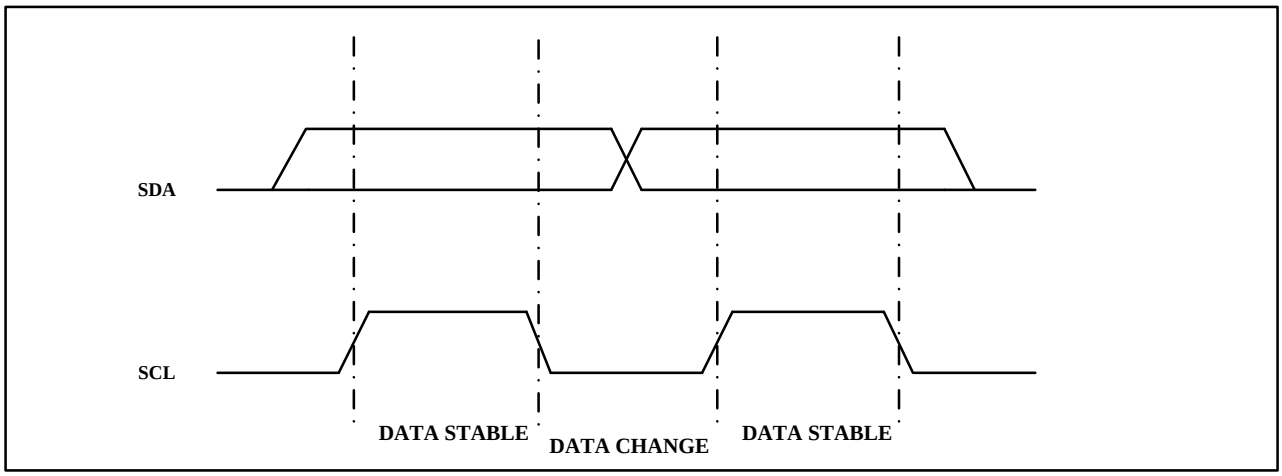


Figure 3. Start and Stop Definition

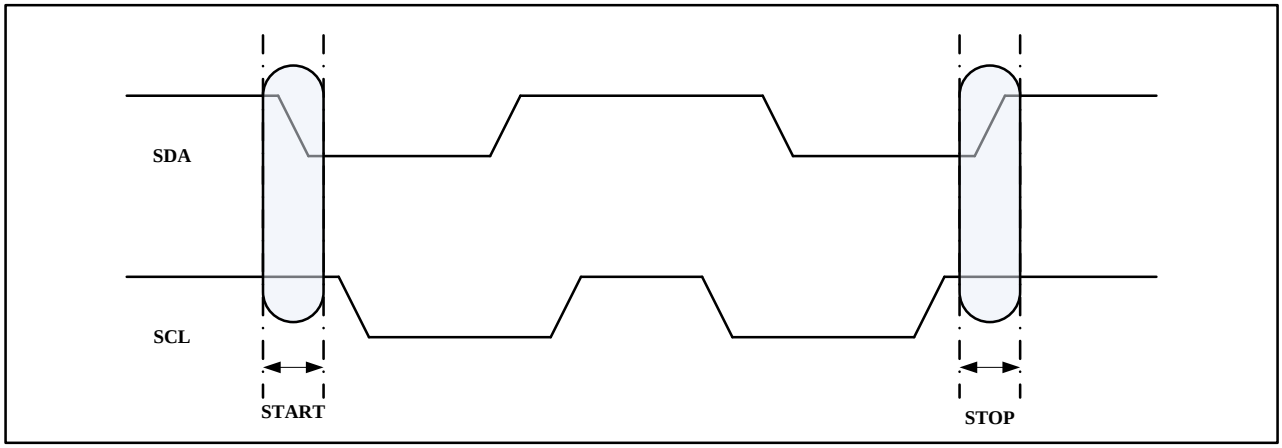
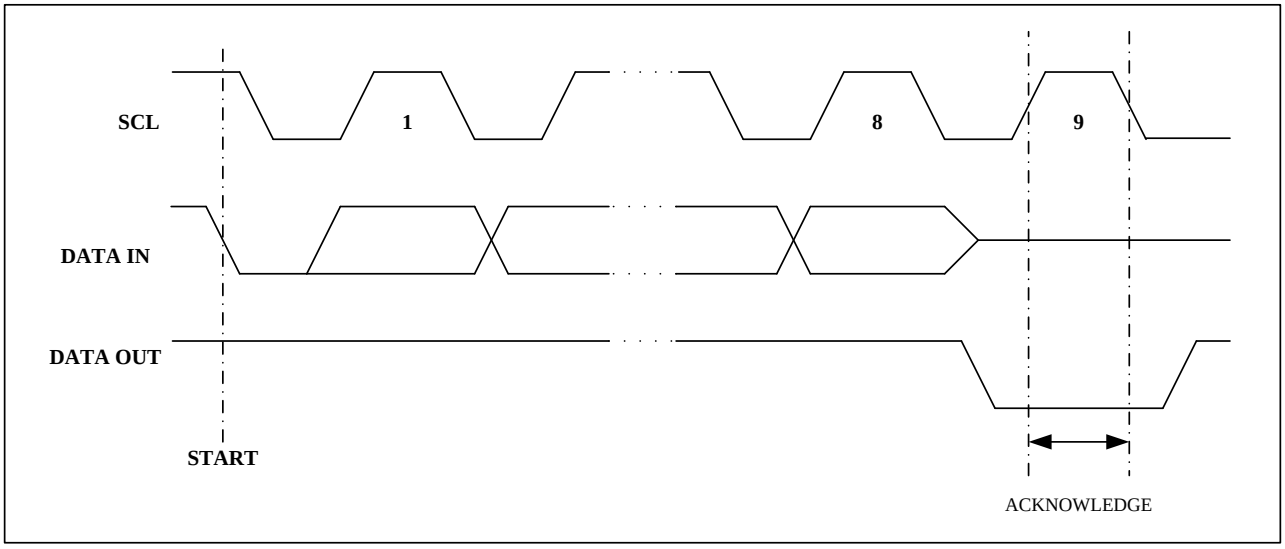


Figure 4. Output Acknowledge



3. Device Addressing

The 64K EEPROM devices all require an 8-bit device address word following a start condition to enable the chip for a read or write operation (see **Figure 5**)

The device address word consists of a mandatory "1", "0" sequence for the first four most significant bits as shown. This is common to all the Serial EEPROM devices.

The four most significant bits of the slave address are fixed (1010).

The next three bits are default to 0.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a "0". If a compare is not made, the chip will return to a standby state.

Figure 5. Device Address

MSB							LSB
1	0	1	0	0	0	0	R/W

4. Write Operations

BYTE WRITE: A write operation requires two 8-bit data word address, as Table2&Table3, following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a "0" and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a "0" and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, tWR, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see **Figure 6**).

PAGE WRITE: A write operation requires two 8-bit data word address, as Table2&Table3, following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a "0" and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a "0" and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, tWR, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see **Figure 7**).

The data word address lower five bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 32 data words are transmitted to the EEPROM, the data word address will "roll over" and previous data will be overwritten.

Table 2. FIRST WORD ADDRESS

0	0	0	B12	B11	B10	B9	B8

Table 3. SECOND WORD ADDRESS

B7	B6	B5	B4	B3	B2	B1	B0

ACKNOWLEDGE POLLING: Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a "0", allowing the read or write sequence to continue.

5. Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to "1". There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page. Once the device address with the read/write select bit set to "1" is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input "0" but does generate a following stop condition (see **Figure 8**).

RANDOM READ:A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a "0" but does generate a following stop condition (see **Figure 9**)

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a "0" but does generate a following stop condition (see **Figure 10**).

Figure 6. Byte Write

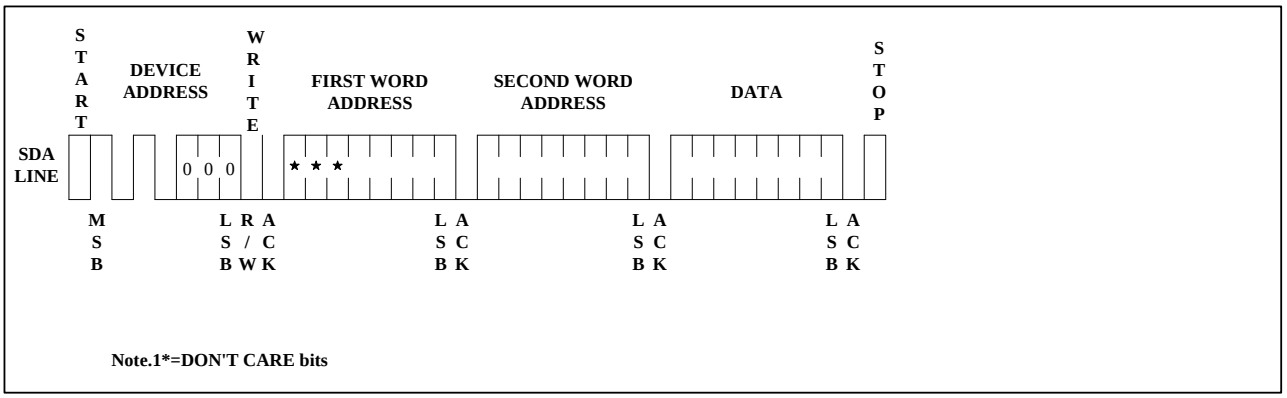


Figure 7. Page Write

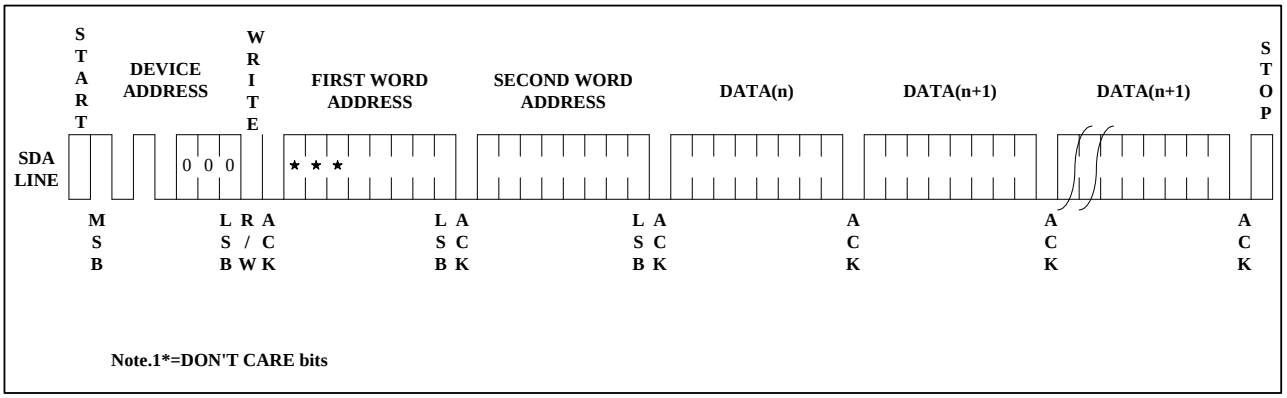


Figure 8. Current Address Read

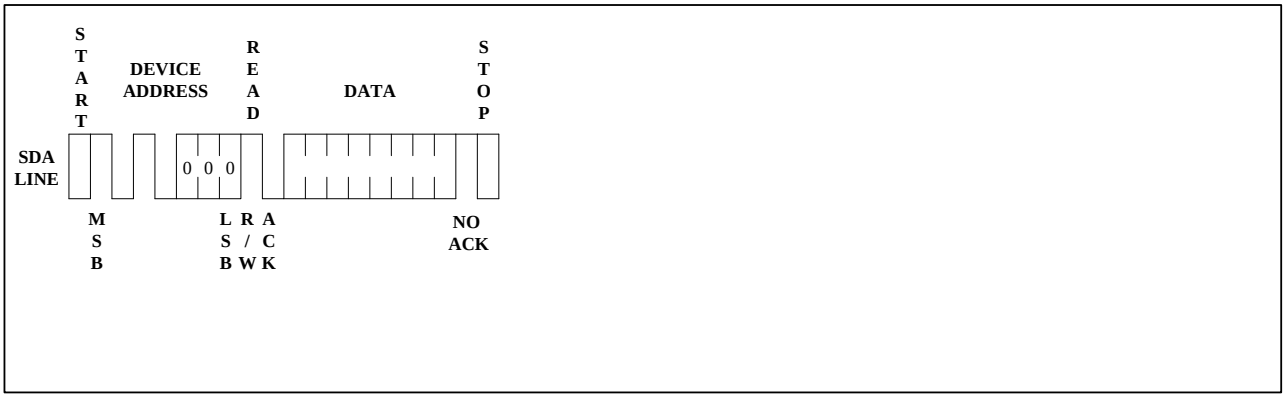


Figure 9. Random Read

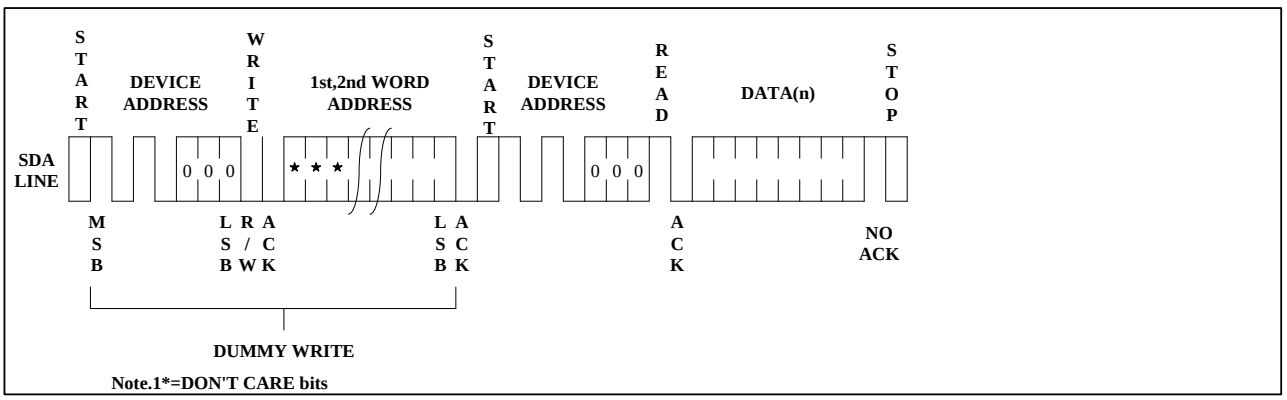
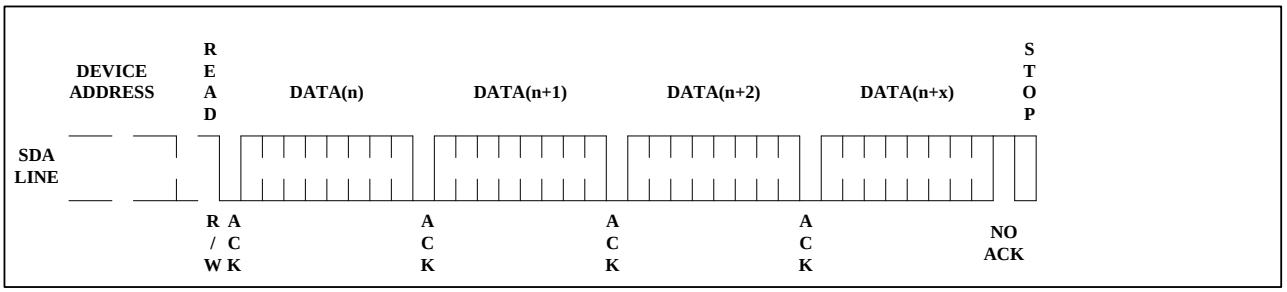


Figure 10. Sequential Read



Electrical Characteristics

Absolute Maximum Stress Ratings：

- DC Supply Voltage . . . . . .-0.3V to +6.5V
- Input / Output Voltage . . . . . .GND-0.3V to VCC+0.3V
- Operating Ambient Temperature . . . . . -40℃ to +85℃
- Storage Temperature . . . . . -65℃ to +150℃
- Electrostatic pulse (Human Body model) 8000V

Comments：

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

Applicable over recommended operating range from: TA = -40℃ to +85℃, VCC = +1.7V to +5.5V (unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Supply Voltage	V_{CC1}	1.7	-	5.5	V	-
Supply Current VCC=5.0V	I_{CC1}	-	0.14	0.3	mA	READ at 400KHZ
Supply Current VCC=5.0V	I_{CC2}	-	0.28	0.5	mA	WRITE at 400KHZ
Supply Current VCC=5.0V	I_{SB1}	-	0.03	0.5	μA	V_{IN}=Vcc or Vss
Input Leakage Current	I_{L1}	-	0.1	1.0	μA	V_{IN}=Vcc or Vss
Output Leakage Current	I_{LO}	-	0.05	1.0	μA	V_{OUT}=Vcc or Vss
Input Low Level	V_{IL1}	-0.3	-	Vcc×0.3	V	Vcc=1.7V to 5.5V
Input High Level	V_{IH1}	Vcc×0.7	-	Vcc+0.3	V	Vcc=1.7V to 5.5V
Output Low Level VCC=1.7V	V_{OL1}	-	-	0.2	V	I_{OL}=0.15mA
Output Low Level VCC=5.0V	V_{OL2}	-	-	0.4	V	I_{OL}=3.0mA

Table 4

Pin Capacitance

Applicable over recommended operating range from TA = 25℃, f = 1.0 MHz, VCC = +1.7V

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Input/Output Capacitance(SDA)	$C_{I/O}$	-	-	8	pF	V_{IO}=0V
Input Capacitance(SCL)	C_{IN}	-	-	6	pF	V_{IN}=0V

Table 5

AC Electrical Characteristics

Applicable over recommended operating range from TA = -40℃ to +85℃, VCC = +1.7V to +5.5V, CL = 1 TTL Gate and 100 pF (unless otherwise noted)

Parameter	Symbol	1.7V≤Vcc＜2.5V			2.5V≤Vcc＜5.5V			Units
		Min	Typ	Max	Min	Typ	Max	
Clock Frequency,SCL	f_{SCL}	-	-	400	-	-	1000	KHZ
Clock Pulse Width Low	t_{LOW}	0.6	-	-	0.6	-	-	μs
Clock Pulse Width High	t_{HIGH}	0.4	-	-	0.4	-	-	μs
Noise Suppression Time	t_I	-	-	50	-	-	50	ns
Clock Low to Data Out Valid	t_{AA}	0.1	-	0.55	0.1	-	0.55	μs
Time the bus must be free before a new transmission can start	t_{BUF}	0.5	-	-	0.5	-	-	μs
Start Hold Time	$t_{HD:STA}$	0.25	-	-	0.25	-	-	μs
Start Setup Time	$t_{SU:STA}$	0.25	-	-	0.25	-	-	μs
Data In Hold Time	$t_{HD:DAT}$	0	-	-	0	-	-	μs
Data in Setup Time	$t_{SU:DAT}$	100	-	-	100	-	-	ns
Input Rise Time(1)	t_R	-	-	0.3	-	-	0.3	μs
Input Fall Time(1)	t_F	-	-	0.3	-	-	0.3	μs
Stop Setup Time	$t_{Su:STO}$	0.25	-	-	0.25	-	-	μs
Data Out Hold Time	t_{DH}	50	-	-	50	-	-	ns
Write Cycle Time	t_{WR}	-	1.9	3	-	1.9	3	ms
5.0V,25℃,Byte Mode(1)	Endurance	1M	-	-	-	-	-	Write Cycle

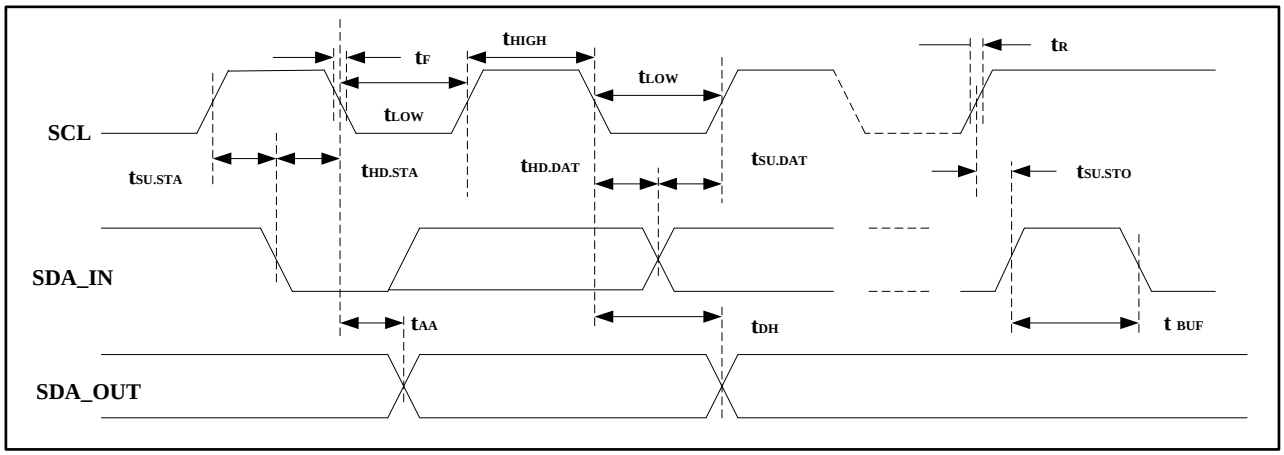
Table 6

Notes:

1. This parameter is characterized and is not 100% tested.
2. AC measurement conditions:
   RL (connects to VCC): 1.3 k
   Input pulse voltages: 0.3 VCC to 0.7 VCC
   Input rise and fall time: 50 ns
   Input and output timing reference voltages: 0.5 VCC
   The value of RL should be concerned according to the actual loading on the user's system.

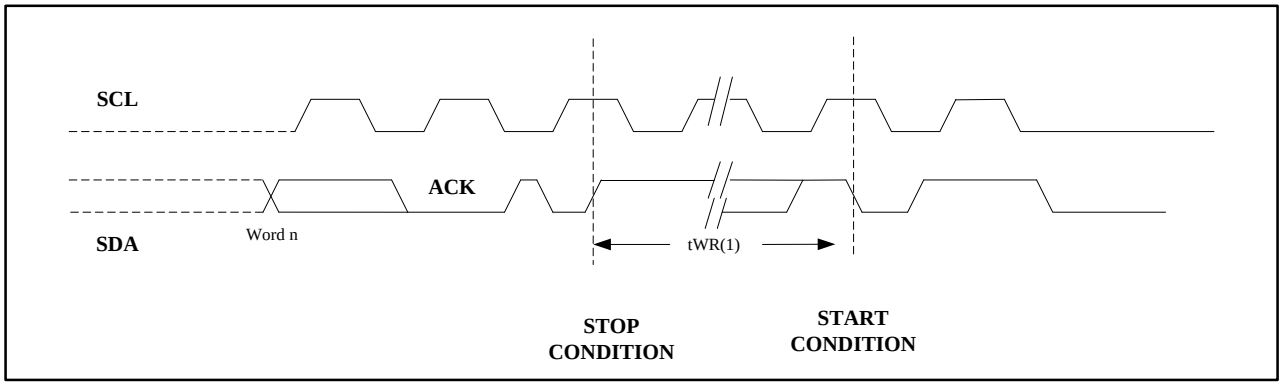
Bus Timing

Figure 11. SCL: Serial Clock, SDA: Serial Data I/O



Write Cycle Timing

Figure 12. SCL: Serial Clock, SDA: Serial Data I/O

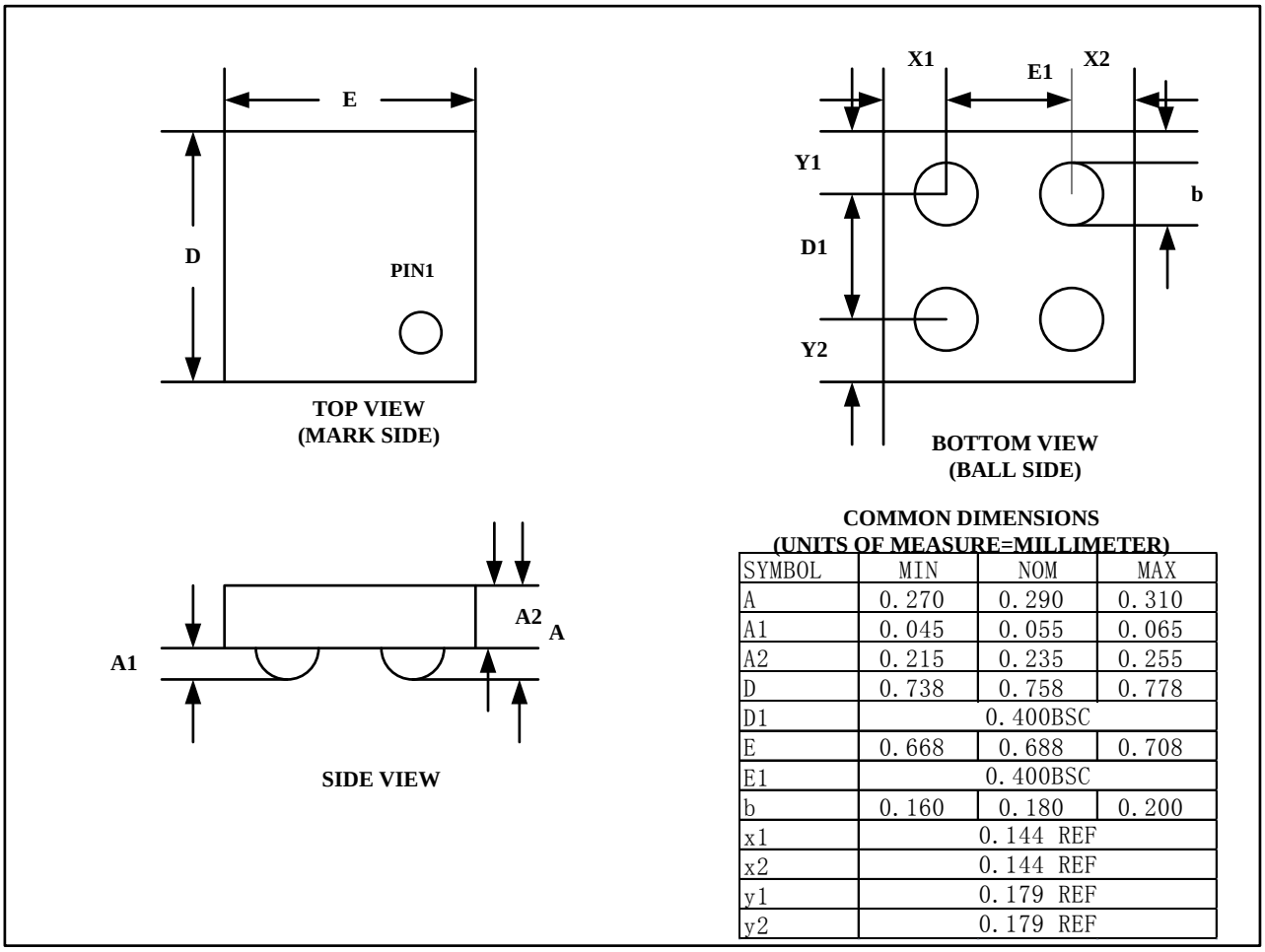


Notes:

The write cycle time tWR is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

Package Information

WLCSP



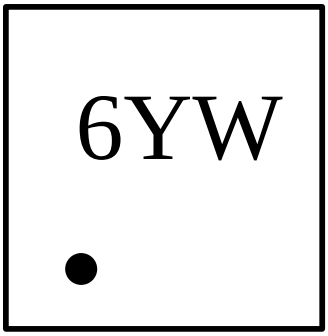
COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.270	0.290	0.310
A1	0.045	0.055	0.065
A2	0.215	0.235	0.255
D	0.738	0.758	0.778
D1		0.400BSC	
E	0.668	0.688	0.708
E1		0.400BSC	
b	0.160	0.180	0.200
x1		0.144 REF	
x2		0.144 REF	
y1		0.179 REF	
y2		0.179 REF	

Notes:

All wafer orientation notch down

Marking Diagram



● 1 PIN MARK

Y:The last digits of the year

W:week code.

Y	1	…	3	4	5	…	9	0
Year	2011	…	2013	2014	2015	…	2019	2020

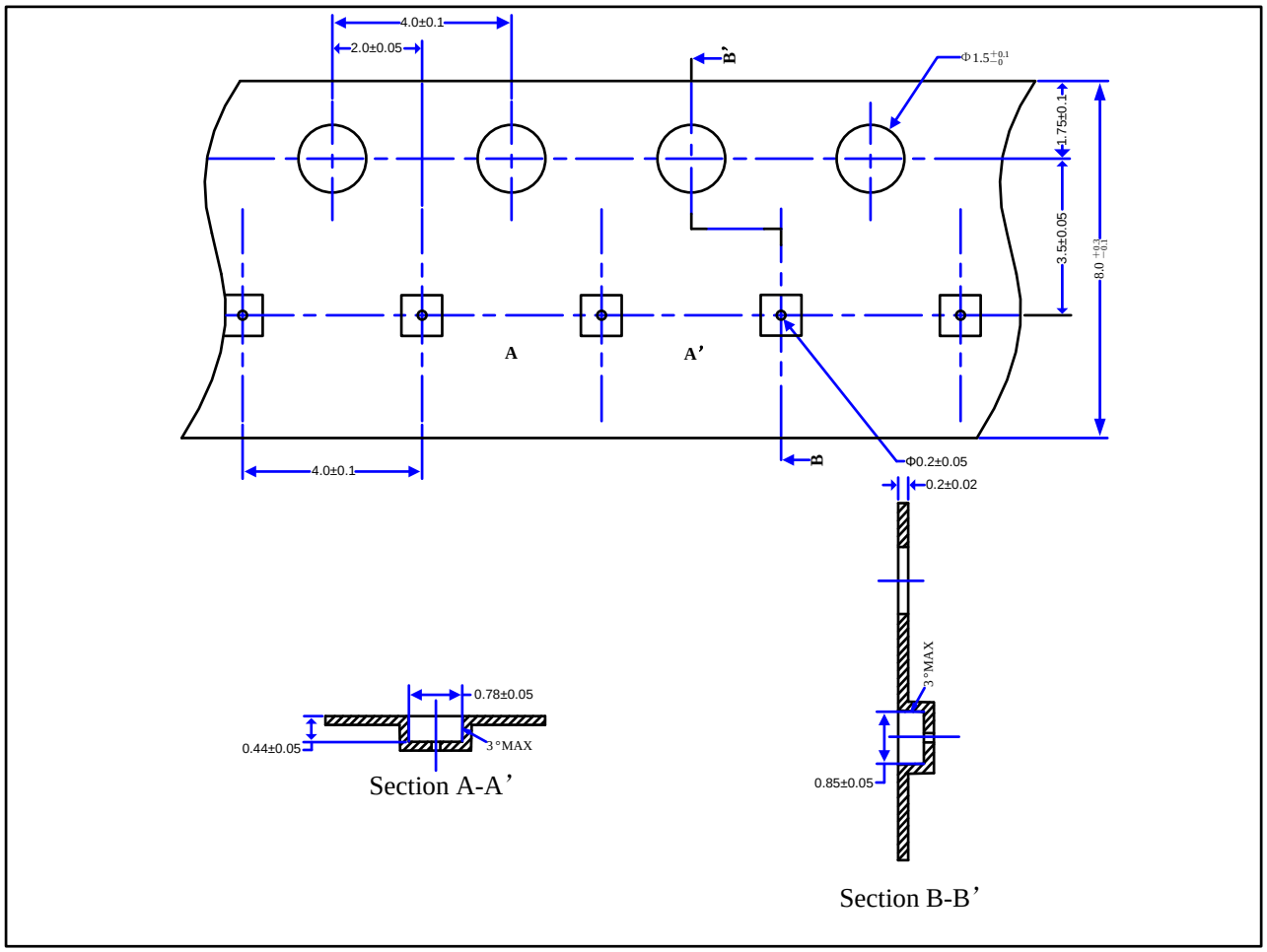
W	A	…	Y	Z	a	…	y	z
Week	1	…	25	26	27	…	51	52

Ordering Information

BL24C64A [1] [2]

Code	Description
1	Package type CS: WLCSP-4
2	Packing type R: Tape and Reel

Device	Package	Shipping(Qty/Packing)
BL24C64A-CS-R	WLCSP-4, 0.688*0.758 (Pb-Free/Halogen Free)	5000/Tape &Reel



Revision History

Vision 1.0 BL24C64A	
Initial version	
Vision 1.1 BL24C64A	
add marking diagram update ordering information	
Vision 1.2 BL24C64A	**7/21/2017**
update DC Electrical Characteristics information Modify the format	
Vision 1.21 BL24C64A	**7/26/2017**
update ordering information	
Vision 1.22 BL24C64A	**7/26/2017**
update Figure 6. Byte Write	